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The Electrical/Optical Transition Boards For 2004 Test Beam ATLAS Calorimeter Readout

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Abstract: The Electrical/Optical Transition Boards were designed and built for the ATLAS Liquid Argon (LAr) Calorimeter readout system in the Test Beam facility. These boards translate the electrical signals from the Module-0 Front-End Boards to the optical signals needed by the Readout Driver boards. They will be used to test and calibrate end-cap calorimeter components including electromagnetic, hadronic and forward calorimeter modules.

Key words: electrical, optical, transition, calorimeter, readout.

1 Introduction

During the 2004 Test Beam run of the end-cap calorimeter system [1] the data are collected by the "old style" module-0 Front-End Boards (FEB) [2]. These data are then transmitted for further processing to the Read-Out Driver (ROD) boards [3]. The module-0 FEBs have electrical outputs, while the ROD boards use optical inputs. The Electrical/Optical (E/O) Transition Boards were designed to translate the signals from the module-0 FEBs to the ROD boards. Each FEB needs one transition board. Additionally, separate boards also were designed to simulate the data sent by the FEBs and to provide parity error detection of the ROD boards. These simulation boards are used during the installation and debugging. The documentation of the E/O Transition Boards is presented in this note. The documentation of the simulation boards is described in the appendix.

2 The architecture of the E/O Transition Boards

The architecture of the E/O Transition Boards is shown in Fig. 1. The central component of the E/O Transition Board is a field programmable gate array (FPGA) device, EP1C6Q240C8 of the Cyclone family from Altera [4]. The functional modules indicated by the shaded blocks in Fig. 1 are all implemented in the FPGA device. In the module "Latch 1", the 32-bit input data from a FEB are latched at the rising edge of the input clock running at 40.08 MHz (the LHC/ATLAS frequency). In the module "MUX" the input clock is used to multiplex the 32-bit data into two consecutive 16-bit data and an additional flag bit. The flag bit indicates whether the high 16 bits or low 16 bits are sent. The phase-locked loop (PLL) inside the G-link

serializer “G-link Tx” generates a clock at 80.16 MHz, the double frequency of the input clock. The G-link serializer, HDMP-1022 from Agilent, is the transmitter of the commonly called G-link transmitter/receiver chip set [5]. The multiplexed data and the flag bit are latched in the module “Latch 2” at the rising edge of the delayed 80.16 MHz clock. The delay time can be adjusted to meet the setup and hold time requirements of the G-link serializer and of “Latch 2”. In the G-link serializer the parallel data are serialized into a serial data stream. The serial data stream is converted into optical signals in a custom optical transmitter “OTx” and sent out through an optical fiber to a ROD board. The optical transmitter is produced in the Academia Sinica of Taiwan [6].

The parity of each word is checked in the module “Parity Detector” and the checking results are displayed with several light emitting diodes (LED). The parity error detection function is useful during the installation and debugging. The block diagram of the module “Parity Detector” is shown in Fig. 2. In the module “Frame Border”, the FEB data are scanned to find out the beginning of a frame and the end of the frame. The module “Frame Border” also counts the number of frames. The parity of each word inside any frame is checked in the module “Parity Detector”. The number of the parity errors is counted in the module “Error Count”.

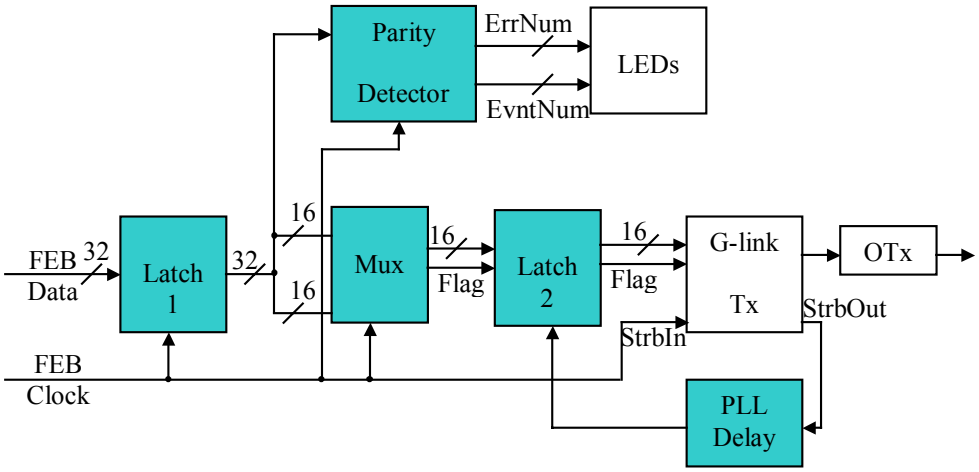

Figure 1. The block diagram of the E/O Transition Boards

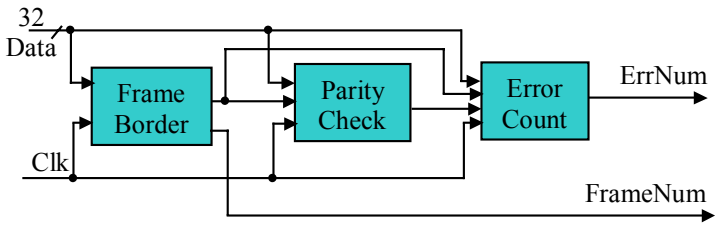

Figure 2. The block diagram of the parity error detector

A photograph of an E/O Transition Board connected to a simulation board is shown in Fig. 3. In this photograph the E/O Transition Board is on the right and the simulation board is on the left.

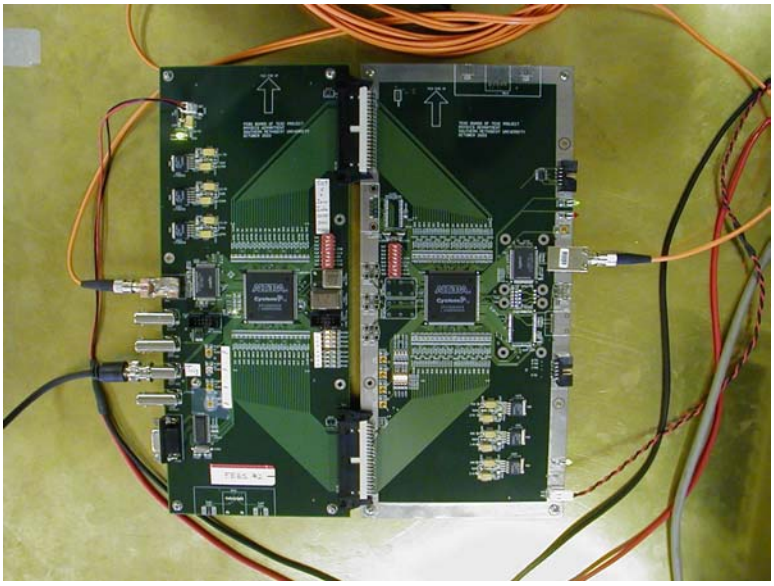

Figure 3. A photograph of an E/O Transition Board (right) and a simulation board (left)

3 Level translation in the E/O Transition Boards

The output signals of the module-0 FEBs are Positive Emitter Couple Logical (PECL) signals. The FPGA device used in the E/O Transition Boards does not support PECL signals. The PECL signals have to translate into the signals supported by the FPGA device. The FPGA device supports Low Voltage Differential Signaling (LVDS) signals. The translation from PECL to LVDS signals can be implemented by using a simple resistor and capacitor network. Therefore, LVDS is chosen to be the input

signals of the FPGA device. In the following we will discuss the translation from PCEL into LVDS signals.

The translation from PECL to LVDS signals can be achieved by either a DC coupling or by an AC coupling [7]. The AC coupling is simpler and uses less power than the DC coupling. The AC coupling also provides the "hot swapping" capability [8]. The AC coupling is perfect for the transmission of return-to-zero data or of non-return-to-zero but encoded data. For un-encoded non-return-to-zero data, such as the data from the FEBs, the AC coupling may cause transmission errors. The reason is explained in the following paragraph.

The AC coupling blocks the DC path of the data lines and requires bias voltages for the receiver inputs. When the levels on the transmitter side of the coupling capacitors transits from one logical level into the other logical level, the input levels on the receiver side follow respectively. After the transition, the input levels on the receiver sides decay exponentially back to the bias voltages. The recovery time for the input levels to go back to the bias levels depends on the time constant of the AC coupling circuit. If the data have another transition before the input levels to go back to the bias levels, the input levels change again and the data will be transmitted correctly. However, if the data contain the consecutive identical digits (logical ones or zeros) lasting longer than the recovery time, after the input levels return to their bias level the receiver output depends on the bias voltages and on the random noise instead of the inputs. Thus the transition errors may happen.

The consecutive logical ones in the FEBs data will not cause any transmission error because within the data structure of the FEB transmission no consecutive logical ones last longer than the recovery time. In fact, the recovery time in the E/O Transition Boards is 5 microseconds and corresponds to 25 words. In the FEB data there is an address word or a control word before and after consecutive 8 words of waveform sampling data. Bits 13 and 12 of the address word and of the control word are defined to be logical zeros [9]. Therefore, the consecutive logical ones last no longer than 9 words.

Since the consecutive logical ones will not cause any transmission error, the only possible problem is the long consecutive logical zeros. As mentioned above, after the recovery time of long consecutive logical zeros, the receiver output, depending on the bias voltages and on the random noise, may be logical ones and thus cause transmission errors. If the bias voltages are set negative to keep the receiver output at logical zeros after the recovery time, the AC coupling will not cause any problem. Since the bias voltage is normally set to be zero or near to zero [10], we call the concept described above the customized biasing.

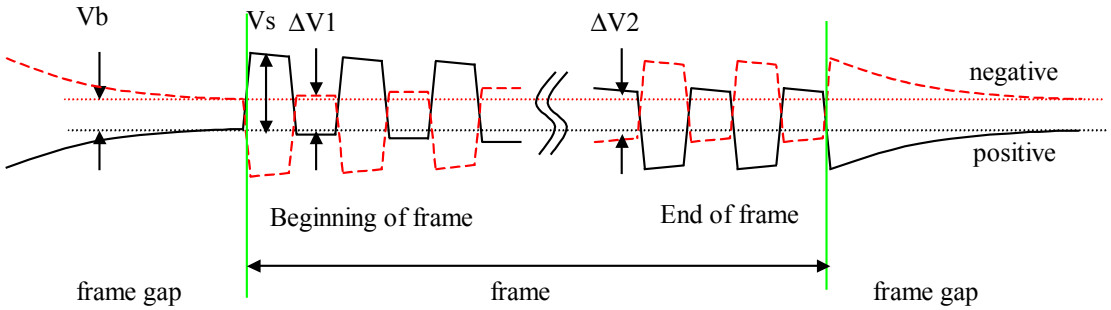

Figure 4. The waveforms of a differential input signal on the receiver side

The customized biasing is illustrated in Fig. 4. The negative input data line (red dashed curve) is biased higher than the positive input data line (black solid curve), so that the differential bias voltage is negative (-Vb in Fig. 4.) Here, Vb is the absolute value of the differential bias voltage. The positive and negative input voltages go back to their bias voltages on the left and the right sides of Fig. 4 after long consecutive logical zeros in frame gaps, but the negative differential bias voltage keeps the receiver output at logical zeros.

A compromise has to be made when choosing the bias voltages. On one hand, the bias voltage should be big (negative) enough for the noise not to affect the receiver output after the recovery time during long consecutive logical zeros transmission. On the other hand, the bias voltages should not be too big to affect the receiver output before the recovery time during the normal data transition.

In Fig. 4, in the beginning of a frame, the voltages on the positive and the negative data lines swing on the base of their bias voltages. The differential input voltage is 2Vs–Vb for logical ones, and Vb for logical zero, where Vs is the slew amplitude. The differential noise margin, ΔV1 in Fig. 4, is equal to Vb in the beginning of the frame. If a frame lasts long enough, and if the data are balanced between logical zeros and logical ones, in the end of the frame the voltages on the positive and negative data lines will swing centered at their bias voltages. The differential input voltage is Vs–Vb for logical one, and Vs+Vb for logical zero. The differential noise margin, ΔV2, is Vs-Vb in the end of the frame.

With the above considerations, the optimal choice is to set the differential noise margin in the beginning of the frame equal to the differential noise margin in the end of the frame. This choice leads to Vb = Vs/2. For PECL signals coming Vs is about 800mV, and thus the optimal differential bias voltage is about 400mV.

The schematic of the bias circuit is shown in Fig. 5. C1 and C2 are coupling capacitors. R1, R2 and Rt are the resistor network to provide the bias voltages. The bias network should meet three conditions. First, the differential input resistor should be equal to the differential impedance of coaxial transmission cables, 100Ω. Second, the differential bias voltage should be 400mV as discussed above. Finally, the bias voltages should be in the input voltage range, which is normally from the ground to the power voltage. A simple choice of the third condition is to set the average bias voltage, (Vn+Vp)/2, as a half of the power voltage, 1.25V. This choice leads to R1 = R2. Combining these three conditions, we get R1 and R2 as 316Ω and Rt as 120Ω.

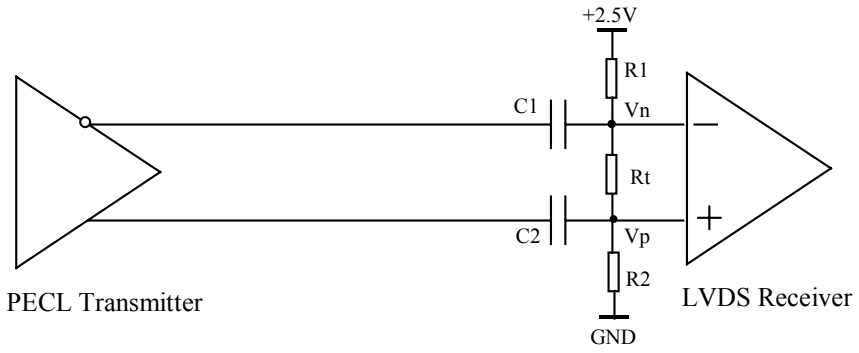

Figure 5. The schematic of the bias circuit

4 The test of the E/O Transition Boards

The E/O Transition Boards were tested in the lab. During the test the data were generated by a simulation board, passed through an E/O Transition Board and an optical fiber, and received back at the simulation board to detect the parity error. In general, the simulation board can generate a single bit error or periodic bit errors so that the error detection can be verified. All E/O Transition Boards run error free in the lab condition for more than 12 hours, corresponding to a bit error rate of less than 2×10^{-14}.

Next the E/O Transition Boards were tested in the Test Beam environment. Each FEB worked with an E/O Transition Board plugged in. The data parity was checked in a ROD board or in a simulation board. The received data were also transferred from the simulation board to a computer and the parity was checked. All E/O Transition Boards worked well in these tests and run error free for over 12 hours. This corresponds to a bit error rate less than 2×10^{-14}.

5. Conclusion

The E/O Transition Boards were designed and built for the ATLAS Liquid Argon Calorimeter readout system in the Test Beam facility. These boards were tested in the lab and in the experimental environment. They are used for the calorimeter readout in 2004 Test Beam run.

Acknowledges:

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Appendix A

The Simulation Board Structure Description

The simulation boards were designed to simulate data generation of the module-0 FEBs and parity error detection of the ROD boards.

The simulation boards contain two independent parts. The FEB simulation part generates the data in the FEB format. The ROD simulation part detects if there is a parity error in the received data. The ROD simulation can also dump the received data into a computer for further processing. Two parts can be used at the same time. Any part can also be used independently without the other.

The architecture of the simulation boards is shown in Fig. A1. The FEB simulation part is on the top, and ROD simulation part is on the bottom. The central component of the E/O Transition Board is a FPGA device, EP1C6Q240C8 of the Cyclone family from Altera. All shaded blocks in Fig. A1 are implemented in this FPGA device.

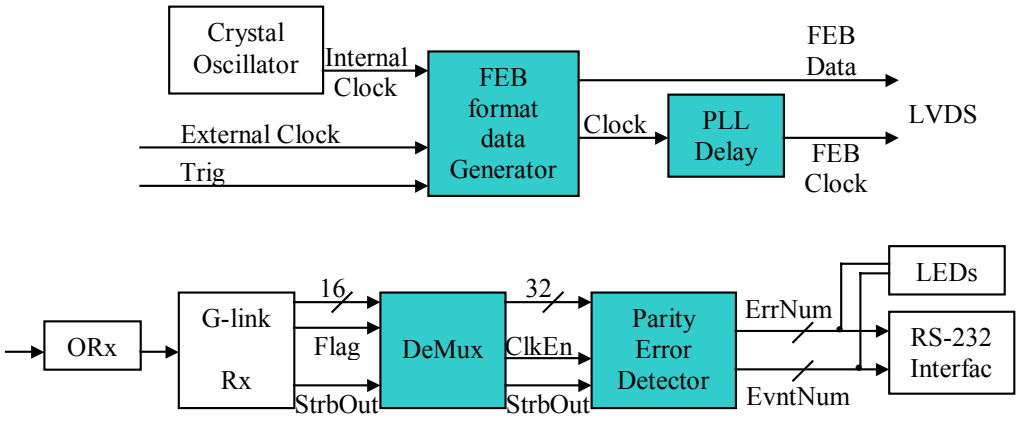

Figure A1. The architecture of the simulation boards

The FEB simulation part generates the data in the FEB format using an external trigger signal and either an external clock signal or an internal clock from an on-board crystal oscillator. The module "PLL Delay" is used to simulate the module-0 FEB timing between the output data and the output clock. The output data and clock are all LVDS signals.

The ROD simulation part detects the parity error. The optical signal is converted into the electrical signal in the optical receiver ("ORx"). The parallel data (16-bit parallel data and 1-bit flag indicating whether high 16 bits or low 16 bits are received) and the

clock (StrbOut at 80.16 MHz) are recovered from the serial electrical signal in the G-link deserializer ("G-link Rx"). The 32 bit data at 40.08 MHz are then extracted from the 16-bit data at 80 MHz based on the flag bit in the demultiplexer ("DeMux"). The frame structure is analyzed in the parity error detector. The parity error detector also counts the number of frames and checks for a parity error. The number of frames and the number of parity errors can be displayed with several on-board LEDs. The whole frame of data can be sent to a computer through a serial port for further processing.

The block diagram of the module "FEB format data generator" is shown in Fig. A2. "Word Clk Gen" generates the clock enable signal of each word. "Frame Data" generates all 16 parallel 32-bit data. The data generated simulate linear waveforms. The simulation data meet the FEB data format and are used to test the E/O Transition Boards. It does not contain any specific information. The module "Parity" generates a parity bit for each word. According to the FEB format requirement, all words inside a frame except the beginning word of the frame and the end word of the frame have odd parity. The module "Serialize" outputs the parallel 16-bit data in serial data stream, 2 bits in each clock period. The output data are 32 bits.

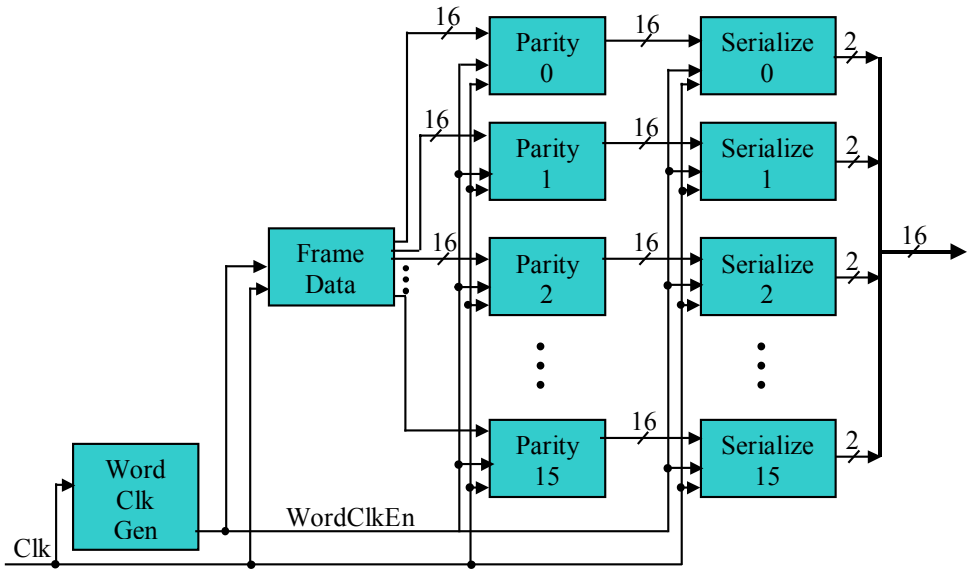

Figure A2. The block diagram of "FEB format Data Generator"

Appendix B

The E/O Transition Board Data Sheet

B1. The board specifications

The E/O Transition Board works with single +5V power supply. The power can be supplied either from a module 0 FEB board or a simulation board (with two jumpers shorted), or from an independent power supply source. The specifications for the power supply are listed in Table B1.

Table B1. The specifications for the power supply

Symbol	Parameters	Unit	Min	Typ.	Max
V_{CC}	Power supply voltage	V	4.5	5.0	5.5
I_{CC}	Power supply current	A		0.79	

Parallel 32-bit data and two identical clocks are sent into the board. They are recognized as differential LVDS signals. The data are sampled at the rising edge of a clock. Their specifications are listed in Table B2.

Table B2. The data and clock signal specifications

Symbol	Parameters	Unit	Min	Typ.	Max
V_{TH}	Differential input voltage to guarantee logical high	V	0.1		
V_{TL}	Differential input voltage to guarantee logical low	V			-0.1
V_{IN}	Input voltage range	V	0		2.4
V_{BPD}	Positive bias voltage of the data	V		1.45	
V_{BND}	Negative bias voltage of the data	V		1.05	
V_{BPC}	Positive bias voltage of the clocks	V		1.24	
V_{BNC}	Negative bias voltage of the clocks	V		1.21	
R_{IN}	Differential input impedance	Ω		100	
f_{clock}	Clock frequency	MHz		40.08	
η_{clock}	Clock duty cycle	%		50	
t_{su}	Data setup time	ns	3.0		
t_h	Data hold time	ns	0		

The optical signal is sent out to an optical fiber. The optical signal specifications are listed in Table B3.

Table B3. The optical signal specifications

Symbol	Parameters	Unit	Min	Typ.	Max
λ	Waveform length	nm		850	
P_{out}	Optical power	dBm	-7.0		-4.0

The G-link serializer HDMP-1022 generates a lot of heat. A fan is necessary to keep HDMP-1022 temperature lower than 50ºC.

B2. The LED function description

The board contains 11 LEDs. Their functions are defined in Table B4. Two green LEDs located at the side of the board indicate power supply and G-Link transmission lock. These two green LEDs should be lit during normal operation. Next to the transmission lock LED is a red LED used to indicate that the board has detected a parity error in the incoming data stream from the FEB. Typically, during FEB start-up procedure there will be some parity errors causing it to turn on. There are also 8 LEDs visible underneath the heat shield. The yellow LEDs are used to indicate that the board is receiving full frames from FEB correctly. There are also 4 red LEDs which function as the parity error counter.

Table B4. The LED function description

LED identification	Color	Function description
Power Supply	Green	On when the board are powered
Tx locked	Green	On when the G-link serializer gets locked on its input clock
Parity error	Red	On when a parity error is detected
LED0, LED1	Yellow	On = “1”. Lowest two binary bits of the count of the beginning of frames.
LED2, LED3	Yellow	On = “1”. Lowest two binary bits of the count of the end of frames
LED4~LED7	Red	On = “1”. LED4, LED5 and LED6 indicate the lowest 3 binary bits of the count of parity errors. LED7 indicates if the logic OR of all other bits

B3. The push button function description

The board contains 4 push buttons. Their functions are listed in Table B5. Only one push button (Reset) is used. Some parity errors may be detected during the FEB power-up. The parity error LED and LED0~LED7 may have to clear by pressing the

Reset push button. The Reset push button may also be pressed anytime during operation.

Table B5. The push button function description

Push button identification	Function description
Reset	Clear the parity error LED, and LED0~LED7
PB0~3	Not used

B4. The dipswitch function description

The board contains 8 dipswitches. Their functions are defined in the Table B6. Before installation, make sure dipswitches are set correctly. Currently only the default setting (DIV0 = 0, DIV1 = 0, and double frame mode) is supported.

Table B6. The dipswitch function description

Switch	Default	Meaning when ON	Meaning when OFF
SW0	OFF	The G-link serializer pin DIV0 = 1	DIV0=0
SW1	OFF	The G-link serializer pin DIV1 = 1	DIV1=1
SW2	ON	The G-link serializer is in double frame mode	Single frame mode
SW3~7	OFF	Not used	

Appendix C

The Simulation Board Data Sheet

C1. The board specifications

The Simulation Board works with single +5V power supply. The specifications for the power supply are listed in Table C1.

Table C1. The power supply specifications

Symbol	Parameters	Unit	Min	Typ.	Max
V_{CC}	Power supply voltage	V	4.5	5.0	5.5
I_{CC}*	Power supply current	A		1.11	

* Note: The E/O Transition Board is powered independently.

The trigger, the external synchronization and the external clock are recognized as LVTTL signals. Each of them is terminated with a 50-Ω resistor to reduce the possible reflection due to the media discontinuity. The input impedance is too heavy for the normal LVTTL gates to drive them. They have to be driven by the pulse sources with high current driving capability. Their specifications are listed in Table C2.

Table C2. The trigger, the external synchronization and external clock specifications

Symbol	Parameters	Unit	Min	Typ.	Max
V_{IH}	Input voltage to guarantee high	V	1.5		4.1
V_{IL}	Input voltage to guarantee low	V	-0.5		0.7
R_{IN}	Input impedance	Ω		50	
f_{clock}	External clock frequency	MHz	35	40.08	
η_{clock}	Clock duty cycle	%		50	
f_{sync}*	External clock frequency	MHz		80.16	
η_{sync}	Synchronous signal duty cycle	%		50	
$f_{trigger}$	Trigger signal frequency	kHz	0.001		200
$\eta_{trigger}$	Trigger signal duty cycle	%		50	

* Note: The synchronization signal from the crystal oscillator on board or an external pulse source should have the double frequency of the clock used in the transmitter side. The clock and the synchronization signal should not come from a same source (such as two outputs from a PLL).

The 32-bit data and two identical clocks are sent out through two 40-pin connectors. They are LVDS signals. Their specifications are listed in Table C3.

Table C3. The data and clock specifications

Symbol	Parameters	Unit	Min	Typ.	Max
V_{OD}	Differential output voltage (R_L=100Ω)	mV	250		550
V_{OS}	Output offset voltage (R_L=100Ω)	V	1.125	1.25	1.375
η_{clock}	Duty cycle of the clock	%		50	
$t_{valid\ before}$	Data valid before the clock rising edge	ns	4.0		
$t_{valid\ after}$	Data valid after the clock rising edge	ns	18.0		

The optical serial data input the board through a ST fiber connector. The optical signal specifications are listed in Table C4.

Table C4. The optical data specifications

Symbol	Parameters	Unit	Min	Typ.	Max
λ	Waveform length of the optical output	nm		850	
P_{IN}	Optical input power	dBm	-15		

The G-link deserializer HDMP-1024 is the most power consuming part on the simulation board. The part temperature should be kept at lower than 50ºC.

C2. The LED function description

The simulation board contains 10 LEDs. Their functions are defined in table C5. Two green LEDs indicate power supply and the G-Link receiving PLL locked. These two green LEDs should be lit during normal operation. 4 yellow LEDs indicate that the board is receiving full frames correctly. 4 red LEDs function as the parity error counter.

Table C5. The LED function definition

LED identification	Color	Function description
Power supply	Green	On when the board are powered
Rx ready	Green	On when the PLL inside the G-link deserializer locks onto the serial data
LED0, LED1	Yellow	On = “1”. Lowest two binary bits of the count of the beginning of frames.
LED2, LED3	Yellow	On = “1”. Lowest two binary bits of the count of the end of

		frames
LED4~LED7	Red	On = “1”. LED4, LED5 and LED6 indicate the lowest 3 binary bits of the count of parity errors. LED7 indicates if the logic OR of all other bits

C3. The push button function description

The board contains 4 push buttons. Their functions are defined in Table C6.

Table C6. The push button function definition

Push button identification	Function description
PB0	Clear LED0~LED7
PB1	Generate a bit error in the data transmitted
PB2	Reset the g-link deserializer Rx so that Rx starts a re-locking process.
PB3	Not used

The push button PB0 is used for system reset. When pressed, the frame count and the parity error count (indicated by LED0~LED7) are set to zero. The Reset push button may also be pressed anytime during operation.

The push button PB1 generates a bit error in the transmission data once it is pressed. It is used to verify the error detection function in the E/O transition Board and in the Simulation Board.

Once the push button PB2 is pressed, the G-link deserializer enforces to re-lock the input serial data. It is used to simulate a frame loss during the transmission.

C4. The dipswitch function description

The simulation board contains 8 dipswitches. Their functions are defined in Table C7.

Table C7. The dipswitch function definition

Dipswitch identification	Default setup	Meaning when ON	Meaning when OFF
SW0	OFF	The serializer pin DIV0 = 1	DIV0 = 0
SW1	OFF	The serializer pin DIV1 = 1	DIV1 = 1
SW2	ON	The Serializer works in double frame mode	In single frame mode
SW3	OFF	Use the clock and the	Input the clock and the

		synchronization signals on board	synchronization signal
SW4	OFF	Generate a bit error each 100 ms	Generate no bit error
SW5	OFF	Not used	Not used
SW6	OFF	Not used	Not used
SW7	OFF	Use the rising edge of StrbOut to sample the data	Use the falling edge

The dipswitches SW0~SW2 are used to set the G-link deserializer configuration modes. Currently, only DIV0 = 0, DIV1 = 0, and double frame mode are supported. The dipswitch SW3 selects the clock and the synchronization signal sources. The dipswitch SW4 works in the similar way to the push button PB1. It is used to verify the parity check function in the link. The dipswitch SW7 is used during the debugging procedure.