Beamtest results of ATLAS SCT Modules in 2002

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Abstract

Beamtests of ATLAS Semiconductor Tracker (SCT) modules carried out at the ATLAS testbeam facility at the CERN SPS H8. During 2002, three beam runs were carried out in May/June, July and August. In the August 2002 beam test period four irradiated modules, two "K5" end-cap and two barrel, with the final design were tested. Module propierties (efficiency, charge collection, signal/noise, pulse shape) and the dependence of them for a particle high incidence angle was studied. A comparison with previous testbeam results was also performed. Time-stamping performance of SCT modules and specially, the effect of irradiation on the time characteristics of the Front End was investigated more closely. On this note we show a summary of these studies.

1 Setup

In the 2002 a set of irradiated modules with the final design [1] were tested in H8 facility. Beam test setup at the H8 beamline at the CERN SPS was very similar to that described in [2] and [3]. A total of nine irradiated modules were present in August, most of them were also present in previous beam test the

same year. The irradiated modules were six barrel and three end-cap, marked with an asterisk (*). A hybrid module [1] and five non irradiated modules were used for comparison and check.

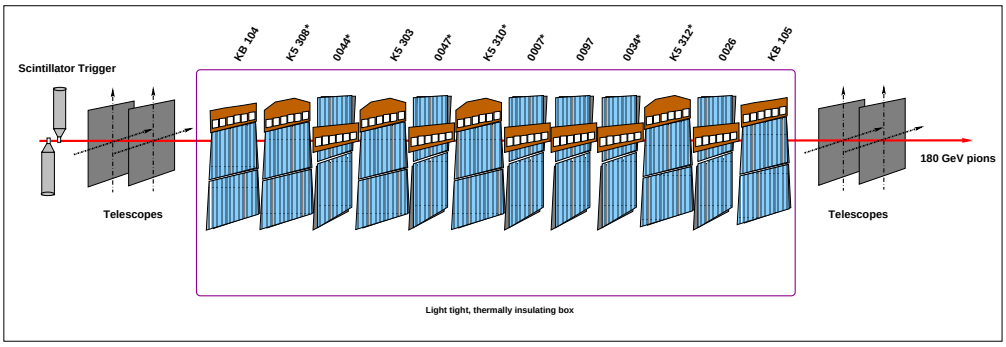


Fig. 1. Setup for the firsts runs of the August 2002 Test Beam.

Figure 1 shows a setup used with twelve modules (four K5 end-cap modules, two KBs and six Barrel modules). Three different studies were performed. The "standard" study in which efficiency, charge collection, signal/noise, pulse shape are evaluated for perpendicular incidence and various bias voltages. The behaviour of the prototypes using a beam with high incidence angle was checked and some runs with high incidence angle were taken. The LHC bunch crossing frequency of 40 MHz imposes severe requirements on the Front End electronics of the sub-detectors. The time-stamping performance of SCT modules has been measured in the laboratory (time walk) and the test beam (efficiency versus time). Here, an overview of the latter is presented.

2 Calibration

The modules calibration has been performed in-situ: as described in [10], to determine the front-end parameters as gain and noise, an internal calibration circuit that simulates a charge input is implemented in the ASICs. Figure 2 is the simplified representation of electronics of the chip.

A generated pulse goes through the calibration capacitor (Ccal) to the front-end electronics and the simulated charge is proportional to the height of the voltage step and the capacitance. Front-end parameters of the modules as gain and noise for each channel are measured by performing threshold scans for different input charges and for each channel of the chips. A complementary error function is fitted to each threshold scan to yield values of 50% point efficiency (vt_{50}) and output noise for each channel. A multi-parameter fit to a set of

[1] K5 315 is a module with an irradiated K5 hybrid and non irradiated sensors. This module will be marked with a dagger (†)

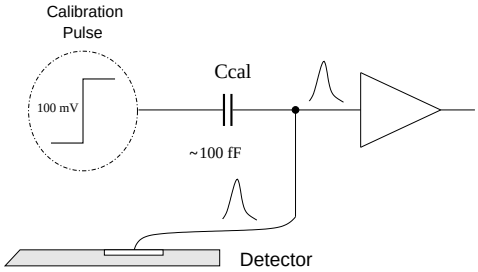


Fig. 2. Schematic representation of the chip read-out.

vt_{50} points is used to obtain the response curve from which gain and offset for each channel are determined. The input noise is thus calculated by dividing the output noise measured at 2fC by the gain. Before any response measurement a trimming procedure is performed in order to minimize the impact of the threshold non-uniformity across the channels on the noise occupancy. The ABCD3T design foresees the possibility to adjust the discriminator offsets channel-to-channel, thus allowing to improve the matching of the discriminator thresholds, which is an issue especially for irradiated modules, due to the increasing of threshold spread with radiation dose. Figure 3 on the right shows an example of irradiated barrel module tested injecting 1 fC through the calibration circuit: the spread of the distribution across the channels is of the order of 10% after the trimming procedure for irradiated prototypes, while it is around 1% for unirradiated prototypes (on the left).

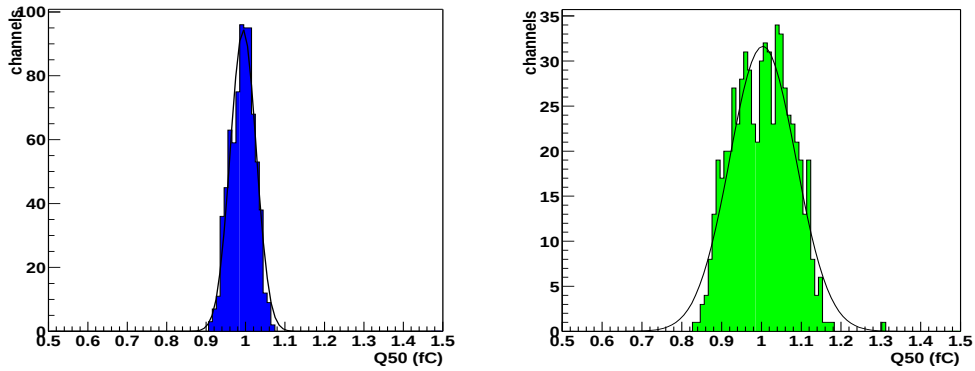


Fig. 3. 1 fC injected charge for one of the two sides of barrel module B097 non irradiated (on the left) and module B047 fully irradiated (on the right).

2.1 Further tests on irradiated modules

In addition to the standard electrical procedure described in [5] and here shortly summerize, a few more tests are required to optimize the working conditions of the ASICs for irradiated modules.

The front-end circuit for binary readout architecture is based on a transimpedance amplifier with a bipolar input transistor: for unirradiated ASICs, the nominal values for collector (preamplifier) and shaper currents are 220 μA and 30 μA respectively. As consequence of the β factor degradation, the optimum values of these currents decrease after irradiation; two 5-bit DAC's implemented on the ASICs permit to change the preamplifier and shaper currents[**?**] and the working point estimation is made checking different combinations of the two. Each chip can be independently adjusted and typical values found for K5 irradiated modules were 120 or 140 μA for the input transistor current, 27 or 30 μA for the shaper bias.

This procedure, the so called current scan, was made as a first step of the electrical tests and two different configuration were chosen; the first attempted to make chip working with maximal gain loosing slightly in noise performance, the second presented lower ENC noise level together with an average gain decreasement. On the other hand, the working range of modules in terms of possible preamplifier and shaper current is narrow so that different combinations result to not affect sensitivly signal and signal-to-noise ratio; thus, the configuration presenting lowest noise level has been chose for the most part of the test beam.

During previous tests, a degradation in timing performances of fully irradiated endcap modules has been observed. This can be correlated with the radiation effects in the digital part of the ABCD circuitry. Modifying the digital power supply V_{dd} thus didn't lead to any improvement; on the contrary, the high number of slow channels can be significantly reduced by increasing the analog voltage, V_{cc}, supplied to the chips.
In addition to reduce considerably the discriminator timewalk for many channels, operating the ASICs at $V_{cc} = 3.8$V instead of the nominal value also slightly improves the front-end parameters; in particular, the gain is in average 3 mV/fC higher and the noise occupancy slightly lower. It also allows to recover some channels, masked mainly because of the impossibility of being trimmed. The characterization *in-situ* has been done for fully irradiated module K5-308, keeping $V_{cc} = 3.5$V and $V_{cc} = 3.8$V. The time walk is displayed in figure 4: it shows a high number of channels with high timewalk (almost 200 channels out of the 1536 have a timewalk higher than 16 ns and among them 15 above 25ns) in case of nominal $V_{cc} = 3.5$V and the improvement increasing the analog voltage is clear in the comparison but for few channels.
Consistent results in term of pulse shape, signal and signal-to-noise comparison are presented in section 6

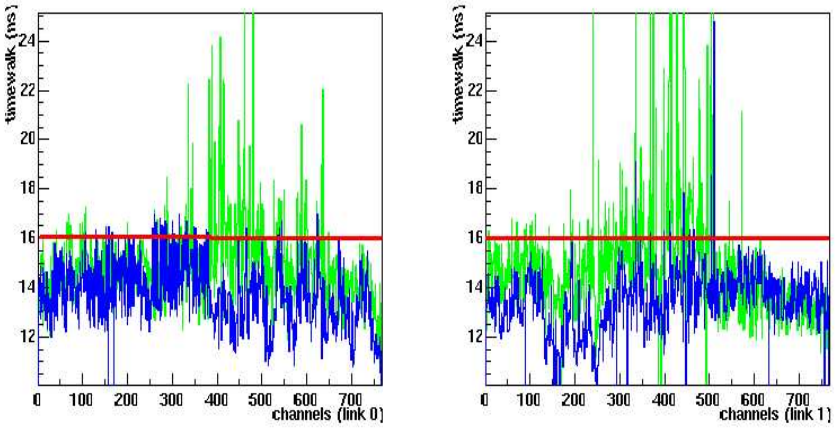


Fig. 4. Comparison of timewalk distributions across the channels (both sides) with Vcc 3.5 V (light line) and Vcc 3.8 V (dark line). The horizontal line corresponds to the specification requirement of 16 ns as maximal limit for tw.

2.2 Noise and gain correction and modules calibration results

Two types of corrections have to be taken into account to compare modules with each other for what concerns noise and gain.

First, the noise is dependent from the temperature as it has been measured in dedicated tests performed on single modules [5]: unirradiated modules show a correlation between the noise and the temperature of the thermistor placed on the hybrid, which can be fitted with a line of 5.8 $e^-/°C$ slope. For irradiated modules the results are affected by higher uncertainities: the study has been performed using a constant temperature of -7°C for the environment and the slope of a linear fit results in a temperature dependence of the noise around 24 $e^-/°C$. To compare results of different modules and to evaluate the expected signal-to-noise in the SCT, the noise values have to be normalized to a given temperature. Evaluations of the SCT cooling system have led to an expected temperature on the baseline module hybrid of about 2^oC so this is the chosen value. On the other hand, during the test beam, modules have been kept to a temperature within a range of 7-8 degrees, between -7^oC (irradiated barrel modules) and 0 ^oC (irradiated endcaps). Not normalizing to 2^oC, the signal-to-noise might be affect by a maximal error of the order of 5%.

As second correction to take in account, the amplitude of the calibration pulse issued by the ASICs needs a correction factor (referred below as "calibration factor"), that takes into account variations from the design value of the calibration capacitor on the front-end. To determine this variation, indirect measurements of this capacitance are performed by measuring the oxide thickness of the capacitor, and then by comparing it to the nominal value. In order to have realistic values for signal and noise, the calibration factor must be applied

to noise and gain as shown in Equation 1. The values of the individual Ccal correction factors are listed in table 1.

$$ENC_C = ENC \times Ccal \qquad Gain_C = Gain/Ccal \tag{1}$$

Table 1 shows the modules analyzed with the number of masked channels, online + (offline) used in the analysis. In the same table the chip-set type and the previous beam tests where the module was present is written. The results of the *in-situ* characterization, noise, in Equivalent Noise Charge (ENC), and gain for the irradiated end-caps and the new barrel modules are written in tables 2 and 3.

Module	*Chip set*	*Dose*	*Present @*	*Ccal*	*Masked* Channels
0044*	new epi	1	Oct 01	1.09	4 + (0)
0047*	new epi	1	Oct 01	1.09	7 + (4)
007*	old epi	1	July 02	1.09	Chip + 18 + (5)
034*	old epi	1	July 02	1.08	6 + (1)
096*	series	1		1.04	16 + (6)
USQ3*	new epi	1		1.15	24 + (4)
097	series	0		1.04	0 + (0)
K5 308*	new epi	0 / 1.1	May/July 02	1.10	5 + (1)
K5 310*	new epi	0.5		1.10	Chip + 59 + (0)
K5 312*	old epi	0.5		1.11	16 + (2)
K5 315†	new epi	hybrid		1.15	8 + (0)
K5 303	new epi	0	July 02	1.17	9 + (0)

Table 1
Ccal correction factors for the modules analyzed. Masked channels have been divided in online + offline analysis.

Chip	K5 308*		K5 310*		K5 312*		K5 315	
	ENC_C	$Gain_C$	ENC_C	$Gain_C$	ENC_C	$Gain_C$	ENC_C	$Gain_C$
M0	1992	38.0	2097	39.7	1780	38.5	1915	41.0
S1	2142	34.9	1796	42.4	1780	40.1	1862	42.3
S2	2144	32.0	1746	39.5	1775	40.3	1845	41.4
S3	1923	31.6	1748	40.9	1758	39.3	1942	40.0
S4	2090	34.9	1845	38.2	1816	38.7	2029	41.6
E5	2193	35.4	0	0.0	1716	33.7	1949	40.6
M8	2211	34.4	1736	41.2	1812	35.0	1948	41.3
S9	2081	34.6	1990	39.2	1794	40.0	1865	39.7
S10	2378	26.8	2011	35.4	1815	37.3	1865	39.7
S11	2463	27.7	1698	39.4	1772	37.7	1778	41.7
S12	2291	34.0	0	0.0	1759	38.1	1841	42.4
E13	2185	39.1	1922	40.2	1677	43.2	1800	43.0

Table 2
Corrected values of ENC_C (e^- ENC @ 2 fC) and $Gain_C$ (mV/fC) for the end-cap modules.

3 Analysis

For all of the modules a high statistics threshold scan at a bias voltage of 150 Volts for non-irradiated and 500 Volts for the irradiated was taken. Once the

Chip	097		096*		USQ3*	
	ENC_C	$Gain_C$	ENC_C	$Gain_C$	ENC_C	$Gain_C$
M0	1506	55.9	2146	36.4	1766	43.7
S1	1563	50.8	2137	36.9	2013	35.7
S2	1587	50.1	2136	35.5	2033	37.4
S3	1647	55.2	2296	31.2	1842	41.3
S4	1643	50.2	2290	33.8	1893	40.9
E5	1350	59.7	2346	31.9	2032	39.8
M8	1452	55.3	2278	32.0	2069	41.4
S9	1497	55.2	2464	33.7	2084	38.6
S10	1538	51.0	2415	33.6	1955	37.1
S11	1610	49.0	2304	32.7	2122	37.1
S12	1458	57.2	2243	35.5	2046	39.0
E13	1485	55.7	2313	34.8	1978	39.6

Table 3
Corrected values of ENC_C (e^- ENC @ 2 fC) and $Gain_C$ (mV/fC) for the barrels modules.

alignment of the modules is obtained one of the firsts results is the tracking efficiency for a certain discriminator threshold. With runs at different threshold the tracking efficiency dependence on threshold (fC), s-curve, can be studied. The s-curve is the integration of the charge distribution (Landau). The figures 5 and 6 are the s-curves for the irradiated end-caps, K5 310* and K5 312*, and the barrels 096* and USQ3*. With the binary readout the pulse height can not be extracted directly. The 50 % point corresponds to the median charge of the charge distribution [6], an example can be seen in figure 5 (left). The threshold values have been corrected by the calibration factor.

The region around the envisaged operating threshold is blown up in figures 7 and 8. In the same figure the noise occupancy corresponding to the same threshold is plotted. Noise occupancy is obtained during the time in between spills, with no beam on the modules. The efficiency and noise occupancy specifications are indicated as straight lines. The results are compared to those of other modules in this and previous test beams [3][4] in the tables at the end of the section (table 5 and 4).

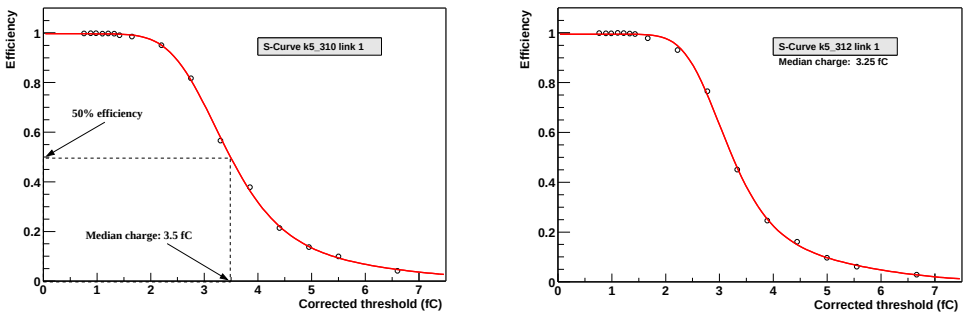


Fig. 5. S-curves of module K5 310* link 0 (left) and K5 312* link 1 (right). Response to perpendicularly incident tracks. Bias voltage of 500 Volts.

An estimate of the peaking time is obtained from a fit of the ABCD to the pulse shape reconstructed from the binary data and the trigger phase measurement.

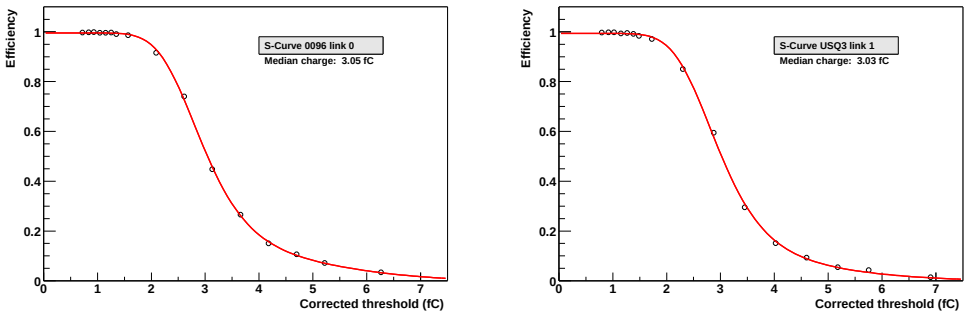


Fig. 6. S-curves of module 0097* link 0 (left) and USQ3* link 1(right). Response to perpendicularly incident tracks. Bias voltage of 500 Volts

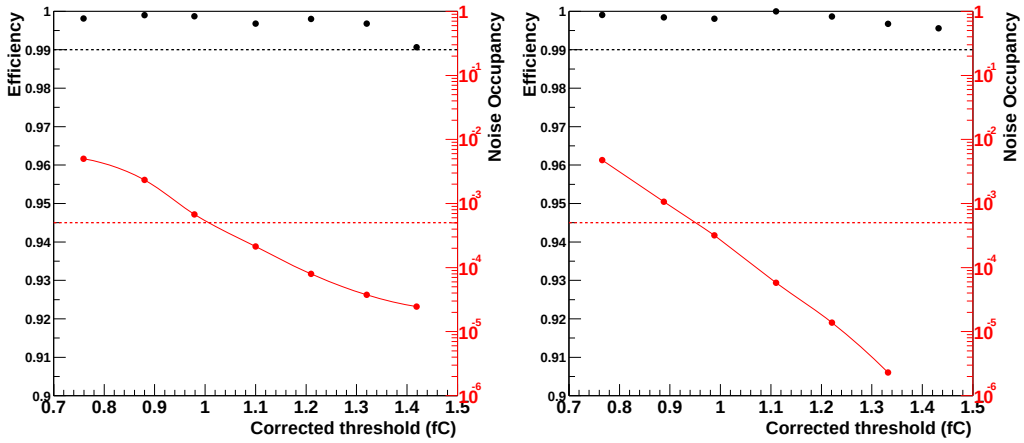


Fig. 7. Efficiency and noise occupancy of module K5 310* link 1 (left) and K5 312* link 1 (right). Response to perpendicularly incident tracks. Bias voltage of 500 Volts.

The fit assumes a $CR - RC^3$ transfer function[12] for the ABCD front-end. Figure 9 shows two different pulse shapes, a non-irradiated module on the left and an irradiated, right. The ABCD function, the continuous line, fits perfectly for the non-irradiated modules. The pulse of the irradiated modules is well fitted for the rising edge. But, the pulse is wider than the shape described by the function.

A summary of all the results is written in tables 4 and 5. The tables contains efficiency, occupancy, charge, peaking time measurements, bias voltage and the chips pointed by the beam on a set of modules. Table 4 lists the results from the reference threshold scan in the August 2002 beam test. Table 5 is a collection of the values from previous test beams. The August results are compatible within errors with the previous ones.

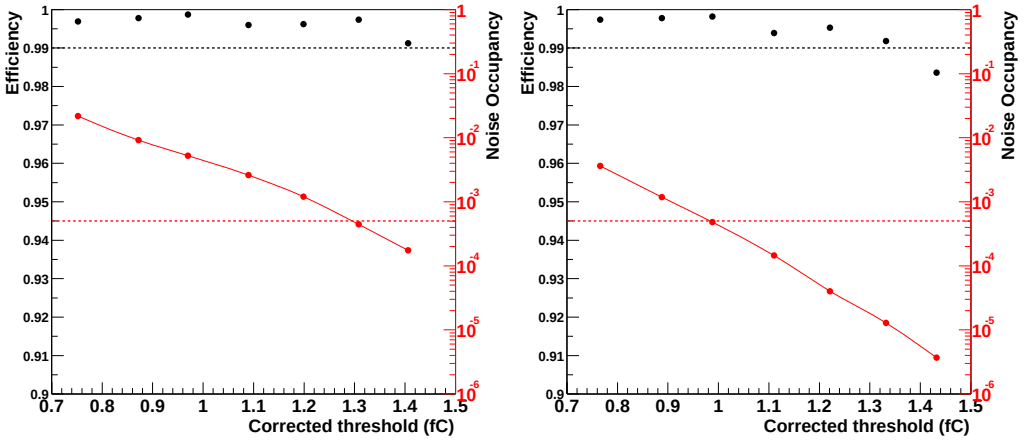


Fig. 8. Efficiency and noise occupancy of module 0096* link 0 (left) and USQ3* link 1 (right). Response to perpendicularly incident tracks. Bias voltage of 500 Volts.

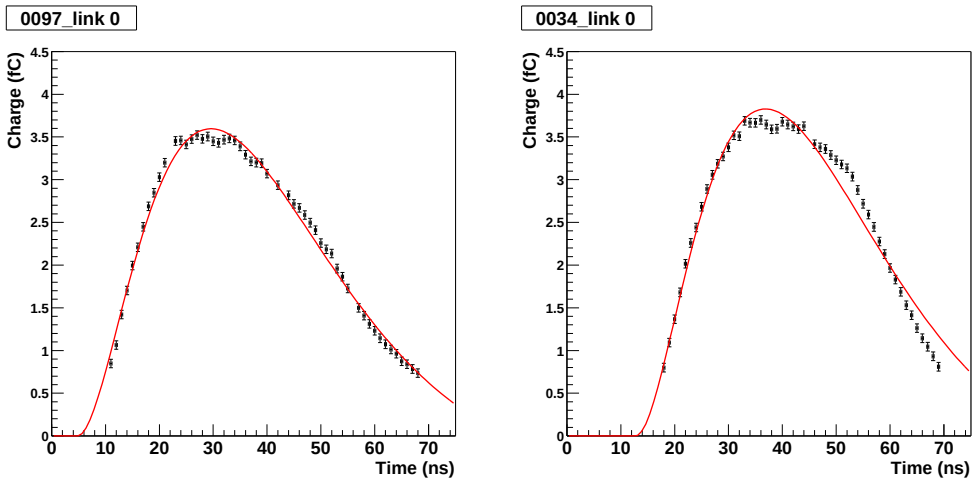


Fig. 9. Pulse shape of a non-irradiated module left and irradiated one right. The continuous line corresponds to the fit with the ABCD function.

4 Bias Scan

In the irradiated modules the collected charge is strongly dependent on the bias applied to the detectors. For the non-irradiated detectors a plateau is reached, collecting the full deposited charge a few tens of volts after depletion voltage. For irradiated detectors, the collected charge continues to increase, although slowly, even tens of volts after depletion.

In the beam test threshold scans at different bias were taken. For biasing the detectors a pad on the hybrid is used. In between the hybrid bias pad and the detector a resistance of 11 KΩ has been measured. In order to know the real voltage on the detector it is necessary to subtract the voltage drop in the

Module	*Eff* @ 1fC	*NO* @ 1fC	Q_{med} (fC)	*S/N*	*Pktime* (ns)	*Current* (μA)	*Bias* (V)	*Chips*
0047*	99.8	7×10^{-4}	3.2	9.7	23.2	1697	500	(S2)
	99.7	1.6×10^{-3}	3.0	9.8	27.6			(S11)
0044*	99.7	1.0×10^{-3}	3.3	10.0	22.2	1485	500	(S2)
	99.8	1.5×10^{-3}	3.1	9.9	22.1			(S11)
007*	99.7	1.9×10^{-3}	3.8	12.1	25.3	1348	500	(S2)
	99.9	2.3×10^{-3}	3.3	11.5	25.6			(S11)
034*	99.8	2.2×10^{-3}	3.5	10.7	24.1	1284	500	(S2)
	99.7	1.8×10^{-3}	3.4	10.8	23.8			(S11)
K5 308*	98.9	2.3×10^{-3}	2.4	7.8	26.8	1968	500	(S3)
	99.8	4.0×10^{-3}	3.0	7.9	24.9			(S10)
K5 303	99.8	1.4×10^{-4}	3.9	13.2	22.6	0	150	(S3)
	99.9	1.2×10^{-4}	3.6	12.8	22.2			(S9)
K5 310*	99.8	6×10^{-4}	3.1	11.0	24.3	950	500	(S3)
	99.8	7×10^{-4}	3.5	10.9	25.2			(S10)
K5 312*	99.8	4×10^{-4}	3.2	11.3	24.3	944	500	(S2)
	99.8	3×10^{-4}	3.3	11.6	24.7			(S11)
K5 315†	99.8	7×10^{-4}	3.6	12.2	24.2	0	150	(S2)
	99.8	6×10^{-4}	3.4	12.0	25.4			(S10,S11)
USQ3*	99.7	9×10^{-4}	3.1	9.5	22.9	2860	500	(S1,S2)
	99.8	5×10^{-4}	3.0	8.8	23.2			(S11)
096*	99.8	5×10^{-3}	3.0	8.8	24.5	3040	500	(S2)
	99.8	8×10^{-3}	3.2	8.7	24.3			(S11)
097	99.6	7×10^{-5}	3.3	13.2	25.3	0	150	(S2)
	99.7	9×10^{-5}	3.3	13.0	24.6			(S11)

Table 4
Summary of August 2002 results at perpendicular incidence, no magnetic field. The K5 315 is the hybrid module, irradiated hybrid and non irradiated sensors. The last column shows the chips pointed by the beam.

Module	*Eff (1fC)*	*NO (1fC)*	Q_{med} *(fC)*	*Pktime (ns)*	*Bias*	*Chips*
0047*	99.7	3×10^{-3}	3.1	23.4	350 V	??
				24.8		??
0044*	99.4	3×10^{-3}	3.1	23.2	350 V	??
				23.3		??
007*	99.6	1.7×10^{-3}	3.7	26.6	500 V	(S2,S3)
	99.7	2.4×10^{-3}	3.3	28.1		(S10,S11)
034*	99.7	1.5×10^{-3}	3.5	24.6	500 V	(S2,S3)
	99.7	1.2×10^{-3}	3.5	24.2		(S10,S11)
K5 308*	99.4	2.7×10^{-3}	2.7	25.3	500 V	(S2,S3)
	99.6	5.8×10^{-3}	3.1	25.7		(S10,S11)
K5 303	99.7	5×10^{-5}	3.8	23.2	150 V	(S2,S3)
	99.7	4×10^{-5}	3.5	22.7		(S9,S10)

Table 5
Summary of previous results at perpendicular incidence, no magnetic field. Efficiency and noise occupancy at 1 fC, median charge, peaking time, bias and chips in which the beam was pointing has been written.

resistance. Currents from 1 mA to 3 mA at 500 V lead to a voltage on the detector of 490 to 470 Volts.

The ratio of both numbers, median charge and noise, the S/N, is less sensitive to errors in calibration. Figures 10, 11 and 12 are some examples from the modules of the test beam.

The plots have been put into groups of similar types. Figure 10 shows two

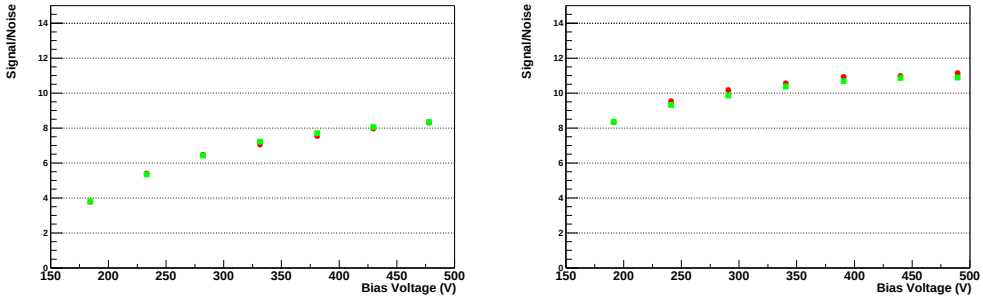


Fig. 10. Variation of the signal to noise ratio with detector voltage for two endcap modules, K5 308* (left) and K5 310* (right). Different markers distinguish different links (chips).

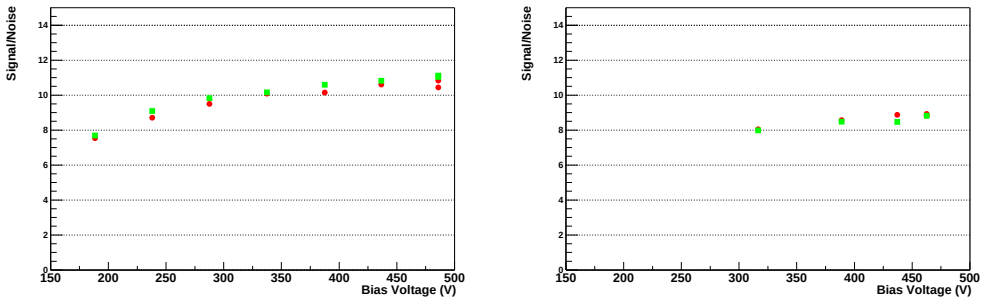


Fig. 11. Variation of the signal to noise ratio with detector voltage for two barrel modules, 0034* (left) and 0096* (right). Different markers distinguish different links (chips).

end-cap modules from two irradiation periods. Not only S/N value at 500 V is different (table 4), also the bias dependence. In figure 11 the 0034* and 0096* variation with bias is plotted.[2] The last two plots, figure 12, are S/N from a non-irradiated barrel and the end-cap hybrid, K5 315†.

5 Chip-to-Chip variation

In previous beam tests it was noticed that the behavior of chips of the same module is not the same. It was found that the median charge and S/N changes from one chip to another. The spread is larger after irradiation.

In order to quantify the deviation, scans at the same voltage, but with the beam pointing to different chips were taken. Figure 13 shows the values for charge and S/N across the module for the K5 308*.

[2] The annealing of the 0096* module finished close to the end of the beam test, and only four bias points were taken.

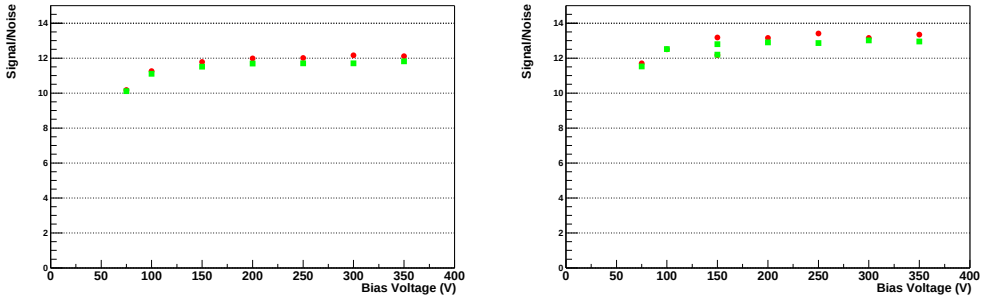


Fig. 12. Variation of the signal to noise ratio with detector voltage for two modules, hybrid K5 315† (left) and non irradiated 0097 (right). Different markers distinguish different links (chips).

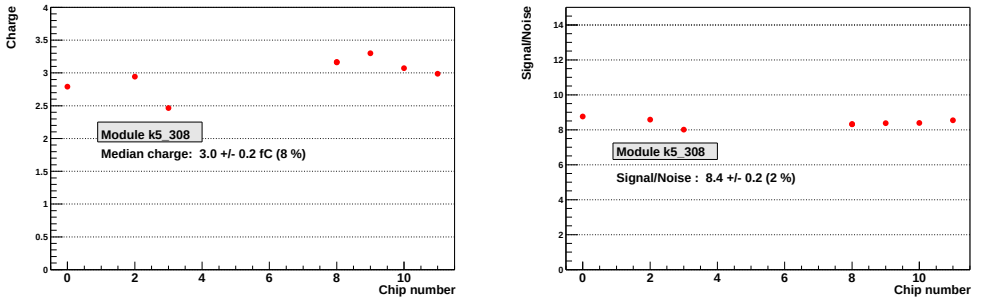


Fig. 13. Values of the charge in fC (left) and S/N (right) for the chips of the module K5 308* measured in the test beam.

Table 6 shows the mean value of median charge and S/N . The error in both cases is the standard deviation. The spread in observed charges in the irradiated modules is quite large. The error due to variations in the calibration of the chips is estimated to be around 0.2 fC (standard deviation). For the end-cap modules the variation in the S/N from different chips is smaller than the variation of either charge or noise. This reflects the cancellation of the absolute scale of the calibration [3] .

6 Front settings dependence

Different front end settings were probed in the irradiated end-cap modules to see the influence in the S/N value. As explained before, the β factor degradation after irradiation implies a decreasement of preamplifier and shaper current optimum values. The optimization is made trying to keep a low noise level and a reasonable high gain. It has been demonstrate that the ENC noise amount is more sensitive to the preamplifier current and it is lower at high current

[3] The barrel modules results are being investigated

Module	*Charge (fC)*		*S/N*	
0044*	3.32 ± 0.12	(3%)	10.8 ± 0.9	(8%)
0047*	3.2 ± 0.2	(6%)	10.2 ± 0.7	(6%)
007*	3.68 ± 0.17	(4%)	12.1 ± 0.8	(6%)
034*	3.51 ± 0.09	(2%)	10.8 ± 0.6	(5%)
097	3.19 ± 0.15	(4%)	12.9 ± 0.6	(4%)
K5 308*	3.0 ± 0.2	(8%)	8.4 ± 0.2	(2%)
K5 310*	3.3 ± 0.3	(8%)	11.2 ± 0.2	(2%)
K5 312*	3.21 ± 0.08	(2%)	11.4 ± 0.3	(2%)
K5 315†	3.6 ± 0.2	(5%)	11.8 ± 0.3	(2%)
K5 303	3.76 ± 0.11	(2%)	13.1 ± 0.3	(2%)

Table 6
Mean values for charge in fC and signal to noise ratio of the irradiated modules and the new barrel at 500 V. We have written the standard deviation and the equivalent percentage of the error

value, while the gain is mainly correlated to the shaper current.
Since the search of the working point is just an estimation made checking different combination of preamplifier and shaper current, it has been interest of the collaboration to quantify the influence of this on the signal to noise value and two possibilities were checked. One of the settings with a high pre-amplifier bias current (A) minimizes the noise, leading to a relatively low gain, since it has been necessary to compensate with a low shaper current. The second set with low pre-amplifier current (B) has a slightly higher gain, since it was possible to use higher shaper current values, at a moderate cost in noise. For each of the front-end settings the modules were calibrated. A table has been made with results for the different settings. The median charge of six chips is written in table 7. No change in the median charge is observed due to difference in the front-end settings. As expected, a difference in gain (in this case 3-4 mV/fC) does not affect the capability of charge collection, so the S/N ratio could be just increased if the noise is lower. In the measurements here reported, the improvement is not appreciable since the working range of modules, in term of preamplifier and shaper currents, is very narrow and the decreasment in terms of noise is of the order of 100 e- or less, within the error of the S/N itself.

A second comparison using different working parameters has been done for irradiated module k5-308: threshold scans have been performed using analog voltage Vcc at 3.5 (nominal) and 3.8 V (the two different calibration corresponds to config A and B respectively), where the latter value is preferable because of the general decreasement in number of masked channels and of improvement in timing performance. On the other hand, during the test beam only a particular chip on each side has been studied, and in this case the difference in term of collected charge is not appreciable, as reported in table 7. Still, the evidence of improvement in timing performance is visible in the pulse shape of figure 6.

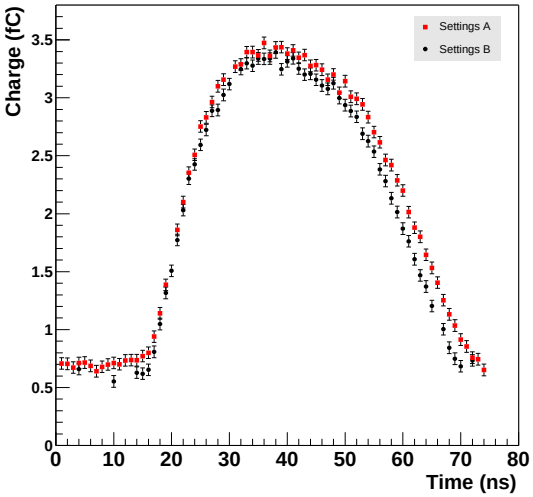


Fig. 14. Pulse shapes for the two front end settings *A and* B for the full dose irradiated endcap module K5 308.

7 High angle scan

During the August test beam, some measurements in addition to the main program have been performed, to check the behaviour of the prototypes using a beam with high incidence angle. Figure 15 shows the two possible cases that have been distinguished to evaluate effect of non-perpendicular tracks: in respect to a fixed beam direction, the first scenario *(a)* is equivalent to a rotation of the module onto the axis parallel to the strip direction; the second one *(b)* is equivalent to a rotation around an axis in the detector plane, but perpendicular to the readout strip. In the real experiment, case *(a)* will occur as an effect of the track curvature in the solenoidal magnetic field; moreover, the end-caps geometry of ATLAS will lead to incidence angles up to 34 degrees on the outer ring of the first disk, as in case *(b)*.

In both conditions, the path length through the silicon detector is longer than with perpendicular tracks and, in first approximation, the deposited charge increases linearly by a factor $1/\cos\alpha$. On the other hand, with a binary readout system, when a track crosses two or more strips, the released charge could

Module	*Chip*	*Settings*	
		A	B
K5 308*	S2	2.95	2.94
	S11	3.29	3.30
K5 310*	S2	3.08	3.05
	S3	3.13	3.16
	S10	3.62	3.59
K5 312*	S11	3.27	3.29

Table 7
Median charge values at a bias voltage of 500 Volts for the different front-end settings. *A* high pre-amplifier current and *B* low pre-amplifier current.

be deposited in neighbouring strips: already with perpendicular beam, a lack in efficiency in the middle inter-strip position of the track is measurable. The effect of charge sharing increases with non-perpendicular tracks, resulting as a significant loss of median charge: that has been measured in previous test beams, where incidence angle between 0 and 15 ^{o} have been used and the results, as reported in detail in [3], have showed a maximal decreasement in terms of collected charge of about 0.6 fC.
The narrow range of incidence angle previously tested was due to mechanical limits in the geometry of the main box where the modules are usually arranged. In the August 2002 test beam, an additional box have been used, in which few prototypes could be arranged in different positions. In particular two modules are considered in the following analysis, placed with the two explained orientations, using an incidence angle α of about 35: module kb-105 has been arranged as for case *(a)*, module B053 as for case *(b)*.

Figure 16 shows the residual distributions as measured for B053 (on the left) and KB-105 (on the right): in both case the residuals, calculated as the difference between where the track has crossed the centre of the silicon wafer and the centroid of the binary cluster, are wider than for the prototypes arranged in the main box. The track position is extrapolated by the telescope system, in this case placed far from the two under study modules, so that the effect of analog telescope modules resolution is not neglegible anymore. In particular, while charge sharing between neighbouring strips should have a slight beneficial effect on the spatial resolution in case *(a)*, KB-105, placed even further, presents a resolution of about 38μm (resulting from a gaussian fit), worse than B053 (σ $\simeq$30 μm). On the other hand, the measurement of efficiency and median charge are only slightly affected by the poor resolution, since it implies a lower number of good tracks, so a lower statistic.

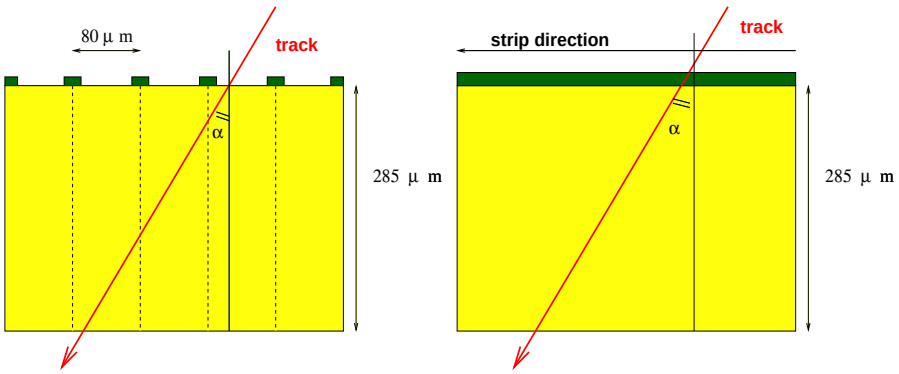


Fig. 15. On the left, case ***(a)***: the incidence angle α of the beam on the detector is equivalent to a rotation of the module onto the axis parallel to the strip direction, fixing the track direction. On the right, case ***(b)***: in a similar way, that is equivalent to a rotation of the module onto the axis parallel to the strip direction, respect to the track direction.

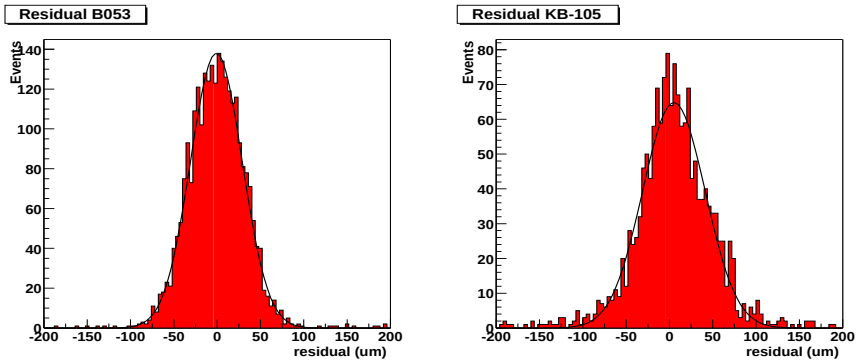


Fig. 16. Residuals measured @ 1 fC: due to the long distance between the modules and the telescope system, the reconstructed tracks compared to the hit position of the modules have a poor resolution and the obtained residuals are wide. On the left, B053 and on the right KB-105, both @ 1fC threshold and with nominal bias 150 V.

Module	*Qmed @ 0°* *Bias=150V*	*Qmed @ 35°* *Bias=150V*	*Qmed @ 0°* *Bias=350V*	*Qmed @ 35°* *Bias=350V*	*Res.*	*Clus.* *@1fC*
B053	3.29	4.02	3.45	4.34	29.8	1.2
KB-105	3.30	1.65	3.40	2.05	37.5	1.42

Table 8
Median charge for perpendicular tracks and for incidence angle α of 35^o at 150 V and 350 V. Residuals and cluster size @ 1 fC are also reported: no difference is notable between the two different bias voltage.

Table 8 shows a comparison between median charge measured at 150 V and 350 V of bias voltage, with perpendicular beam and with track having incidence angle 35^o. Residuals and average cluster size are also reported.

- **case *a***: the median charge of module KB-105 (s-curves at 150 V and 350 V reported in figure 17), is much lower than what it has been measured with perpendicular track. The effect of charge sharing is significatly high and it translates in a lack of efficiency and consequently of collected charge, that could be compared with what had been measured in previous test beams with incidence angle α between -14^o and +16^o. Circle points of figure 18 show the correlation between median charge and incidence angle α for barrel module B018 as measured in 2001 test beam (see [3]): adding the KB-105 measurement (last point, squared),and extrapolating the curve, Q is low as expected; an uncertanity of about 10% has to be considered on the KB-105 median charge value because of the low statistic. No normalization has been applied, since the median charge with perpendicular beam is the same ($Qmed$=3.3 fC) for both barrel and KB module.
- **case *b***: as mentioned above, the end-caps geometry of ATLAS will lead to incidence angles up to 34 degrees on the outer ring of the first disk. The median charge of module B053 is as high as expected, with an increasement by a factor 1/cosα respect to the perpendicular charge Q(α=0). Figure 19 shows the correlation between median charge and incidence angle for module B029 as measured in 2001 test beam in addition to the point refered to

B053, fitted with function $1/\cos\alpha$. The median charge is normalized to the value found in perpendicular scan, 3.19 fC for B029 and 3.29 fC for B053 respectively.
Moreover, the measured median charge with a bias voltage of 350 V is 4.34 ± 0.15 fC, to be compared to the expected one 4.20 ± 0.18 fC, where the uncertainity is dominated by the error of $\pm3^o$ on the incidence angle.

8 Timing of SCT modules

The bunch crossing frequency of the LHC is 40 MHz: the Front End electronics has a very limited time to process a signal and be ready for the next. It is especially important to correctly time-stamp the hits: a hit that is tagged in the wrong bunch crossing leads to a loss of efficiency and it results in an uncorrelated (ghost) hit in the subsequent bunch crossing.

In view of the above arguments a short integration time would be preferable. Robustness against ballistic deficit and the requirement of low noise on the other hand require a longer integration time. The design value for the ABCD of 20 ns is a compromise between both arguments. A special edge sensing circuit in the discriminator makes it more sensitive to timing. The circuit issues a 25 ns high when a low-to-high transient is detected. Thus, only one "1" is written into the pipe-line even though the signal remains higher than the threshold for a longer time.

Two types of measurements have been performed routinely:

- the characterization of the module includes the determination of the time-

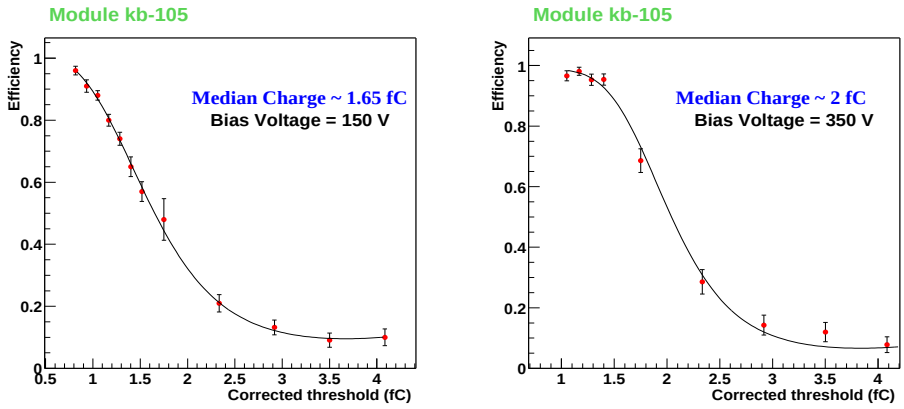


Fig. 17. Efficiency s-curve for unirradiated module kb-105, placed with an incidence angle of $\alpha=(35^o\pm3^o)$ equivalent to a rotation of the module onto the axis perpendicular to the strip direction respect to the beam direction. The left plot refers to 150 V nominal bias, the right one reports s-curve with module biased at 350V.

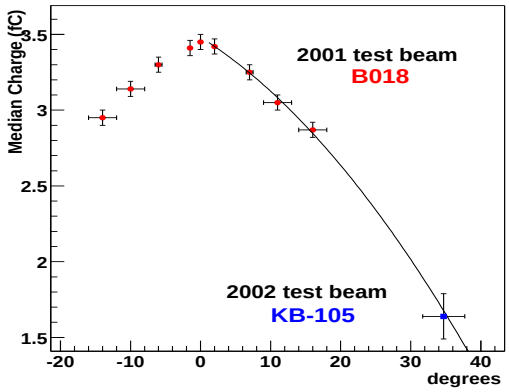


Fig. 18. Correlation between median charge and incidence angle of the beam: the red circle refers to module B018 as measured in 2001 test beam, the blue squared correspond to KB-105 resulting from the high angle scan performed in 2002. The parabolic fit shows that the median charge is low as expected. Modules have been biased at 150 V and charge was corrected with appropriate calibration factor.

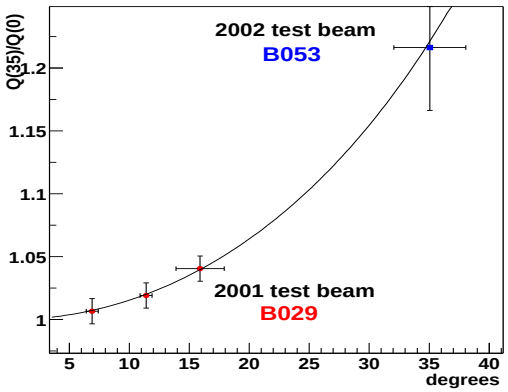


Fig. 19. Q(α=35^o)/Q(α=0^o) versus incidence angle: the latest point at 35^o results from the 2002 test beam, while the other measurements refer to barrel module B029 measured in 2001. The plot is fitted with the function 1/cosα as expected from theory.

walk using the pulses injected by the calibration circuit.

- In beam tests the shape of the pulse resulting from the shaping of the detector signal has been reconstructed for different detector bias voltages [4].

Comparison of both types of measurements shows a clear correlation between the peaking time as measured in the beam test and the time walk measurement, provided the detector bias voltage is high.

[4] The pulse shape reconstruction method was developed during the beam test at KEK in December 2000 and was published in [8,7]

Peaking times measured on non-irradiated modules vary in the range 19-22 ns. Indications of a dependence on the chip was seen in [3] [5] . Statistics on these measurements are quite low: only two different batches were investigated. The availability of production chips allows to contrast these findings with a third sample.

It is known that the timing characteristics of the Front End change when the modules are irradiated. The peaking time was measured to increase by 2-5 ns [8,7,3]. It is not clear at this point whether the longer peaking times initially observed on (K3) end-cap modules are a temperature effect or intrinsic to the end-tap readout. Some more recent measurements are discussed in this note.

Timing effects have been studied in detail in a test beam with a 25 ns bunch structure in October 2001 ([4]).

8.1 Test beam measurements

In standard test beam operation in the H8 test area in the CERN SPS the beam and the readout clock are not synchronized: particles arrive with a random phase in the 25 ns clock interval. This phase is measured with a 0.2 ns resolution TDC as the delay between the discriminated signal from the scintillator trigger and the next rising edge of the readout clock.

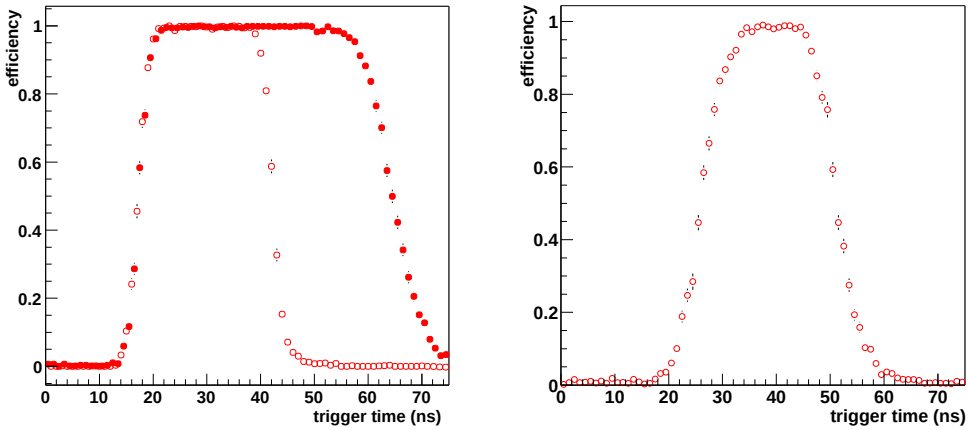
On receipt of a L1 trigger the ABCD chips provide the binary hit information from the triggered clock cycle and the previous and next clock cycles. This three bit code is known as the hit pattern. In the test beam modules are readout in ANYHIT compression mode: the binary information is made available for all channels that had a "1" in at least one of the three clock cycles. Offline, the hit patterns and TDC information are combined to calculate the efficiency for each time bin. a cut is placed on the TDC value to select a narrow window where the efficiency is optimum. This is equivalent to running in LEVEL compression mode.

Details of the timing performance can be studied by plotting the efficiency versus time [6] . These figures can reveal timing effects due to:

- the edge sensing circuit
- the radiation damage of sensors and FE electronics
- the detector bias voltage

[5] The chips from the new-epi batch were found to be significantly faster than those from the old-epi batch

[6] One can even go further and reconstruct the complete S-curve for small time intervals and thus statistically reconstruct the pulse shape of the shaper amplifier [8,7]



(a) (b)

Fig. 20. Module efficiency versus arrival time of the particle. Leftmost figure: a non-irradiated end-cap module at a detector bias is 250 Volts and a discriminator threshold 1 fC. The discriminator is operated in level sensing (filled circles) and edge sensing mode (open circles). Rightmost figure: an irradiated end-cap module. The bias discriminator threshold is set to $V_{bias} = 450\ V$ and $Q_{thr} = 1\ fC$.

Figure 20(a) shows the efficiency dependence on the arrival time of the particle. The effect of the edge sensing circuit becomes clear: the range where the module is efficient is limited to 25 ns. Virtually no hits related to the track are found in the clock cycle subsequent to the maximum.

Efficiency versus time distributions like those in figures 20(a) have been reconstructed for a large number of modules and a range of bias voltages from data taken in the 2002 beam periods. To allow a quantitative comparison of the results a number of observables are defined here. The time corresponding to the rising and falling edge is fitted as the 50 % efficiency point on both sides of the distributions 20(b). The average of both values defines the center of the distribution t_c. Assuming the clock and trigger jitter in ATLAS to be of the order of 1 ns the efficiency for optimal timing is determined as the average in a window $[t_c - 1.5, t_c + 1.5]$. The probability of a ghost hit in the subsequent bunch crossing is the "efficiency" in a similar window centered on $t_c + 25$. The optimization of the timing relies on similarity of the response of all chips on the module. The difference between the rising edge of the two chips, Δt_0, is listed as well. The width of the distribution - the difference between the times corresponding to rising and falling edge - is found to be 25.1 ± 0.1 ns for all modules [7]. As no systematic differences are observed between modules, this

[7] Measured at 1.2 fC. At 1.0 fC the distribution is slightly wider 25.3 ± 0.1

Module	*Dose*	eff_{max} *(%)*	*P(ghost) (%)*	$\Delta t_0 (ns)$
K5 312	0.5	99.6	0.8	1.8
K5 310	0.5	99.3	0.9	3.5
K5 312	0	99.7	0.2	0.2
K5 310	0	99.6	0.4	1.2
K5 315	hybrid	99.3	1.1	0.1
K5 305	1.1	97.4	5.9	0.0
K5 308	1.1	98.9	2.9	2.6
K5 308 3.8 V	1.1	98.8	2.0	0.9
K5 308 3.8 V, 1.2 fC	1	98.9	1.2	0.9
0097	0	99.4	1.2	0.1
0044	1	99.2	1.4	2.8
0047	1	99.0	0.9	2.5
0007	1	99.2	1.6	0.1
0034	1	99.3	1.3	1.6

Table 9
Measurements of the timing performance in the May and August beam tests. Unless otherwise specified the discriminator threshold is set to 1 fC and the detector bias voltage is 150 Volts for non-irradiated modules and 450 Volts (May) or 500 Volts (August) for irradiated modules. The best guess for the dose to which the modules were irradiated is specified (in units of $3 \cdot 10^{14} p/cm^2$) in the second column.

observable is not listed in the table.

The performance of the two irradiated K5 modules in the May test beam is clearly worse than what is obtained on irradiated barrel modules. The same module K5 308 operated with an analog supply voltage to the chips of 3.8 Volts shows a slightly improved performance. The ghost hit probability is reduced rather efficiently by raising the threshold: at 1.2 fC all modules except K5 305 show a probability to produce a ghost hit close to or below 1 %, while still maintaining an efficiency compatible with 99 %.

For irradiated modules the average time difference between the rising edges of two randomly chosen chips on the front and back of the module is 2 ± 1 ns. Non-irradiated modules show much smaller differences in timing: 0.4 ± 0.3 ns.

We can try to evaluate the effects of timing differences between chips or channels in a module. Deviations in time of channels (chips) can be simulated with a movement on the TDC window used for the analysis. Figure 21 shows the loss in median charge observed with the variation of the position of the window. The loss is refered to the maximum median charge value. The small points are the individual measurements. For each time the values for all the chips are shown. Markers joined by a line are the average of the values, irradiated modules the dark markers and non-irradiated the empty ones. A different shape can be seen looking to the different curves. Examples of losses and deviations ($\Delta\tau$) values are listed in table 10.

$\Delta\tau$ (ns)	Non - Irrad	Irrad
+ 5	4 %	6-7 %
- 5	3-4 %	2 %
+ 10	22 %	35 %
- 10	8 %	8-9 %

Table 10
Percentage of charge loss for a selected values of delay for irradiated and non irradiated modules.

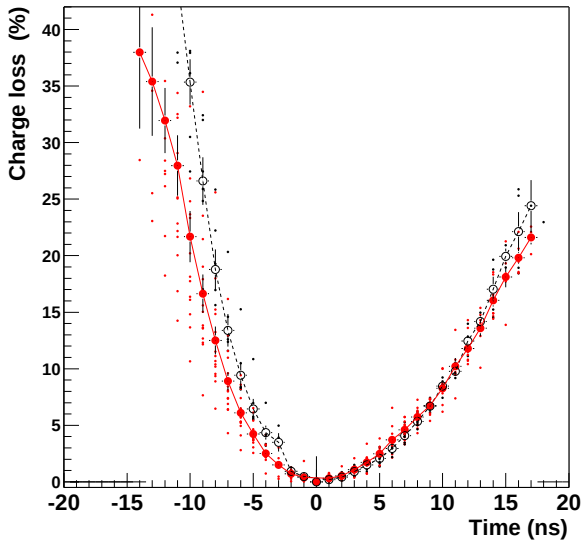


Fig. 21. Loss in the the median charge observed (in %) versus the time variation. Time zero is the point for which the median charge is maximum. Markers joined by a line are the average of the values, irradiated modules the dark markers and non-irradiated the empty ones.

9 Conclusions

Modules from all geometries with different fluences have been tested. A clear dependence on the fluence has been seen. For the full dose the operating margin (efficiency $> 99\%$ and N.O. $< 4 \cdot 10^{-5}$) exists but becomes narrower. The operating margin appears (depending on the module) with a bigger than the nominal.

The study of the different set of front settings showed that a difference in gain (3-4 mV/fC) does not affect the charge collection. To increase the S/N ratio the set with small noise can be used, also an slight improvement in timing performance is seen for these settings.

Beam test runs with the edge sensing circuit of the ABCD Front End chips allow a study of the timing performance of the Front End. Results have been presented on a number of modules of different geometries, different irradiation histories and running with different operating parameters (bias voltage,

discriminator threshold, analog supply voltage).

Generally, the irradiated modules maintain a high tracking efficiency of over 99 % and a ghost hit probability below 1 %. The exception is formed by two irradiated K5 modules when running with nominal analog supply and threshold. An increase of the supply voltage and the threshold to $V_{cc} = 3.8$ V and $Q_{thr} = 1.0$ fC.

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