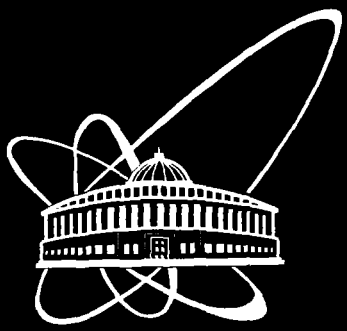

ОБЪЕДИНЕННЫЙ
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ANODE AND CATHODE READOUT ELECTRONICS FOR CYLINDRICAL MULTIWIRE PROPORTIONAL CHAMBERS OF THE **PIBETA** DETECTOR

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Introduction

The PIBETA detector is currently used at PSI (Switzerland) for experimental investigations of rare pion and muon decays. The goal of the first stage of this experiment is to improve the accuracy of measuring the probability of the pion beta decay ($\pi^+ \to \pi^0 + e + \nu$) from currently 4% to about 0.5%.

The experimental setup is shown schematically in Fig. 1.

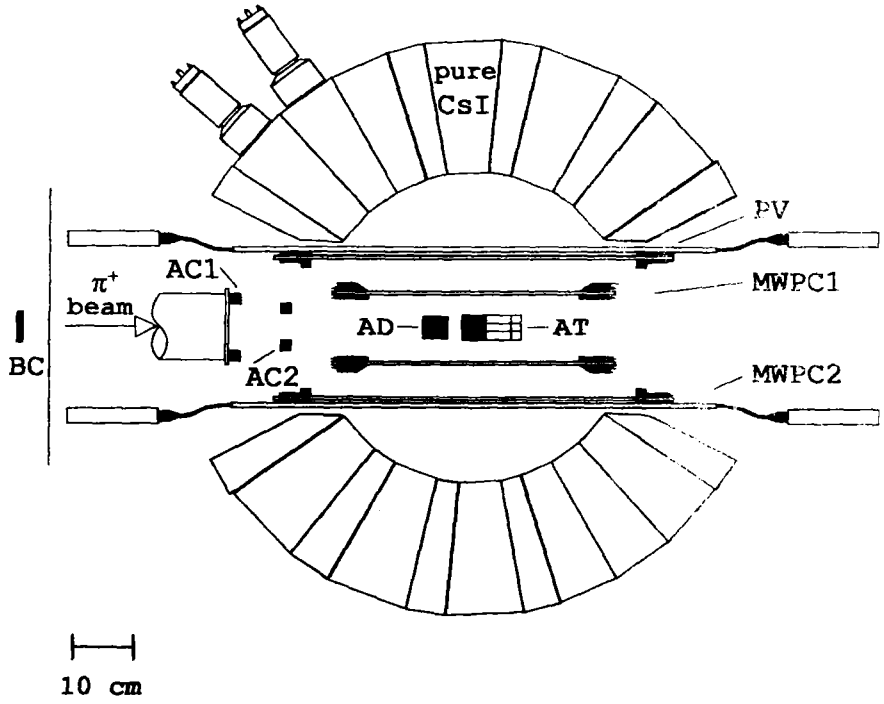

Fig.1. Schematic depiction of the PIBETA detector:
AT - Active Target; AD – Active Degrader; AC1, AC2 – Active Collimators; MWPC1, MWPC2 - Multiwire Proportional Chambers; PV – Plastic Veto; BC - Beam Counters

1. Design and Parameters of the CMPC

A general description of the design and operation of CMPCs can be found in [1]. The chambers are independent self-supporting two-coordinate detectors. The azimuthal coordinate is determined from the triggered wires located along the cylinder axis. The event coordinate along the cylinder axis is determined from the analysis of the induced signals on a cathode split up into separate strips.

Positive high voltage is supplied to the CMPC anode wires. The chamber wires are combined into groups of 32 wires. All wires in each group are connected to each other by resistors of 0.5 MOhm. The high voltage is fed through a resistor of 20 MOhm to the first and the last wire in each group. This arrangement of wire groups allows the independent setting (or changing) of the high voltage for different zones of a chamber. The signals from the anode wires are read out via high-voltage blocking capacitors of 500 pF. All cathode strips are connected to the ground through resistors of 0.8 MOhm, so the cathode surfaces have a zero potential.

It should be noted that the PIBETA detector's design makes it impossible to place the anode and cathode electronics directly on the chambers. Therefore the anode and cathode signals are transmitted from the detector to the readout electronics via 1.5 m long 50 Ohm coaxial cables.

2. Cathode Electronics

The cathode strip signals are amplified, delayed and then digitized in a LeCroy 1882F FASTBUS analog-to-digital converter (ADC) . The amplifier modules are placed outside the chambers and connected to the strip signal connectors via the 50 Ohm coaxial cable of 1.5 m length. To compensate a latency of a setup trigger system, the amplifier outputs are connected to the ADC inputs via the 200 ns delay cables.

The amplifier described below is intended to amplify the positive current pulses from the cathode strips of proportional chambers and drive the 50 Ohm coaxial cable. The amplifier gain and the output voltage swing are matched for operation with the 1882F.

The amplifier (Fig.2) consists of protection circuit (BAV99) followed by two amplifier stages. The test charge is injected through a 1 pF capacitor C1. Both stages are built on bipolar transistors BRF93A and BFT92 from PHILIPS. The first stage provides a 50 Ohm input impedance and current to voltage gain of 3.9mV/μA. The resistor value R1=1.6 kOhm is chosen to set an optimal collector current of the input transistor to minimize an equivalent noise charge (ENC). The second stage has a 4 Ohm output impedance and voltage gain of 6.4 mV/mV. Taking into account a high open-loop gain, the feedback amplifier gain can be written as Rf1*Rf2/Re. To minimize the module dimension and crosstalks, each amplifier is placed on separate two-layers printed board.

Each amplifier module consists of 32 amplifiers which are plugged to the motherboard and a test pulse generator. The amplifier modules are housed in dedicated crates (up to 24 modules per crate). To reduce an external pickup noise the crates are powered from linear voltage regulators.

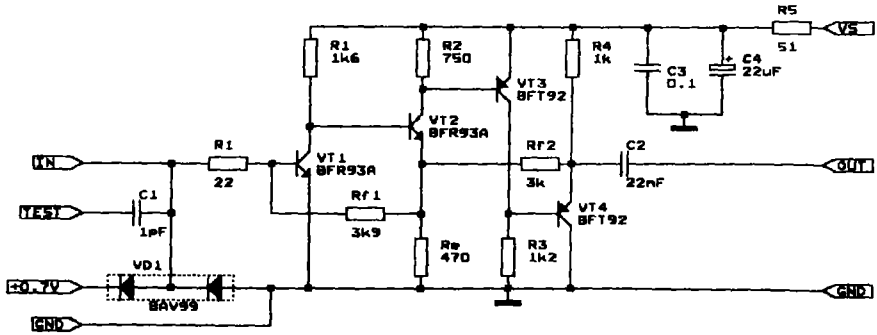

Fig.2. The cathode amplifier circuit

The module specification: number of channels – 32; input pulse polarity – positive; input impedance - 50 Ohm; Gain - 25 mV/μA; gain stability (Vs=6V ±10%) - ±0.5%; output impedance - 4 Ohm: output negative voltage swing (R1=50 Ohm) - 1V; ENC, r.m.s. - 3300e + 14 e/pF; integral linearity (R1=50 Ohm) - ±0.3%; rise and fall time -14ns; crosstalks (charge measurement mode) - ±0.1%; power requirement - Vs=+6V at 320mA.

The test results of the amplifier module are described in [2].

3. Anode Electronics

A new readout system for the anode wires of proportional chambers have been developed in CAMAC standard as a replacement for the LeCroy PCOS III system used before. The new system is much more compact, better interference proof and relatively inexpensive than the old one. The whole system for 576 input channels fits in one CAMAC crate. The basic component of the system is a 32-channel single width CAMAC module. Below is given the brief description of the module operation based on its block diagram shown in Fig. 3. The signals arrive at two 16-pin connectors of the ADD-32 unit. Next, they are amplified by four Ampl 8.3 8-channel amplifiers [3,4] and arrive at 4-input MAX978 comparators (8 pcs). The thresholds for these two comparator groups are set by program and produced by the doubled AD7302 digital-to-analog converter (DAC). The signals converted by the comparators to the TTL level arrive at inputs of IDT72421 FIFO microcircuits (4 pcs, each with 9 inputs, one of them is not used).

By leading edges of clock pulses (50 MHz) arriving from the generator the data signals are written into the internal FIFO memory array constructed in an 8x64 circuit. The supply of the clock pulses and, hence, their writing into the memory array is triggered by command from the CAMAC bus.

The Trigger signal stops the data writing. Then, the logical summation is performed at given memory locations. This is done by EPM3032A

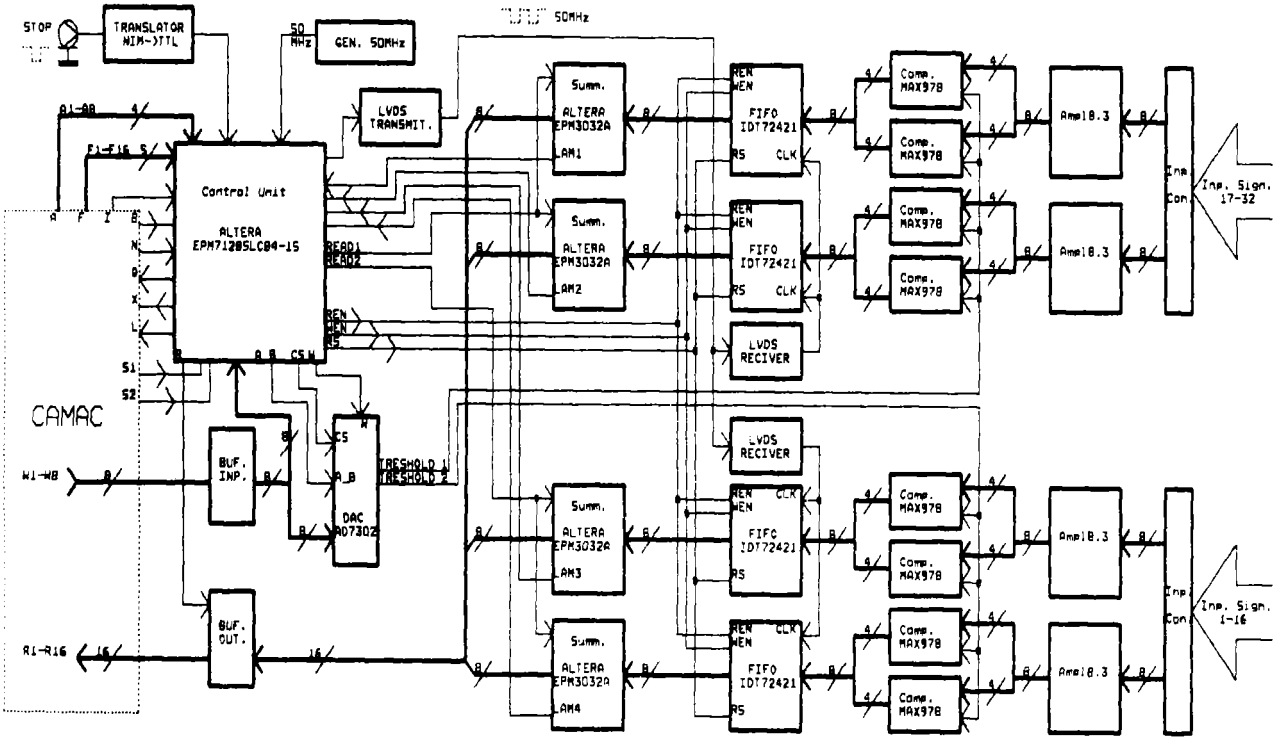

Fig.3. Block diagram of the ADD – 32 unit

programmable microcircuits (ALTERA) into which the data from the FIFO are automatically sent with the arrival of the Trigger signal.

Upon the completion of the logical summation procedure and in case of the available useful data, the adders send request signals LAM1-LAM4 to the control circuit constructed with the EPM7128LC84-15 programmable microcircuit (ALTERA), which, based on these signals, produces a common for the whole module LAM signal.

The adder outputs with Z-status are connected to a 16-bit bus by means of which the data via buffer circuits is read out into the CAMAC controller. The data is read for two module address cycles. The low voltage differential signaling (LVDS) transmitter and receivers are used for transportation of 50-MHz clock pulses within the PCB to decrease noises.

The characteristics of the Ampl 8.3 current amplifier are as follows: conversion factor is 140 mV/μA (70 mV/μA per arm); at Cin.det. = 0 pF the noise current 56 nA, at Cin = 60 pF it is 110 nA; rise time of the output signal is 8 ns; polarity of the input signal ±; input impedance 50 Ohm; protection against positive and negative voltage surges at the input; channel number is 8; dynamic range is 60 dB; differential output; output load 1 kOhm; supply voltage is ±5 V; power consumption is 75 mW/channel; case type is plastic, 48-output, 4222.48 GOST17476-88.

Figure 4 demonstrates a block diagram of the one channel of the ADD-32 unit which consists of the Ampl 8.3 amplifier, MAX978 comparator, and input section of IDT72421 FIFO microcircuit.

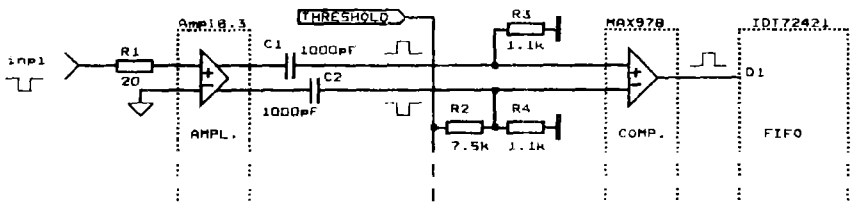

Fig. 4. Block diagram of one channel of the input section of the ADD-32 unit

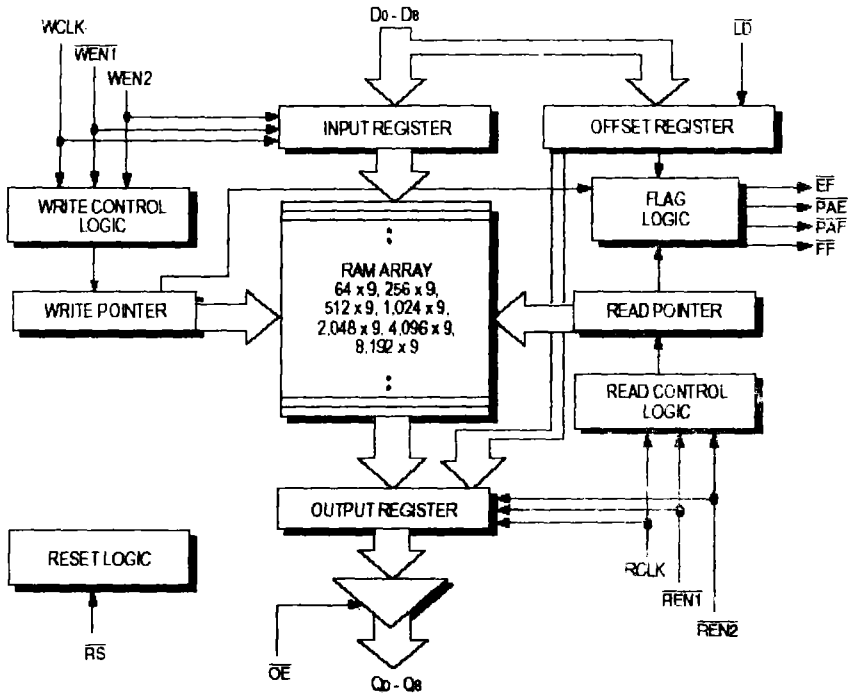

Fig. 5. Block diagram of the internal structure of IDT72421 FIFO microcircuit

If the operation of the amplifier and comparator circuits is quite understandable from Fig. 4, the operation of the FIFO microcircuit requires some explanation. Figure 5 shows the internal structure of the IDT72421 FIFO microcircuit.

The IDT72421 microcircuit has 9-bit input and output ports, which are controlled by WCLK, $\overline{\text{WEN1}}$, WEN2 (hereinafter referred as WEN) and RCLK, $\overline{\text{REN1}}$, $\overline{\text{REN2}}$ (hereinafter referred as REN) signals, respectively. The WEN signal enables the writing into the input port by the positive WCLK leading edge. In this case, the data is written into the current location of the FIFO memory array; after that the write pointer (WRITE POINTER) shifts by one step.

The REN signal enables the reading, and the contents of 9-bit FIFO location, at which at the moment the READER POINTER is set, is written into the output port, and with the enabling signal $\overline{OE}$ appears at outputs Q1-Q9. In this case, the read pointer shifts by one step. The WCLK and RCLK outputs can be connected. Then, write and read operations will be performed simultaneously. The $\overline{RS}$ signal serves for the FIFO circuit reset; when it is applied, the write and read pointers are set at the first FIFO location.

The system based on the FIFO circuit operates as follows. Initially, when the $\overline{RS}$ signal is applied (remind you that in this case the read and write pointers are set at the first FIFO location), the program shifts the write pointer by the location number corresponding to the trigger delay expressed in generator time steps. For example, if the trigger delay is 300 ns, at 50-MHz operating frequency (T = 20 ns) the write pointer should be shifted with respect to the read pointer by 15 locations. The write pointer is shifted by applying a given number of pulses at WCLK with the enabling level at WEN. If WCLK and RCLK inputs are connected (we designate this status as CLK) then, it is necessary to set additionally the disabling level at the REN input to prevent the read pointer shift. Now, if to apply a clock frequency from the generator at the CLK input with the enabling REN and WEN signals, the data from the FIFO input will be continuously written into locations, shifted and 15 time steps (300 ns) later appear at the output. The Trigger signal arrival stops the clock signal supply. At the moment, the useful data is at the FIFO output. By applying the clock pulses to the CLK input by program, it is possible to read the FIFO contents at a selected depth.

If the read pointer were set in accordance with a delay in the Trigger signal arrival, the schematic representation of the FIFO memory contents would have looked like in Fig. 6. It can be seen that the useful data are located in a comparatively narrow address space whose boundary, on the one hand, is determined by the trigger delay and, on the other hand, by the maximum duration of the chamber signal. In our case, the signal duration, as a rule, does

not exceed 160-170 ns what corresponds approximately to eight locations. To determine the number of the fired wire, for a majority of events it is sufficient to read the contents of only the first locations, but for some reasons, situations arise when the data is written with some scattering. So, the system uses the logical summation at several adjacent locations of one line - in so-called time window. The size of the window is set by program.

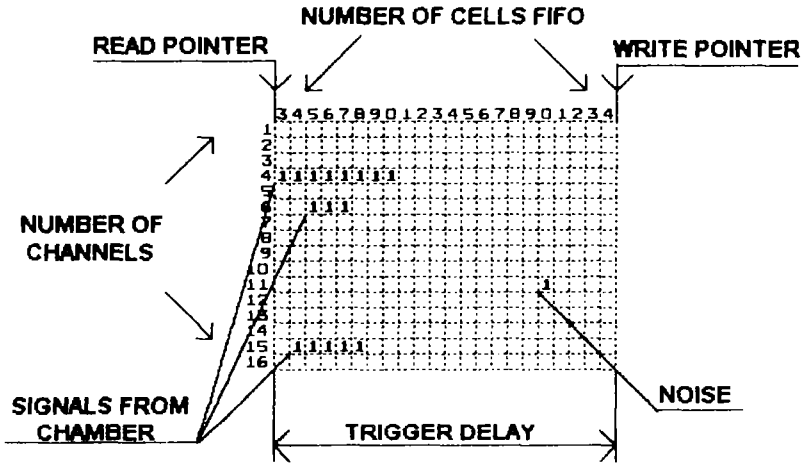

Fig. 6. Schematic representation of the FIFO memory contents on condition that the read pointer is set in accordance with the trigger delay

The logic adder is based on a Series 3000 EPM3032A microcircuit with programmable logic from the ALTERA company. It makes it possible to select the summation algorithm, taking into account special features of the system application. Logic adder outputs have Z-status. So, they can be unified into a bus; in this case, into 16-bit one (see. Fig. 3). Each adder (if the data is available) produces a request signal (LAM1-LAM4, respectively, see Fig. 3), which is applied to the control circuit. As it was noted earlier, these signals are used for shaping the common LAM signal. There are two determined by

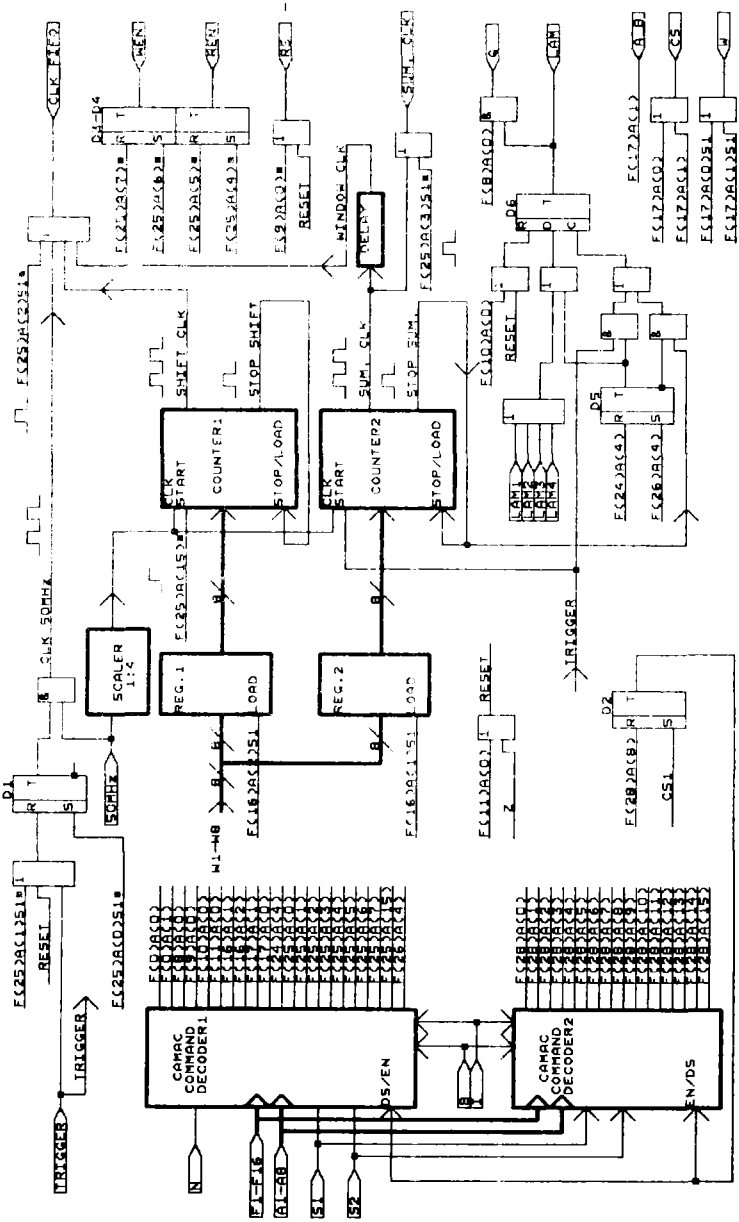

Fig.7. Simplified block diagram of the control device based on the ALTERA EPM7128SLC84-15 programmable logic microcircuit

program versions of shaping the LAM signal: 1) by trigger signal and 2) with available data in the adder. The first version is basically used for adjustment and tests of ADD-32 units; the second one is used in the data reading to skip units which do not contain the data.

Figure 7 shows a simplified block diagram of the control unit of the ADD-32 unit, which consists of an interface for the unit interaction with the CAMAC bus, FIFO microcircuit control circuit, and AD7302 8-bit two-channel DAC control circuit. The register REG.1 stores a shift code of the write pointer for the FIFO microcircuit (this code is the digital equivalent of the trigger delay expressed in periods of the clock generator). The code is written in the write pointer shift circuit, which by command F(25)A(15) produces a given number of pulses at the CLK input of the FIFO microcircuit. In this case, WEN should be set to the enabling status, and REN to the disabling one. The register REG.2 stores the time window code determining the number of memory locations at which the logical summation will be performed. With arrival of the Trigger signal, the circuit produces a given number of pulses. If the code is zero, the logical summation is not performed.

All the ADD-32 commands are divided into two types - single-module and multimodule (in Fig. 7 the single-module commands which have analogs among multimodule commands are marked with asterisk). The main difference between them lies in the fact that, to execute a single-module command, it is necessary to decode station numbers, i.e. they are the usual standard CAMAC commands. In using multimodule command, the decoding is not required. Thus, the multimodule commands are executed simultaneously in all the ADD-32 units. The use of similar commands was required to speed up the operation of the total system.

Of additional units, 18-channel NIM signal splitter and crate-controller were required.

The anode and cathode electronics of the PIBETA detector have successfully worked in the course of several years during continuous many-

month-long data-taking runs for experimental study of the processes $\pi^+ \to \pi^0 e^+ \nu$ and $\pi^+ \to e^+ \nu \gamma$.

This work is supported by the Russian Foundation for Basic Research, project No. 01-02-16412.

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Калинников В. А. и др. E13-2002-290
Анодная и катодная электроника для считывания информации
с цилиндрических многопроволочных пропорциональных камер
установки PIBETA

Катодный усилитель предназначен для усиления положительных импульсов тока, поступающих с катодов пропорциональных камер, и последующей передачи их через кабель с волновым сопротивлением 50 Ом на вход АЦП 1882F. Выходные сигналы усилителя специально согласованы для работы с данным типом АЦП.

Особенностью анодной системы является размещение усилительной части блока задержки сигнала и цифровой части в одном общем модуле АДД-32 (КАМАК). В одном модуле АДД-32 размером 1М содержится электроника на 32 проволочки, что позволяет разместить в крейте КАМАК со стандартной магистралью до 672 каналов приема данных. Для усиления сигналов используются 8-канальные микросхемы «Ampl 8.3». Задержка выходных логических сигналов выполнена на 9-канальных FIFO-микросхемах IDT72421, что позволяет получать полную задержку сигнала до сотен микросекунд и более. Цифровая часть системы выполнена на программируемых логических матрицах фирмы ALTERA. В настоящее время такая система общим объемом 576 каналов используется в эксперименте PIBETA по изучению редких распадов пионов на ускорителе PSI (*Швейцария*).

Работа выполнена в Лаборатории ядерных проблем им. В. П. Джелепова ОИЯИ.

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Anode and Cathode Readout Electronics for Cylindrical Multiwire
Proportional Chambers of the PIBETA Detector

The cathode amplifier is intended to amplify the positive current pulses from the cathode strips of proportional chambers and drive the 50 Ohm coaxial cable. The amplifier gain and the output voltage swing are matched for operation with the LeCroy 1882F ADC.

The special feature of the anode system is the integration of the amplifying section, signal delay unit and digital section for the data outputting to computer in the common ADD-32 module (CAMAC). The 1M-wide ADD-32 module contains the electronics for 32 wires that makes it possible to place up to 672 data channels in the CAMAC crate with a standard bus. To amplify signals, Ampl 8.3 8-channel microcircuits are used. The output logic signals are delayed by 9-channel IDT72421 FIFO microcircuits that enables one to obtain a total signal delay of up to hundreds of microseconds and longer. The digital section of the system is based on ALTERA programmable logic arrays. This system with a total of 576 channels is used in the PIBETA experiment to study rare pion decays on the PSI accelerator (Switzerland).

The investigation has been performed at the Dzhelepov Laboratory of Nuclear Problems, JINR.

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