ATLAS Level-1 Calorimeter Trigger: Subsystem Tests of a Jet/Energy-sum Processor Module

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***Abstract*— The ATLAS Level-1 Calorimeter Trigger consists of a Preprocessor, a Cluster Processor (CP), and a Jet/Energy-sum Processor (JEP). The CP and JEP receive digitised trigger-tower data from the Preprocessor and produce trigger multiplicities and total and missing energy for the final trigger decision. The trigger will also provide region-of-interest (RoI) information for the Level-2 trigger and intermediate results of the data acquisition (DAQ) system for monitoring and diagnostics by using readout driver modules (ROD).**

The Jet/Energy-sum Processor identifies and localises jets, and sums total and missing transverse energy information from the trigger data. The Jet/Energy Module (JEM) is the main module of the Jet/Energy-sum Processor. The JEM prototype is designed to be functionally identical to the final production module for ATLAS, and have the full number of channels. Three JEM prototypes have been built and successfully tested. Various test vector patterns were used to test the energy summation and the jet algorithms. Data communication between adjacent Jet/Energy Modules and all other relevant modules of the Jet/Energy-sum Processor has been tested. Recent test results using the Jet/Energy Module prototypes are discussed.

I. Introduction

At the full LHC design luminosity of $10^{34}\text{cm}^{-2}\text{s}{-1}$, there will be approximately 23 proton-proton interactions per bunch crossing. The ATLAS Level-1 trigger is to reduce the 40 Mhz interaction rate to a trigger rate of 75 kHz for input to the Level-2 trigger. The reduction is performed by processing reduced granularity data from the calorimeters and muon spectrometer. Muon candidates are identified in a separate trigger.

In the Level-1 calorimeter potentially interesting events are selected by identifying electron/photon candidates, jets, single-hadron/tau candidates, missing transverse energy, and total transverse energy. The algorithms are implemented in two processor systems: The Cluster Processor (CP) and the Jet/Energy-sum Processor (JEP). Those two processor systems send results for every bunch crossing to the Central Trigger Processor (CTP) which makes a Level-1 Accept (L1A) decision based on them, including additional data from the Muon Level-1 Trigger system. If the CTP accepts the event, the processors read out more detailed information on the types and locations of event features (Regions of Interest - RoI) and provides it to the Level-2 Trigger. The latency of the Level-1 trigger is limited to 2 μsec. The system is built using costum designed, fast digital electronics. The ATLAS Level-1 calorimeter trigger processors use field-programmable gate arrays (FPGAs) as their main technology, which offer both the required performance and high flexibility.

This paper describes the Jet/Energy-sum Processor of the Level-1 calorimeter Trigger system, designed to identify and localise jets, and to sum total and missing transverse energy information. After a more detailed description of the Level-1 calorimeter trigger system, the architecture of the Jet/Energy-sum Processor is described and standalone tests on real time data will be presented and its integration with other modules of the Level-1 trigger will be shown.

II. The ATLAS Level-1 Calorimeter Trigger System

As shown in Figure 1, the ATLAS Level-1 Calorimeter Trigger system [1] consists of three subsystems, namely the Preprocessor, electron/photon and tau/hadron Cluster Processor (CP), and the Jet/Energy-sum Processor (JEP). The CP and JEP will receive digitised calorimeter trigger-tower (TT) data from the Preprocessor, and send trigger multiplicity information to the Central Trigger Processor (CTP) via Common Merger Modules (CMM). Using Readout Driver (ROD) modules, the CP

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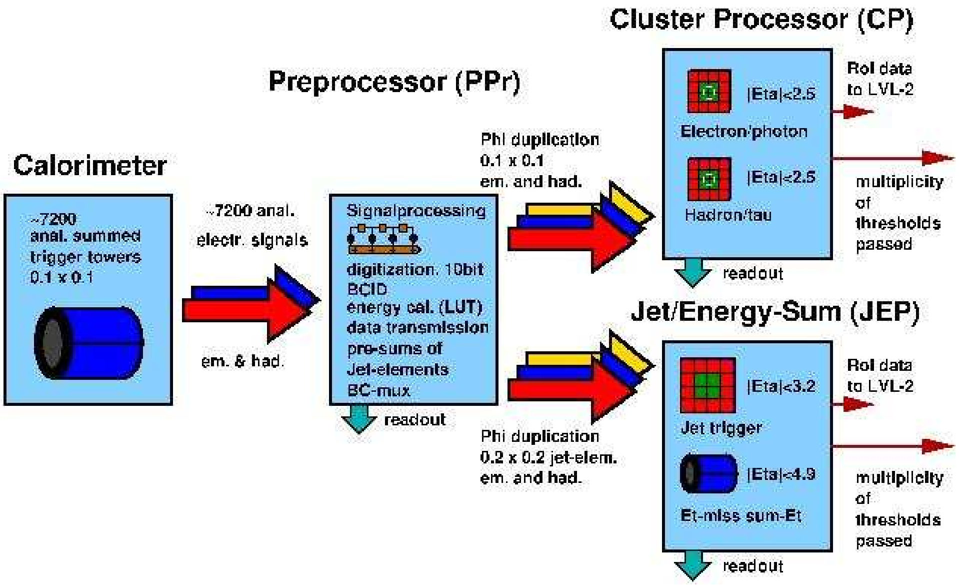

Fig. 1. The ATLAS Level-1 Calorimeter System

and JEP will also provide region-of-interest (RoI) information for the Level-2 trigger, and intermediate and final results to the data acquisition (DAQ) system for monitoring and diagnostic purposes.

The calorimeter trigger covers the region $-4.9 < \eta < 4.9$ and $\phi = 0$ to 2π. On the detector, cells are combined to form trigger towers, with a reduced granularity of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ over the region $-2.5 < \eta < 2.5$ for the CP and a granularity of $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$ for the JEP. Analogue pulses enter the Preprocessor, where they are digitised to 10-bit precision at a frequency of 40 MHz. After bunch-crossing identification (BCID), the precise value of transverse energy for each trigger tower is produced in a lookup table. The transverse energy is an 8-bit word, giving a transverse energy scale up to 255 GeV. The total numbers of trigger towers is 7200.

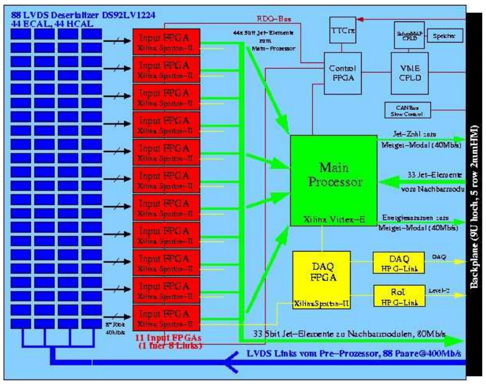

Fig. 2. Schematic architecture of a Jet/Energy module (JEM), prototype version 0.1/0.2. One module uses a XCV600E device as Main Processor, the second one a XCV1600E.

III. JET/ENERGY-SUM PROCESSOR

The JEP [2] must handle a large number of input signals and provide very fast logic. To minimise complexity of inter-module fanin-fanout caused by the use of sliding window algorithms, the system is subdivided into four quadrants, equivalent to the quadrants of the ATLAS calorimeters, which are each covered by a set of 8 Jet/Energy Modules (JEMs). For reasons of cost and flexibility, the JEM uses programmable logic devices (FPGAs). All algorithms are developed, simulated and implemented using the hardware description language VHDL. The JEMs are purely digital modules, controlled via VME interface. The architecture of a JEM is shown in Figure 2.

Each JEM receives 88 data streams of 9-bit width via the serial links with each LHC bunch crossing (25 ns). These are the electromagnetic and hadronic components of jet elements 0.2×0.2 in $\eta - \phi$. The receiving link chips de-serialise the data back to 40 MHz parallel words. In the 11 Input Processor FPGAs, the input electromagnetic and hadronic data are summed to form the 10-bit jet Elements, which are then sent to the JEMs central component, the MainProcessor FPGA. The jet finding algorithm requires not only data from one JEM, but it also needs to correctly analyse jets crossing the JEMs boundary. Therefore, the jet elements are also copied to the neighbouring JEMs via the backplane at 80 Mb/s. For the same reason, jet elements near the border of adjacent quadrants are duplicated in the Preprocessor and sent to JEMs in both quadrants. This results in a 11×7 in $\eta - \phi$ of jet elements available to the jet algorithms on one JEM. The energy sums are calculated from the 64 non-duplicated channels jet elements only (see Figure3).

The Main Processor calculates the local transverse energy (E_T) sum and the projections E_x and E_y of E_T in X and Y direction for each $\Delta\phi$-bin.

These three energy values are coded to 8 bits each using a quad-linear compression scheme, and sent from each of the 16 JEMs located in one crate to a Common Merger

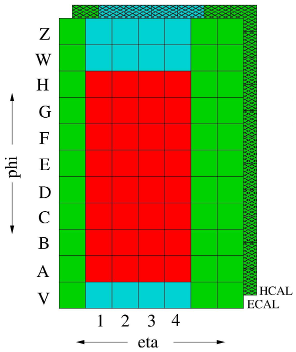

Fig. 3. Channel map of a JEM: total range of input channels: 11×7 in $\eta - \phi$, of which 8×4 in $\eta - \phi$ are the core region.

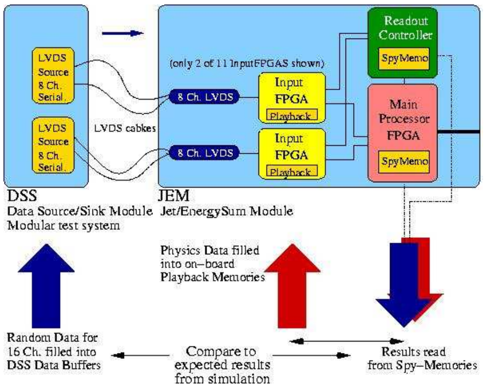

Fig. 4. Standalone test of the Jet/Energy Module with on board memories (playback and spy) and 16 channels serial LVDS input.

Module running firmware that forms the crate energy sums and ultimately the trigger sums that are sent to the Central Trigger Processor (CTP).

The jet algorithm identifies clusters of energy deposition within overlapping windows of adjustable size of 2×2, 3×3 or 4×4 jet elements. Jet locations are determined by looking for local maxima in regions of 2×2 jet elements. The total counts of jets above 8 different programmable transverse-energy thresholds and window sizes are sent to another Common Merger Module running firmware that forms crate jet multiplicities and ultimately the sums over the full trigger that are sent to the CTP.

In order to allow for standalone tests and diagnostics of the JEM, test patterns can be stored in “playback” memory blocks of 255 words depth located on the Input Processors. The data can be injected into the trigger data path to test transmission and processing further down the data chain. The results are sampled in local “spy” memories on the outputs of the Main Processor, also with a depth of 255 words.

IV. Standalone tests of JET/Energy module

Systematic tests [3] have been performed on the JEM prototypes in order to assure correct and reliable operation of the JEM within the trigger environment. As a first step, the modules are operated stand-alone with the system clock provided by the onboard crystal oscillator, not by a TTC system. The playback memories of 256 words depth within the InputFPGAs are filled with various data patterns. A playback/spy cycle is initiated via a VME signal and the results from the spy memories are read back and compared offline by the incrate-CPU with the results of a closely modelled simulation program for the energy summation. Simple tests programs have been used, allowing fast throughput of data, but not interacting the Level-1 trigger software environment. As a second step a Data Source/Sink module (DSS) fitted with two LVDS Source daughtermodules has been used, which provide a total of 16 serial LVDS channels, being able to serve two neighbouring InputFPGAs with data as expected from the Preprocessor system.

Figure 4 shows the procedure of the standalone tests of the Jet/Energy Module.

A. Test patterns

Two options of test patterns are available for JEM prototypes. The physics patterns, in this case the $t\bar{t} \rightarrow W^+W^-b\bar{b} \rightarrow$ Jets channel were produced by the event generator PYTHIA and fed then into the detector and trigger simulation ATLFAST and ATL1CT. 2.5 million events have been produced and stored for using in tests. Since a JEM covers only a very small area of space, an equivalent area was written out by the trigger simulation which has more than 64 GeV of transverse energy depositions. Since the deposition per event is very low, the kinematic cuts on the production level of PYTHIA have been set very high, in order to increase the rate of high energy jets within the data sample for the JEM: Mass 700-2000 GeV, transverse momentum p_T >500 GeV. This set of test patterns requires all 64 channels of the core region to be filled with data, which can always be achieved using the onboard playback memories, but they are not usable if only a small set of real input LVDS channels is available.

Random patterns are also produced which cover the whole range of input data up to 9 bit (511 GeV) and are sensible for those tests with a limited number of input channels of the JEM’s. In order to increase the rate of high-energetic channels, but at the same time to avoid saturation, the channels are filled using a random number between 0 and 1 folded with a sloping exponential function ranging from 0 to 511. These random patterns have also been used with the full channel number.

B. Test using Playback and Spy memories only

Two JEM prototypes have been tested using the test vector patterns described above. A test was performed using the $t\bar{t}$-event library, processing the library 24 times, with a total of 60 million events. The results for the energy summation algorithm for $\Sigma E_x, \Sigma E_y$ and ΣE_T were identical to the expected values from the offline summation. Another test used random patterns. A total of 6 million events was processed, also showing the expected results for the energy sums.

Fig. 5. Latency measurement of the real time data path of the JEM prototype (energy summation only): Total latency of 8 bunch crossings (25 ns each).

C. Test using 16 channels serial LVDS input data from DSS and spy memories

The test was then extended using a Data Source/Sink module fitted with two LVDS Source daughtermodules, which provide a total of 16 serial LVDS channels, being able to serve two neighbouring InputFPGAs with data as expected from the Preprocessor system. Due to the limited number of channels, the random patterns described above have been used in this test. For this test, the data buffers in the DSS (depth 32k words) are filled repetitively with the random test vectors. The DSS is set to send a constant stream of data. A VME signal enables the spy memory inside the JEM's Main Processor to be filled. The data is then read back from this memory, matched with repetitive stream and compared with the expected results. This setup processed 1.8 million events and all received values for the energy sums was as expected. The test has been repeated using all four possible pairs for InputFPGAs in the core region (A and B, C and D, E and F, G and H).

D. Loopback test of duplicated channels

In order to test the connectivity of the backplane, a loopback device has been designed, feeding the outputs of jet element data from the InputFPGAs intended to go to the neighbouring JEM back into the Main Processor of the same JEM. The energy summation algorithm is changed to accept the duplicated channels instead of the core region. A test pattern of a binary counter is used to check the correct reception of the data, which has been found to work properly.

V. Test of JetEnergy module with LVDS data feed within ATLAS software environment controlled by TTC

The test setup for the JEM prototype was then extended with a TTC system for system clocking and command distribution. A daughtermodule housing a TTCrx chip is mounted on the JEM prototype. A TTC system consisting of a TTCvi and a TTCvx module is connected to the JEM via the electrical output and to the DSS via the optical output. Whereas the tests described in the previous paragraph have been controlled by simple test scripts and programms based on the VME driver routines, all further tests have carried out using routines in C++ within the Level-1 Calorimeter Trigger software environment.

The Linux installation of RedHat 7.3 of the VME single board computer includes the ATLAS online software package and the CERN VME driver. The Level-1 Calorimeter Trigger software is installed, which includes all necessary routines to initialise, configure and control the hardware as well as the simulation. The routines dealing with the hardware directly, the *ModuleServices*, are developed in the responsible groups as well as the simulation *ModuleSim*, which are being developed for each module, very closely modelling the functionality of the modules. The simulation is run in parallel in an identical setup as the hardware. This setup is described by database files using XML, which include all information about module types, crate location of modules, cables and connections. The test setup is controlled by the *RunControl*. The firmware of the InputFPGAs is supplemented with a input synchronisation stage, which ensures a reliable data transfer at the input stage of the JEM by adjusting the clock phase of the internal DLLs of the Xilinx Spartan-II FPGA in order to allow for compensation of delays between the input channels caused by cables and onboard tracks and routing. One of the four available clock phases of the DLLs is automatically selected when a special synchronisation pattern is fed to the InputFPGAs.

The tests described in the previous chapter have been repeated with this setup, using both the random and the physics test patterns. System commands for playback/spy cycles are broadcasted using the TTC system. The results read back from the spy-memories of the Main Processor have again been found to be identical to the expected values from the simulation. The main jet algorithm has been implemented into the JEM prototypes Main Processor, but the results are different from the expected values of the simulation. Therefore the implementation is being reworked, allowing to fit the algorithm into the present devices by optimisation of the VHDL code structure. The algorithm has been successfully simulated and run in a standalone environment.

The readout functionality of the module was tested in a standalone setup using a spy-memory within the ROC, that captures all readout data streams from the Input and Main Processor FPGAs. The data has been found to match the expected data packets. Further tests using the complete readout chain are described in the following paragraph. Using the two available JEM prototypes mounted into the custom backplane within the 9U crate, a latency measurement has been done. The deskew 2 setting of the TTC is used for this scan. The latency of the JEM algorithm has been found to 8 bunch crossings (25 ns each). A capture from the oscilloscope illustrating the latency is shown in Figure 5.

VI. Trigger prototype module integration: Readout of the JEM

All interfaces of the JEM to the outside world within the experiment environment are tested in an integration test. The

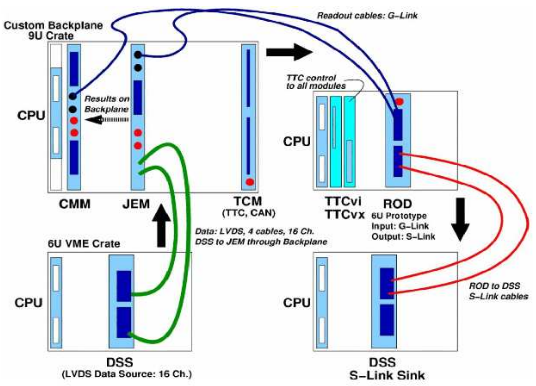

Fig. 6. Readout of Jet/Energy Module with DSS as LVDS data feed, Readout Driver and DSS for S-Link data sink.

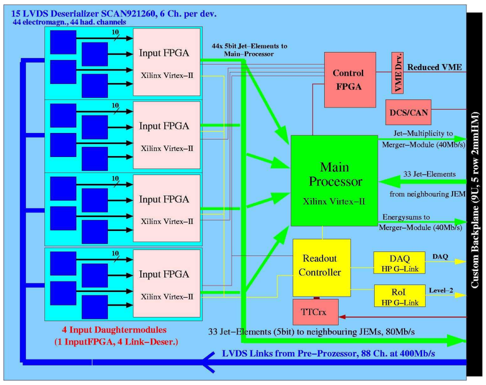

Fig. 7. The final Jet/Energy module for ATLAS.

setup is illustrated in Figure 6. Input data as expected from the Preprocessor is fed into the JEM using a DSS module with 16 channels of serial LVDS source. The results of the JEM are transmitted via the custom backplane to the Common Merger Module. The readout of both the JEM and the CMM is let onto G-Link cables connected to a prototype Readout Driver, which converts the readout data packets onto S-Link and transmits them onto cables. The data send through the S-Links is received by a DSS equipped with a S-Link sink module. Using this setup, incoming data and results at all interface stages of the system can be checked both by comparing the readout data and also by using the spy memories inside the modules. In order to assure a consistent set of data from the various stages, the readout signal is provided by the TTC system, which is also used to provide all system clocks. The system has also been tested for the whole number of input channels using the playback memories of the JEM's InputFPGAs. The expected S-Link output data is generated by the simulation chain. Both sources of input data - either the DSS's data buffers or the InputFPGA playback memories - are filled using the very same data patterns as the online trigger module simulation, allowing for an automated comparison of the readout streams.

VII. Development of final JEM for ATLAS

Based on the positive results of this programme, the final Jet/Energy modules (Module 1) will be designed in 2003. Volume production of the 32 JEMs needed for ATLAS will start in 2004. The next generation of the JEM is planned to be the module to be used in the final ATLAS Level-1 Calorimeter trigger, is being designed taking into account the experiences from the tests of the prototype modules and the development in technology. A schematic overview of this module is given in Figure 7. LVDS deserialiser devices of the SCAN series are used, which will allow for JTAG/Boundary scan testing of the onboard connections. Each of those devices deserialises 6 data channels. A new generation of FPGAs, the Virtex-II series, has become common and will be used on JEM-1. They offer higher logic densities and improved performance. Since fine-pitch BGA packages are usually fitted to smaller PCBs in the current commercial market, it has been decided to fit one InputFPGA and four LVDS deserialisers on daughtermodules. A JEM-1 will be fitted with four of those daughtermodules. The use of daughtermodules also simplifies the rework of faulty modules signifcantly, as they can be easily replaced. The readout and control functions will also be on a daughtermodule, leaving basically only the Main Processor mounted on the mainboard of JEM-1. The firmware has been updated to match the new devices and mapping. Since all interfaces to the outside world are identical, Module-1 can replace the current prototype in the module integration tests. The daughtermodules and the mainboard are under production and will be subjected to standalone tests and module integration tests in 2004.

VIII. Conclusion

Two fully functional JEM prototypes have been designed, produced and tested in a stand-alone test setup using test vectors for the energy sum algorithm. Test vectors were generated by the trigger simulation, which provides both input data for the JEM and the expected energy summation results. Since all stand-alone tests of the electronics modules have been successful, two JEMs are being subjected to system tests in a setup simulating the final ATLAS environment. These measurements allowed for thorough tests of all interfaces of the JEM to the outside world, encompassing both the physical interfaces as well as the software integration. A complete set of LVDS sources, the final backplane, Timing and Trigger distribution system and Readout System was available. Based on the results of this programme and recent developments in technology and board manufacturing, the final Jet/Energy module is being designed. Volume production of the 32 JEMs needed for ATLAS will start in 2004.

References

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