THE PSALM PROJECT

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ABSTRACT

An Analog Linear Memory with Pedestal Subtraction (PSALM) is being developed jointly by LAL-Orsay and CEN-Saclay for the readout of the electromagnetic calorimeter of the ATLAS experiment at the future LHC collider. Preliminary results from a second prototype, received in august 1994, are presented. The dynamic range achieved on a test bench is 12 bits.

In 1993, LAL Orsay and CEN Saclay started a joint development for an analog memory that might be part of the readout electronics of the ATLAS electromagnetic calorimeter. Such analog memories were already in use on the ZEUS experiment at DESY [1], and similar developments were under way in the University of Alberta (in cooperation with LBL) [2] and in Nevis labs [3].

We have used an original design for all components in our memory chip, in particular for the operational amplifiers and analog buffers, and an original layout. We have also used a different process from our competitors [4]. However, the main originality in our project is the systematic subtraction, when reading a data from the memory, of the parasitic charges added to the signal during the write and read operations. This pedestal depends in general on the position used in the memory. Its subtraction should increase the dynamic range of the memory, in particular when no further memory cell-dependant corrections can be applied.

1. Architecture of the calorimeter readout

In the analog approach, the signal from each calorimeter cell is sampled permanently at the LHC bunch crossing frequency (40MHz) and each sample is stored in an analog memory during the latency of the level 1 trigger (2 μs). In case of a positive trigger decision, a number of samples, centered on the corresponding bunch crossing, are read back from the analog memory and digitized. At the maximum trigger rate (100 kHz), we may digitize up to 5 samples per event. We may use even more samples at lower trigger rate.

After digitization, the ADC words are calibrated. Then, the several samples from each calorimeter cell are combined to give a single estimate of the energy in the cell,

of the time of the incoming particle, and of the signal quality. The result is made available in a convenient form for the level 2 trigger and for the data acquisition system.

The main advantage of this solution is that only interesting data are digitized. This may be achieved with a limited number of commercially available ADCs, at a limited cost. Because of the important R&D effort, analog memories just fitting the requirements already exist in the form of prototypes, and even better chips will be available at low cost (less than 10 SF/channel) in the next few years.

2. Requirements on the analog memory

2.1. Dual port memory

To limit the dead time, the sampling of the calorimeter signals and their storage into the analog memory should not stop when data are being read back from the memory.

2.2. Thirteen bit dynamic range

The dynamic range of the electronics for each calorimeter cell should be in excess of 16 bits, and should not degrade the calorimeter resolution. To cope with this difficult requirement, we send the signal from a single pre-amplifier (associated to a single calorimeter cell) into two shapers, each with a dynamic range of the order of 10,000, and with a gain ratio of the order of 12. We associate to each shaper channel an analog memory channel, with a 13 bit dynamic range.

For example, if we use this dual gain system associated to a 13 bit ADC with an rms precision equal to half the lsb to measure energies between -100 GeV and +2 TeV in a cell, it will introduce an rms noise of 24 MeV, to be added in quadrature to the pre-amplifier noise. This is adequate.

3. Principle of an analog memory

A "write address" is given to the memory chip by an external controller each 25 ns. It is distributed on a bus inside the memory chip. Switches allow to sample the input signal and store the resulting voltage in the capacitor corresponding to the given write address. To retrieve a sample, the controller sends its position to the memory chip. Switches allow to place the corresponding capacitor in the feed-back loop of the read amplifier.

4. Limitations of the dynamic range

The limitation of the dynamic range does not come from true noise, but from two systematic effects :

- cross-talk from the digital lines to the input signal. With simultaneous write and read operations, the cross-talk may occur either when sampling the signal

or when reading it back. If the capacitors were always accessed in the same sequence, then the cross-talk affecting a given capacitor would always be the same, and this effect would be corrected by using an effective pedestal, different in each capacitor. However, this does not hold in the case of random accesses, and this effect should be considered as a noise.

- parasitic charges injected by the switches. The switches to write and read are not exactly identical from capacitor to capacitor. As a result, the parasitic charge they inject may be different, and the pedestal value then depends on the capacitor. Using the same average pedestal for all 128 capacitors associated to a given input channel results in measurement errors which should also be considered as noise. The PSALM has been designed to get rid of this effect.

5. Description of the PSALM

One PSALM channel is shown on figure 1. A signal is sampled in a capacitor C_P by switch 1. Switch 2 is then opened to isolate the capacitor. To read, one uses switches 3, 4 and 13 *. To perform the pedestal subtraction, a signal just read is temporarily stored in capacitor C_C using switches 7 and 8. Then C_P is cleared using switches 1 and 5, and a second read operation is performed, the result being temporarily stored in capacitor C_S using switch 6. Switches 9,11 and 10 allow to transfer the difference between the two readings to the output amplifier.

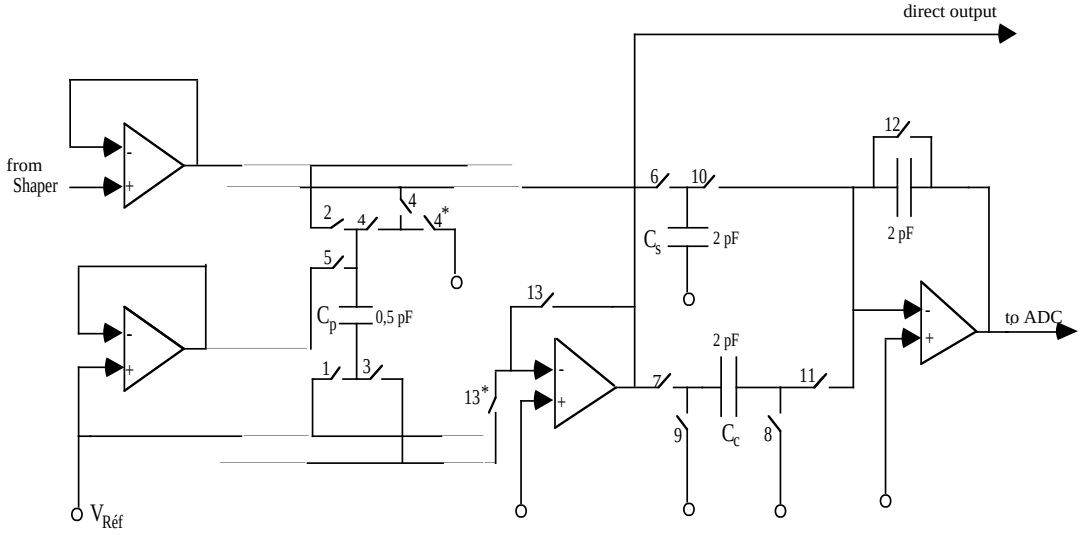

Figure 1: *Schematic view of one PSALM channel*
(only one of the 128 capacitors is shown)

After a first prototype received in march 1994, we have received a second version in august 1994. This chip has 4 channels, each with 128 capacitors.

6. Description of the test bench

For the first measurements, we have developed a test bench split in two boards, linked by a short cable :

- The analog board carries a PSALM chip, a 12 bit 10 MHz ADC associated to a Fifo. Multiplexers allow to send either an external signal or the reference voltage to any of the four inputs of the PSALM. Multiplexers also allow to read either the pedestal subtracted output, the direct output, or the reference voltage, and to perform any subtraction between two of these signals externally to the PSALM chip. The signal may be amplified by a factor 10 at the input of the ADC for a better measurement of pedestals and noise.

- The digital board sits in a VME crate. It provides write addresses (at 40 MHz) and read addresses to the PSALM, but does not allow at the moment simultaneous write and read operations. It also provides a VME interface with a MacIntosh computer, where data are collected from the Fifo and analysed.

7. Preliminary results

The power dissipation of the PSALM chip is 0.5 W, mainly due to the 40 MHz clock. This dissipation should be substantially lower for the next versions. The power dissipation on analog voltages is small (4.5 mW per input channel).

7.1. Dynamic range

We have first measured the system linearity, using DC levels. With a non-linearity below 0.2%, the dynamic range is in excess of 3.3 V. It should be increased by 1 Volt changing the NMOS switches 2, 5 and 4 to CMOS ones. Measurement using the output of present RD 3 shapers are being performed.

The cell to cell dispersion of the pedestal for a given channel, measured without any pedestal subtraction is 0.85 mV rms. We obtain the same number when measuring the difference between two adjacent channels, which shows that only a fraction of this dispersion is coherent over the channels.

If we clear each capacitor before reading it, still using no pedestal subtraction, the cell to cell dispersion goes down to 0.64 mV rms. This contribution should be completely suppressed by the pedestal subtraction, leaving a cell to cell dispersion as small as 0.6 mV. However, when we really use the pedestal subtraction, we obtain a dispersion of 0.8 mV. We hope to obtain better result whith a better tuning of the present chip.

7.2. Noise level

At the moment, we measure an rms noise of 0.8 mV per capacitor. However, we have characterised the op-amplifier which is used in the chip and measured a noise

level less than 0.1 mV rms, for a 1 GHz bandwidth. We therefore anticipate a noise level per capacitor of 0.5 mV rms. A better design of switch 13 (reset of the read amplifier) should allow to go down to 0.35 mV.

The noise level is still 0.8 mV rms per sample when measuring the difference between two adjacent channels. Part of this noise is therefore coherent over the channels. This contribution comes from a coupling between the the PSALM chip and the analog board. We experience that the simple analog board on the test bench needs a very careful design in order to fully benefit from the PSALM performances.

8. Conclusions

Using only one pedestal per channel, our system reaches a dynamic range of 2750 (11.5 bits). With one pedestal per capacitor, we obtain 12 bits.

With a better design of the analog board, we anticipate a dynamic range of 3500 with only one pedestal per channel, and 6600 (12.7 bits) with one pedestal per capacitor.

The next version of the chip will have a dynamic range in excess of 4 Volts, with an rms noise of 0.35 mV. It will carry 16 channels and is expected in Orsay in february 95.

A new digital board for our test bench will allow measurements on the present PSALM chip with simultaneous write and read operations in december 1994.

We prepare a system to be used in the readout of the prototype accordeon calorimeter in a test beam at CERN in 1995.

In the end, our present experience tells us that the design of a board carrying analog memories (such as the future front-end board for the ATLAS calorimeter) is especially delicate.

References

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