Technical Specifications of the First Prototype Pixel Sensors for ATLAS

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Abstract

The design of the First Prototype Pixel Sensors for ATLAS has been completed. The wafers will include two large rectangular structures, each of which accepts 16 readout chips and is compatible with the prototype barrel module design. The two structures, designated Tile 1 and Tile 2, permit examination of a variety of design options and are described here.

1 Overview of the ATLAS Pixel Sensor Program

The ATLAS Experiment at the CERN LHC will include a silicon pixel detector as its innermost tracking chamber. The detector will consist of three layers of rectangular sensors arranged in a cylindrical ("barrel") pattern coaxial with the beamline, and 8 layers of wedge-shaped sensors assembled into disks. The detector will require 1586 barrel sensors and 1000 disk sensors.

The pixel detector must survive for 10 years in the hostile radiation environment of the collider. The sensors closest to the beam will receive more than 10^{15} minimum ionizing particles/cm^2. The anticipated need to operate the sensors partially depleted after some point in their radiation lifetime is the dominant factor in the choice of n-type implants in n-type substrate. As radiation damage to the bulk will require increasingly higher operating voltages during the detector's lifetime, the requirement of operating these sensors at high voltage without electrical breakdown or microdischarge is also important to the design. Some features of the design also reflect the desire to provide bias to every pixel without attaching the readout integrated circuit. This is expected to facilitate testing of the sensors prior to bonding and to guarantee a uniform electric field in the sensor active area in cases of failure of a bump bond.

The ATLAS pixel sensor design program will include fabrication of First Prototypes and Second Prototypes prior to production sensors. This document primarily concerns the First Prototypes. The First Prototype wafers contain 2 large structures, called Tile 1[1] and Tile 2[1, 2], as well as various test structures which examine additional design options but which are not described here. Design details of the two Tiles are described below.

2 Introduction to the Sensors

Figure 1 is an example of a possible layout of the proposed structures on a 4″ wafer. Figure 2 (including its Details A, B, C, D, E, and F) illustrates the n-side of Tile 1 after processing. Figure 3 shows a bond pad region. Figure 4 (including its Details A, B, and C) illustrates features of Tile 2. Figure 5 shows the Tile 2 i/o bus structure. Figure 6 and its Detail A show the p-side guard ring. Figure 7 illustrates the second metal pattern.

Tile 2 uses p-spray for isolation, and Tile 1 uses p-stops.

3 Details of the Design

3.1 As-cut dimensions

The wafers containing the Tiles are provided by their manufacturer without dicing in order that they may be bumped first. After dicing, the dimensions of the Tiles are:

Tile 1 (default): 18.6×62.6 mm^2, and

Tile 2 (default): 24.4×62.6 mm^2.

It may be necessary to increase the distance between the guard ring and scribeline in order to guarantee sufficient radiation hardness. To provide for this possibility, a second scribeline is included which would give the Tiles the following dimensions:

Tile 1 (enlarged): 19.4×63.4 mm^2, and

Tile 2 (enlarged): 24.4×63.4 mm^2.

3.2 Active area

The active area of each Tile is drawn as 16 units. A "unit" is defined such that pixels in each unit use a common amplifier chip. The symmetry lines in Figures 2 and 4 show the arrangement of these units. The active area of each Tile (excluding guard ring) has dimensions 16.4×60.4 mm^2. The symmetry lines themselves do not represent physical structures and are for illustrative purposes only.

3.3 Cell geometry

On the accompanying figures, rows are labelled in the horizontal direction, columns in the vertical. The geometry of each cell is characterized as follows:

- Number of pixel cells per unit: 164×18

- Total number of pixel cells: 47232 ($= 16 \times 164 \times 18$)
- Pixel cell dimensions: $50 \times 400 \mu\text{m}^2$
- Cells that lie in adjacent columns but are read out by different chips are of dimension $50 \times 600 \mu\text{m}^2$ (see Figure 2, Detail B, and Figure 4, Detail B).

3.4 n-side guard ring

The Tiles use similar designs in the n-side guard ring area. There is an inner guard ring which consists in a metallized n^+ implant. On Tile 1 the implant has width 86.5μm; on Tile 2 the width is 90μm. On Tile 2 this inner ring can be used for biassing the whole array. Beyond the inner ring is an outer region covered with n^+ implant. The inner ring and outer region are separated by a gap. On Tile 1, that gap has total width 30μm and is unimplanted. To provide electrical isolation, a 10μm wide p-stop is placed in the center of the gap. On Tile 2, the gap is 8μm wide, and electrical isolation is provided by the p-spray implant which covers the whole device.

Contact pads to the n-type implant appear in the four corners of the Tile. On each Tile, one of these contact pads bears a label so that the orientation of the Tile is uniquely specified.

3.5 p-side guard ring

Both Tiles use the same design[3] for their p-side guard ring. This design appears in Figure 6 and in its Detail 6A. The multi-guardring structure contains 22 rings with a pitch that varies from 20μm near the sensitive area to 50μm near the edge. The p-implant is 10μm wide in every ring while the gap increases from the center to the edge. The metal overlaps the implant by half of the gap width on the side of the ring facing the sensitive area. The entire guard ring structure is 520μm wide.

3.6 Implant dimensions

In Tile 1, the n-type implants are isolated from one another by p-stops of the individual, or "atoll," design. Pairs of units are additionally surrounded by a common p-stop frame. The dimensions of Tile 1 implants are as follows:

- n^+ implant width: 23μm
- p^+ implant width: 5μm
- gap between n-type and p-type implants: 6μm
- gap between neighboring p^+ implants: 5μm

Complete dimensions of the structures on Tile 2 are shown in Figure 4, Details A and B. For each pixel cell, the mask width of the central n-implant is 13μm, while the n-implant that surrounds it is 6μm wide. The spacing between those structures is 6μm. In both Tiles, corners are rounded to reduce electric fields. (See for example Figure 2, Detail D.)

3.7 Metallization

The first metal on Tile 1 has the following shape:

- Metal width on pixels: 14μm
- Metal width on the inner guard ring: 6μm narrower than the implant.

The masks for the metallization over the implant of Tile 2 show a width of 12μm, 1μm less than the mask width of the implant.

3.8 Pads

The bond pads are twenty-sided polygons (approximating circles). On Tile 1 the implant has mask diameter 21μm, or processed diameter approximately 23μm. On Tile 2 the implant has mask diameter 18μm. On both Tiles the

first and second metals have diameter 20μm. The passivation opening has diameter 12μm.

Bond pads are placed at the end of each pixel cell. This layout anticipates a mirrored electronics layout. The closely spaced bond pads are 50μm apart. (See Figure 2, Details A and B). A cross section of a bond pad region is included in Figure 3.

Some pixels have no bond pads. Those cells will have no preamplifier directly above them and so must have their signals routed to bond pads on pixels a few rows away in the same column. For both Tiles, the routing will use a single metal layer. Figure 2 Details C and E show the routing for Tile 1 while Figure 4 Details B and C show it for Tile 2.

Bias pads are placed in several locations on the inner n^+ guard ring. They form two extra rows with the same 50μm pitch as the pixels have. See Figure 2, Detail F for an example of n-side bias pad placement.

Probing pads are placed on the inner guard ring in the region between adjacent units (see Figure 2, Detail F).

3.9 p-side (back side) design

This information concerns both Tiles. A p^+ implant is continuous in the area covered by pixels. The aluminization has $30 \times 100\mu\text{m}^2$ apertures to facilitate stimulating the cells from the p-side with a laser. No unpassivated n^+ implants or contacts to the n-bulk substrate are permitted. Redundant bond pads for p-side biasing are provided.

3.10 Double metal

The manufacturers will apply insulator and a second metal layer to 30% of the First Prototypes. Devices with and without double metal will not differ in any aspect of their design other than the double metal itself, the insulator, and the addition of vias to allow access through the insulator to first metal pads. In the First Prototype program, double-metal is being tested in some (redundant) busses on Tile 2 and as routing of signals from pixels at the edge of units to preamplifiers above neighboring implants. The busses run

parallel to the long side of the sensor and are located between bump bond pads and the active area. Figure 5 shows a detail of the bus structure on Tile 2.

The narrowest line in Metal 2 is 10μm wide and 1.5–2.0 μm thick. The minimum Metal 2 spacing, which is not critical, is greater than 20μm. In the bus structure, Metal 2 has width 20–50 μm. The contact holes are $3 \times 10\mu\text{m}^2$ in the masks. Metal on the first layer has thickness 1.2–1.5 μm. The insulator material varies with manufacturer: one vendor will use SiO_2; the other, polyimide. To maintain flatness of the bump pads, vias are not located beneath them. Figure 7 shows the second metal design.

Devices that have Metal 1 but not Metal 2 will be completely functional. In the devices with both metal layers, the outermost four rows of pixels are not connected by bumps directly to their preamplifiers (i.e., their bump pads have no vias). Signals from pixels in those rows are instead routed in Metal 2 to neighboring pixels by using the same metal pattern as appears in Metal 1 in the sensor's central region.

3.11 Passivation

The passivation must be compatible with technologies for applying bumps for bonding. A 1μm thick silicon nitride layer is used. The openings in the passivation for bump bonding have 12μm diameter.

4 Sensor Optical and Mechanical Properties

4.1 Wafer thickness

During the prototyping phase of the pixel project, options for using thin sensors will be explored. First Prototype sensors from one manufacturer have thickness 300μm, while those from the other have thickness 280μm.

4.2 Tolerances

The sensors must maintain the following tolerances:

- Uniformity of thickness: $\pm 10\mu$m
- Mask alignment: $\pm 2\mu$m

5 Sensor Electrical Properties

The following is a summary of the required electrical properties:

- Initial depletion voltage: 50–150V
- Initial maximum operating voltage: $\geq$ 200V
- Initial leakage current (for 300 micron wafers): < 100 nA/cm^2
- Initial oxide breakdown voltage: $\geq$ 100V.

6 Testing

Acceptance testing will be done by ATLAS only. The wafer will have test structures for monitoring flat band voltage, layer thickness, implant resistivity, aluminum sheet resistance, etching uniformity, and alignment.

7 Processing

The following processing requirements must be met:

1. n^+ implant dose: $> 10^{14}$/cm^2.
2. concerning n-side isolation:
    - for Tile 1, the p^+ implant dose should be $\geq 10^{13}$/cm^2.

- for Tile 2, the p-spray effective dose in silicon should be $3 \times 10^{12}/\mathrm{cm}^2$. Doping variation should be less than $\pm 0.5 \times 10^{12}/\mathrm{cm}^2$.

3. Back contact (p-side) dose: $> 10^{14}/\mathrm{cm}^2$.

4. Implant depth after processing is to be $\geq 1\mu$m.

8 Radiation Hardness

The following specifications *will be required* for production sensors. They are *not required* of prototype sensors. The properties of irradiated prototype sensors will nonetheless be studied.

The production sensors must have the following performance after an irradiation of 10^{15} p/cm^2:

1. Breakdown voltage: > 500 V.

2. Depletion voltage (for 300 micron sensors): < 800 V.

3. Leakage current (measured at $-5°$ C) after one month of annealing at $20°$ C (for 300 micron sensors): $< 125\mu\mathrm{A}/\mathrm{cm}^2$ or < 25 nA per pixel cell.

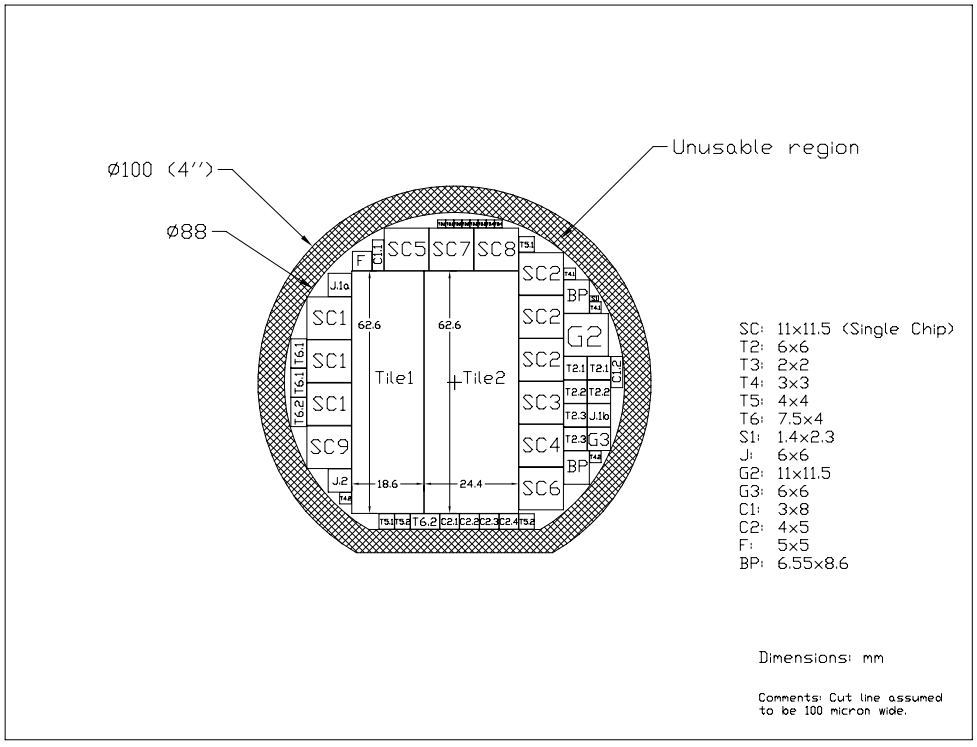

Figure 1: A possible layout of Tiles 1 and 2 and test structures on a 4 inch wafer.

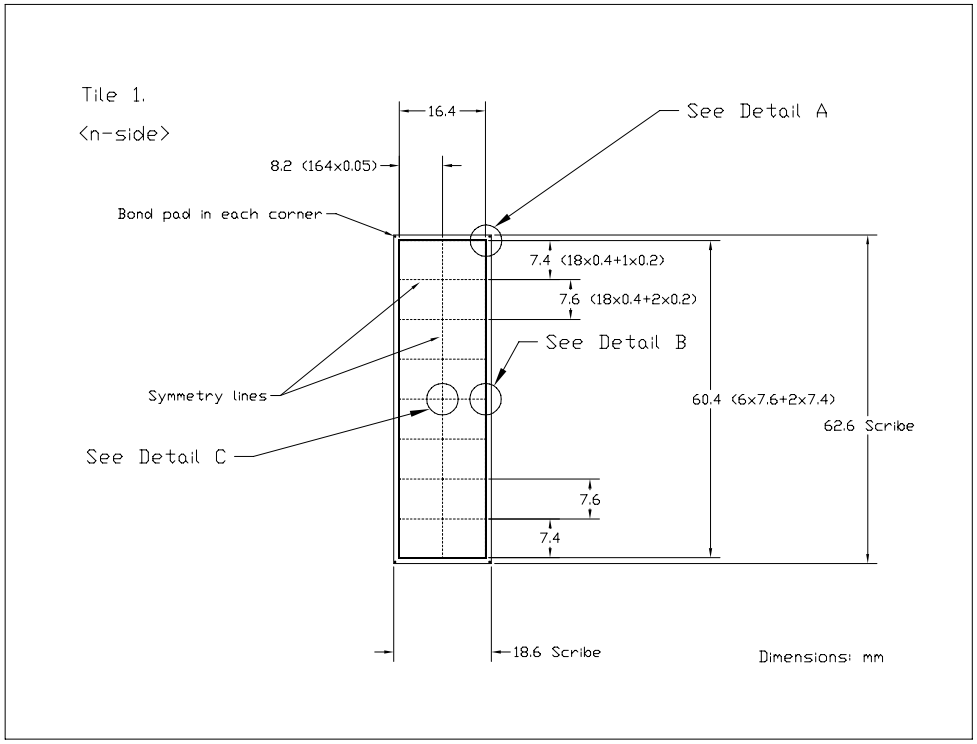

Figure 2: The Tile 1 concept.

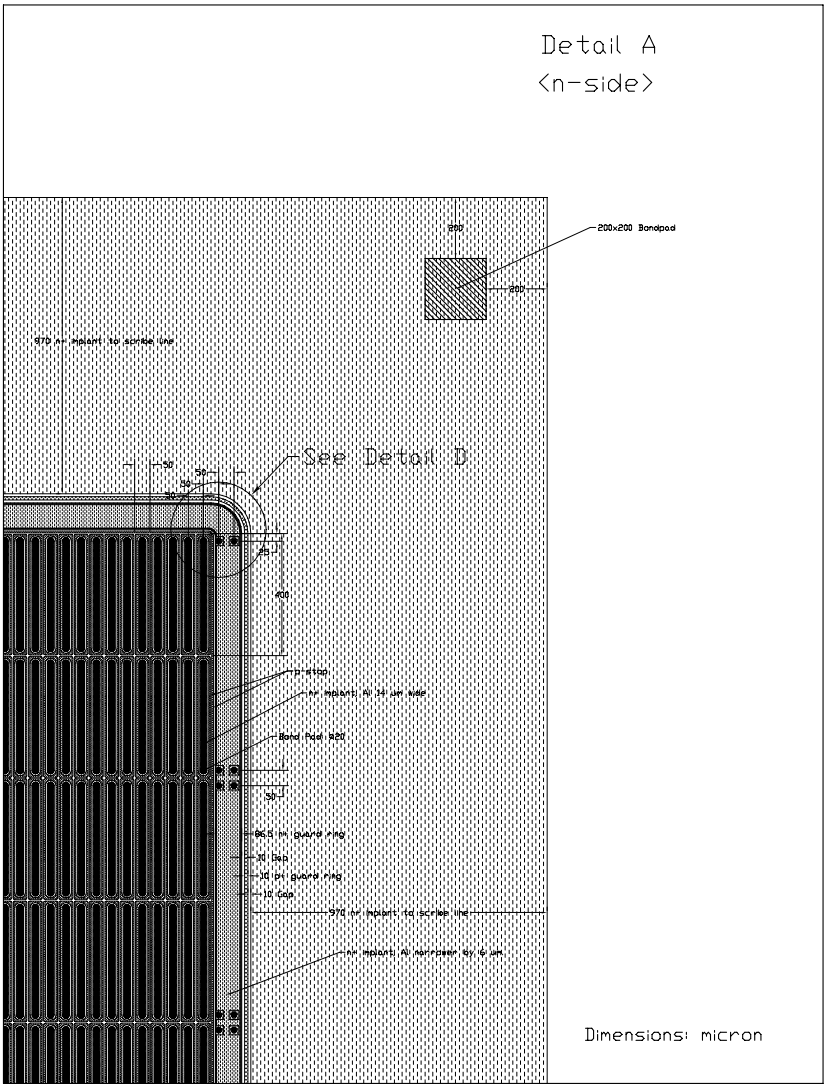

Figure 2a: Corner detail of Tile 1.

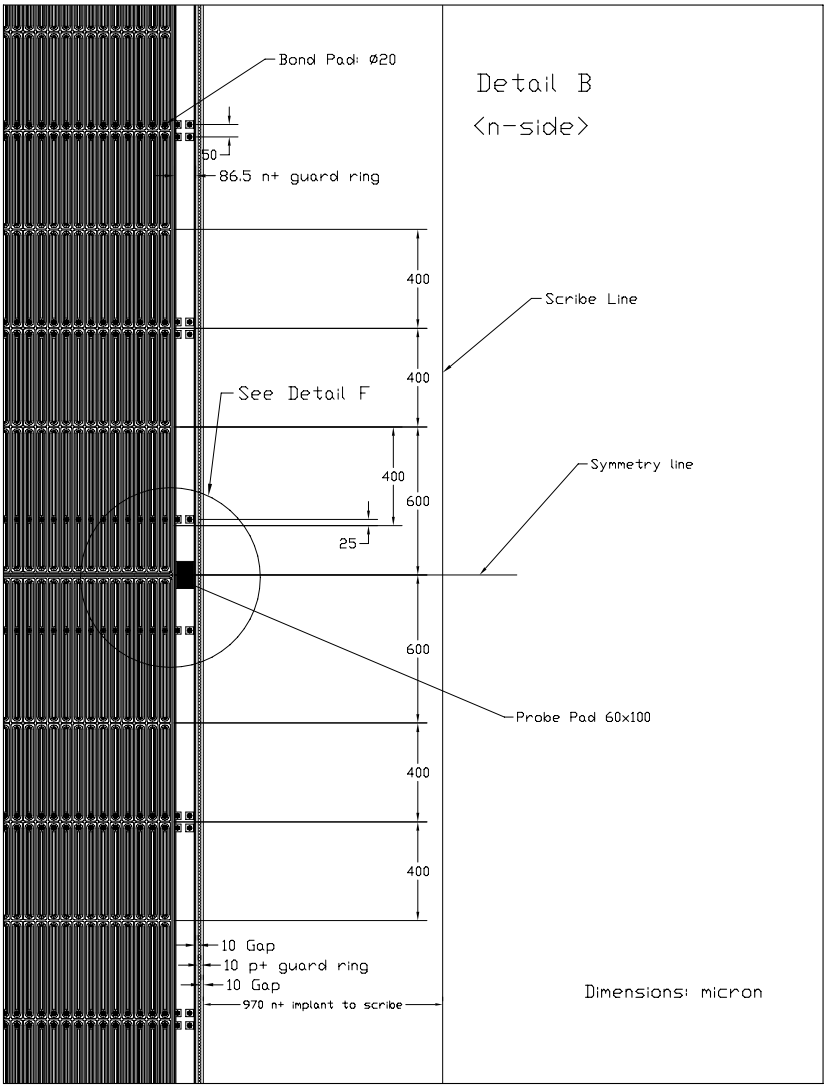

Figure 2b: Detail of Tile 1 showing a region between units in which cells of length 600 μm are used.

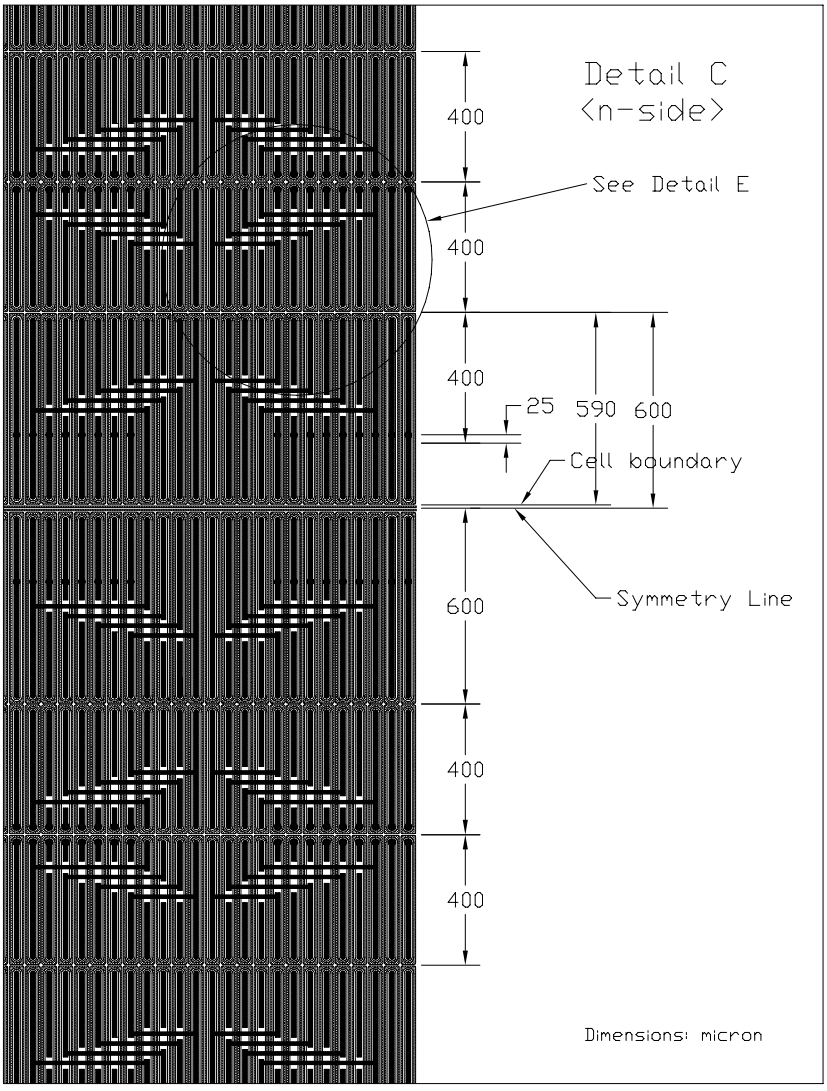

Figure 2c: Detail of Tile 1 showing first metal traces which route signals from implants at the edges of their units to the preamplifers above neighboring implants.

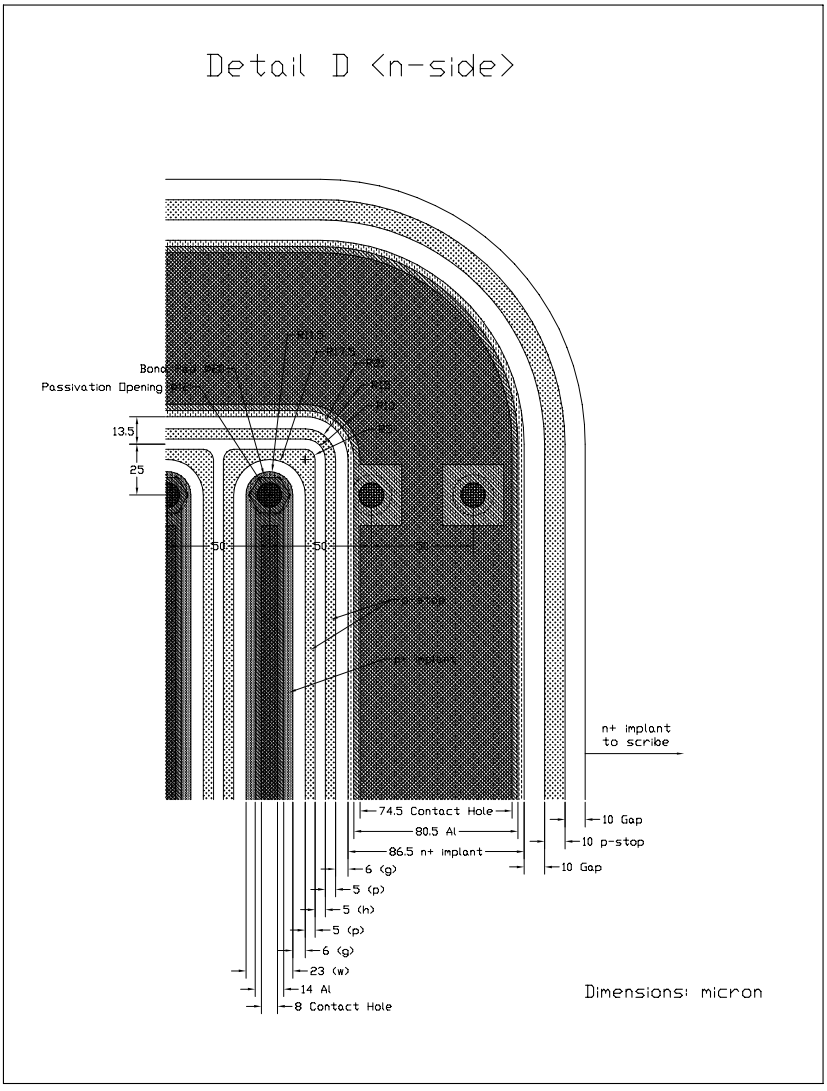

Figure 2d: Detail of Tile 1 showing the corner of the n-side guard ring and the isolation implants.

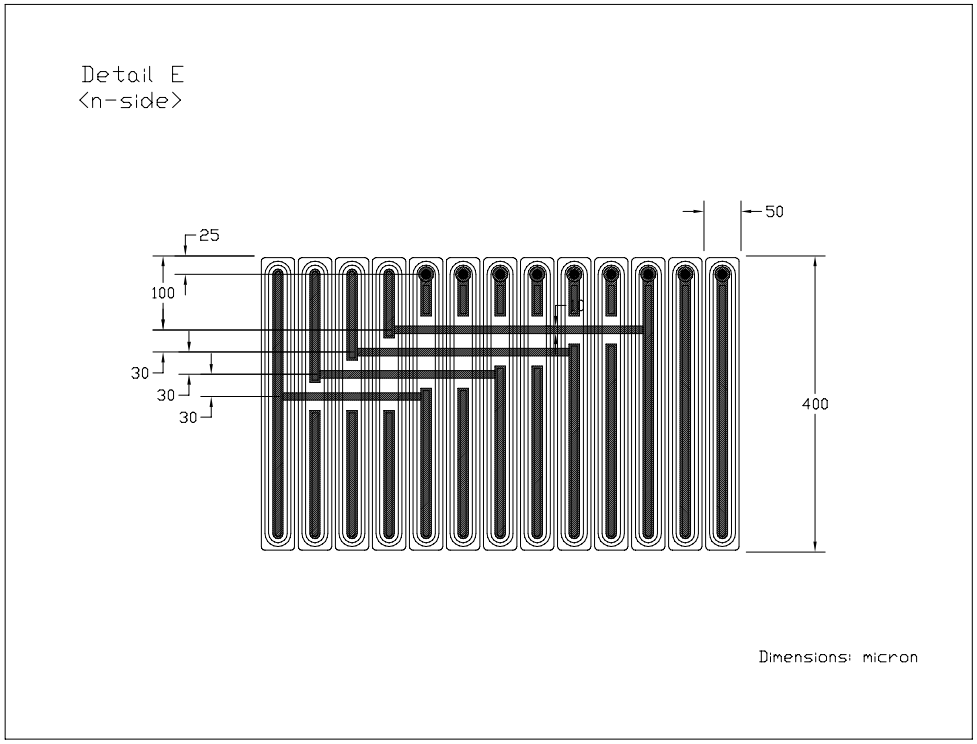

Figure 2e: Detail of Tile 1 showing the first metal near the edge of a unit.

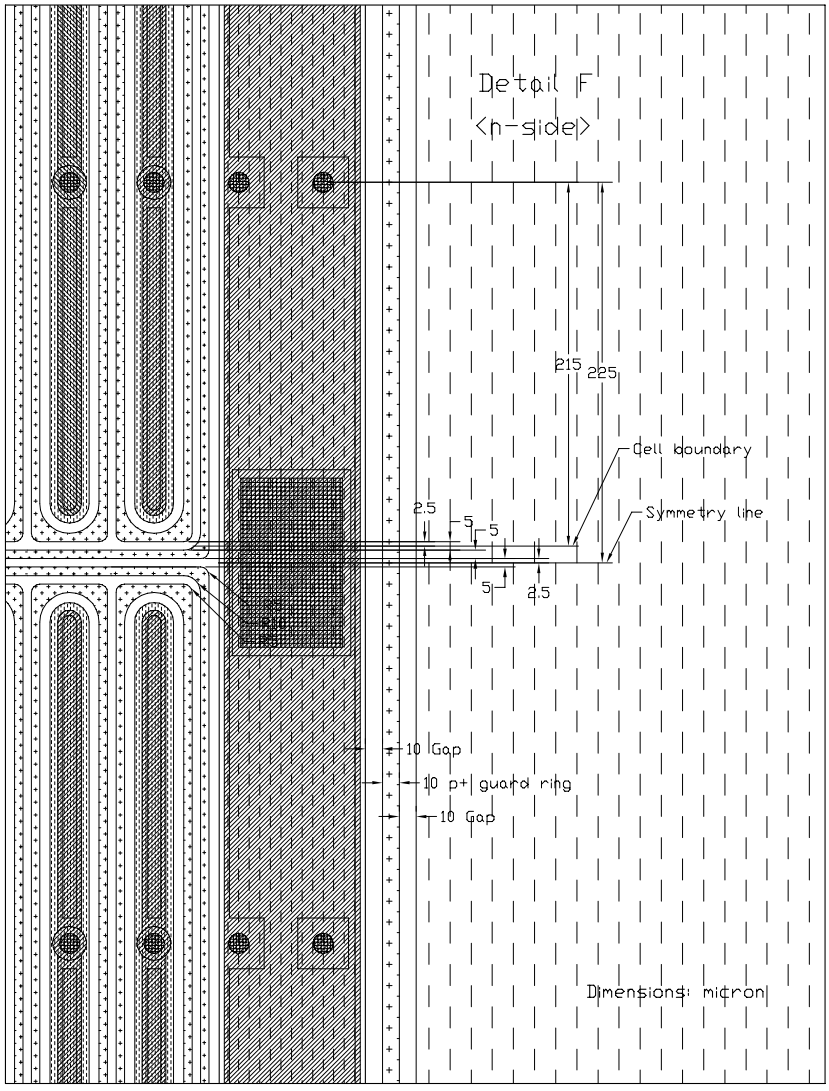

Figure 2f: Detail of Tile 1 showing the structure of isolation implants at the boundary between units.

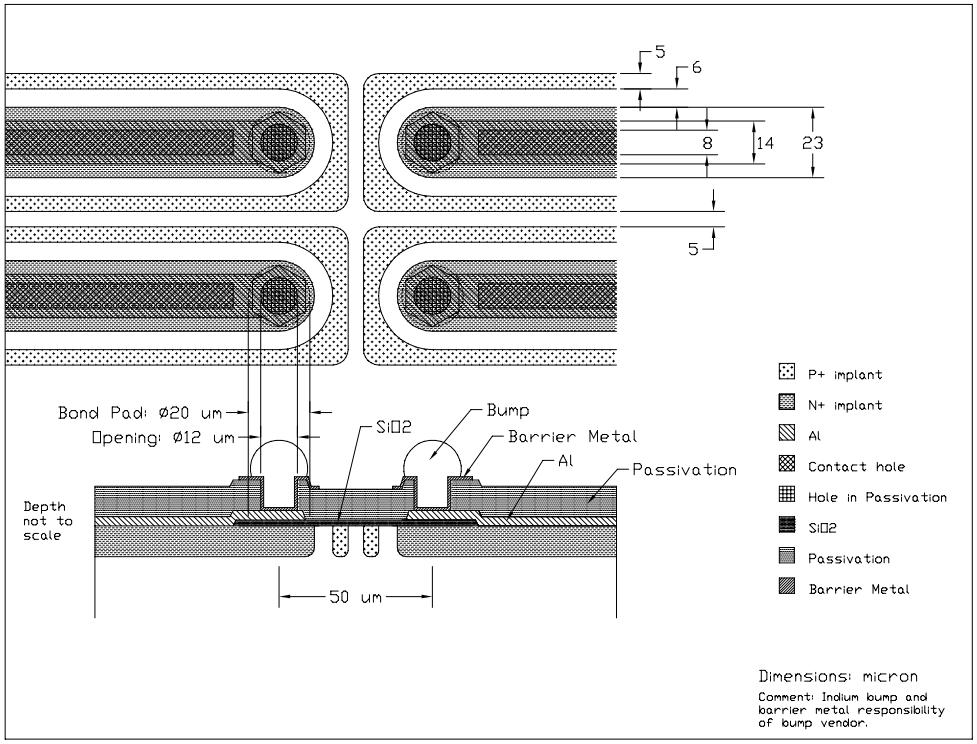

Figure 3: Concept of a Tile 1 bond pad region.

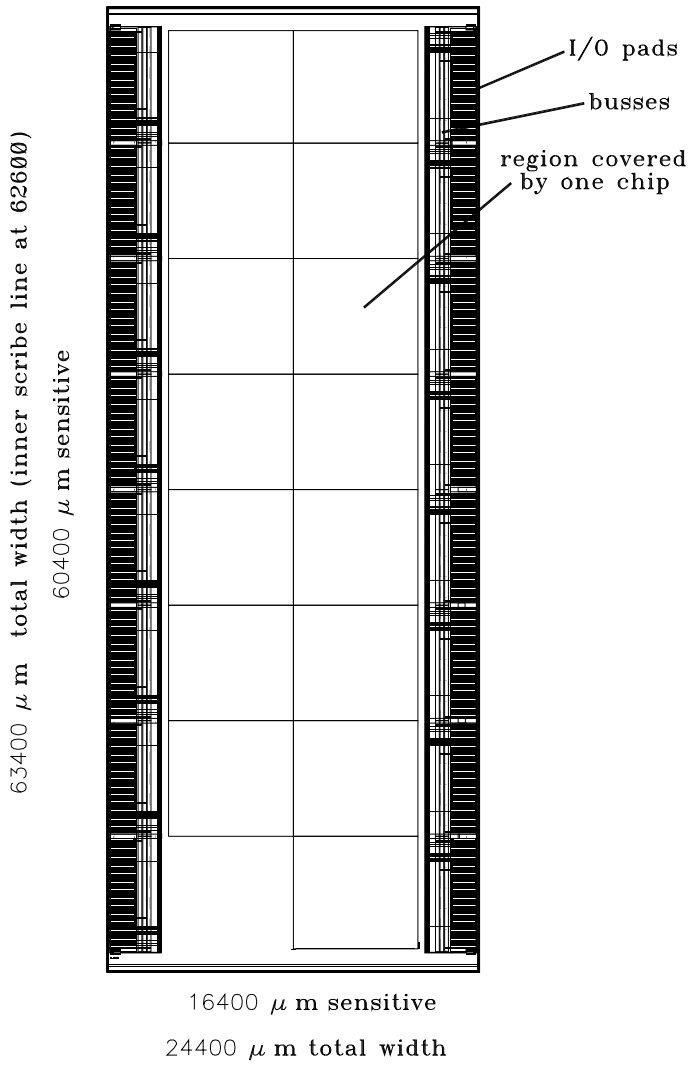

Figure 4: The Tile 2 concept.

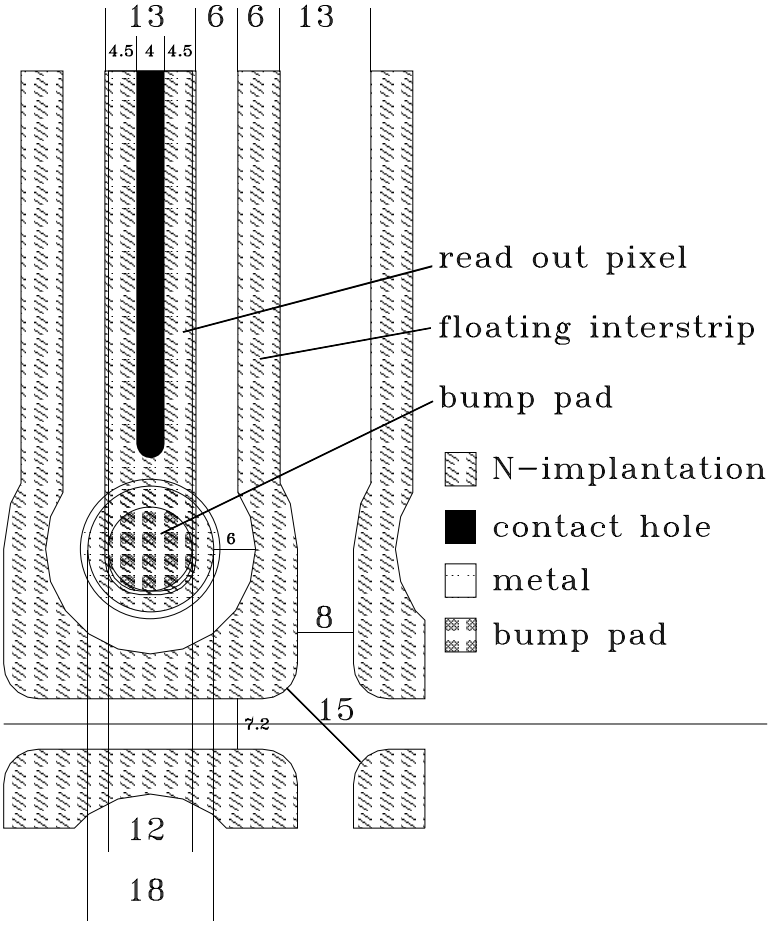

Figure 4a: Portion of a pixel cell in Tile 2.

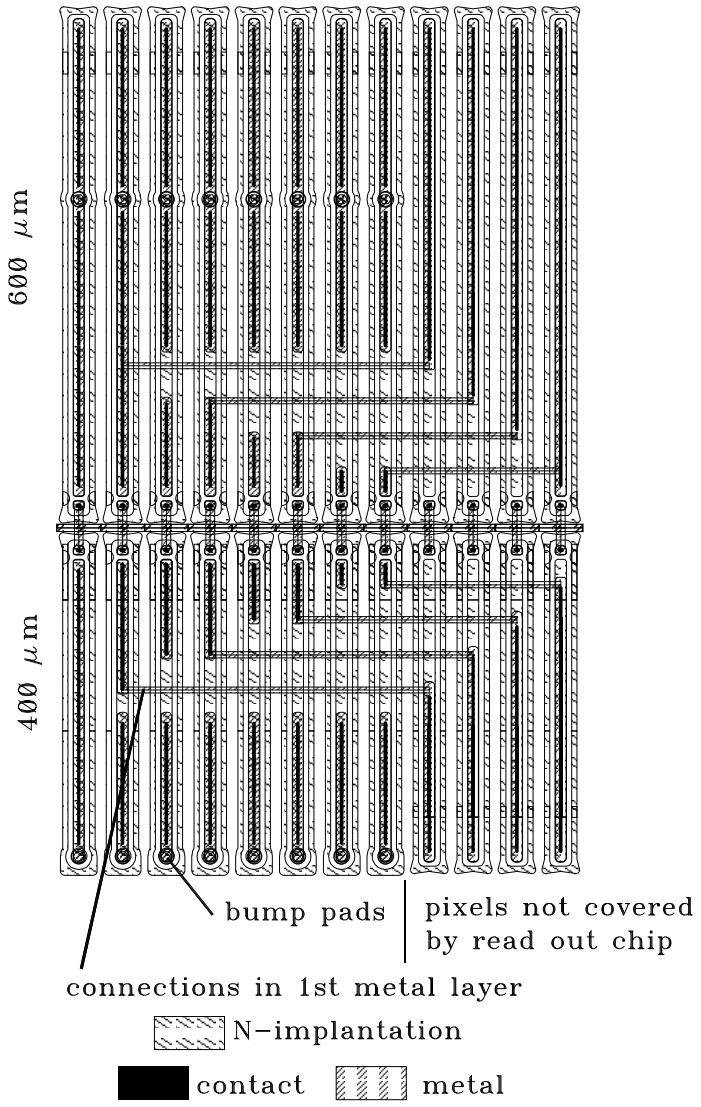

Figure 4b: Detail of Tile 2 showing first metal traces which route signals from implants at the edges of their units to the preamplifers above neighboring implants.

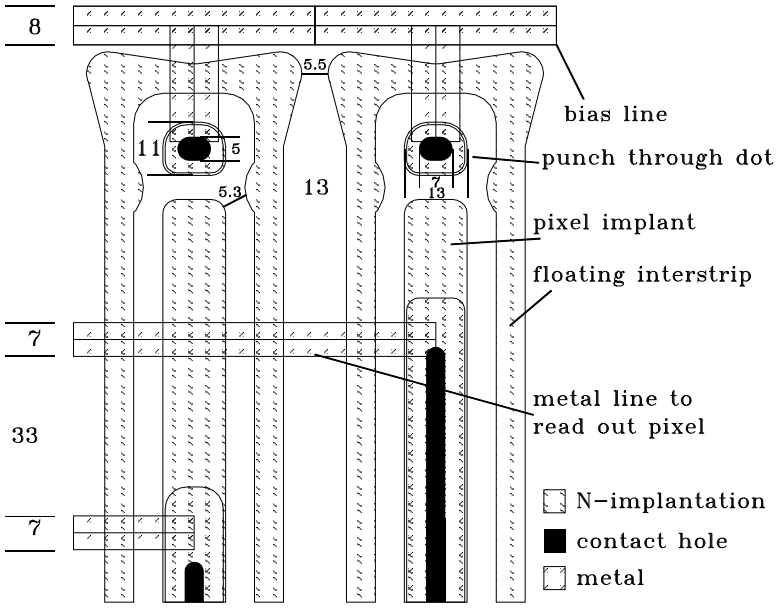

Figure 4c: Section of the Tile 2 multiplexing scheme.

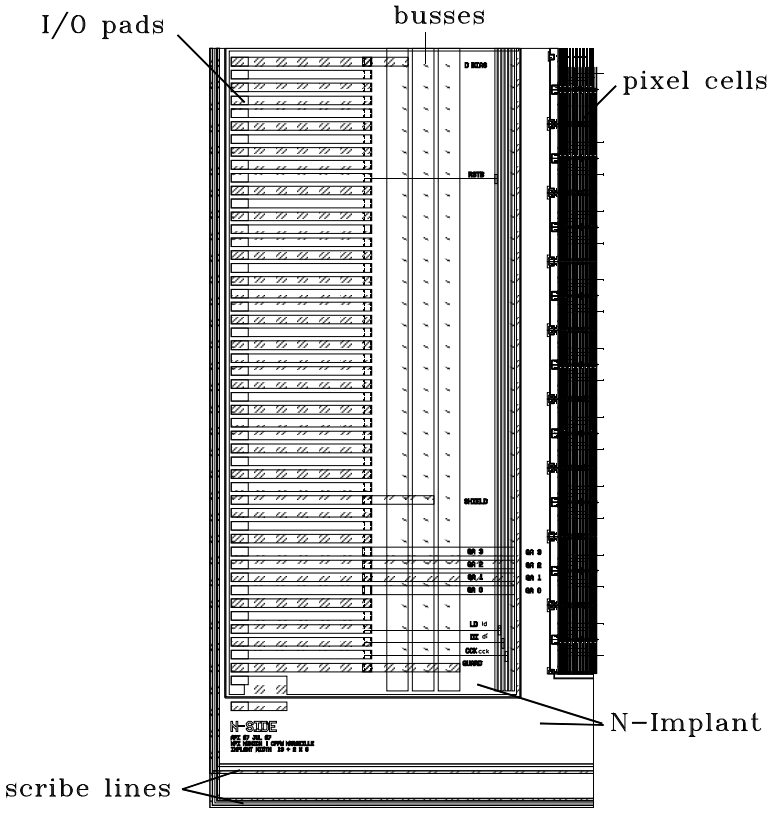

Figure 5: I/O busses on Tile 2.

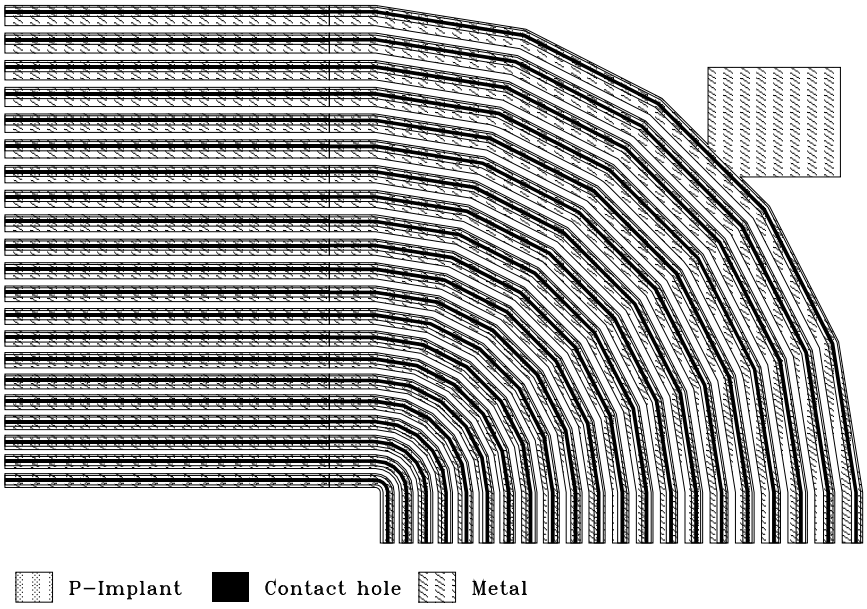

Figure 6: The p-side guard ring.

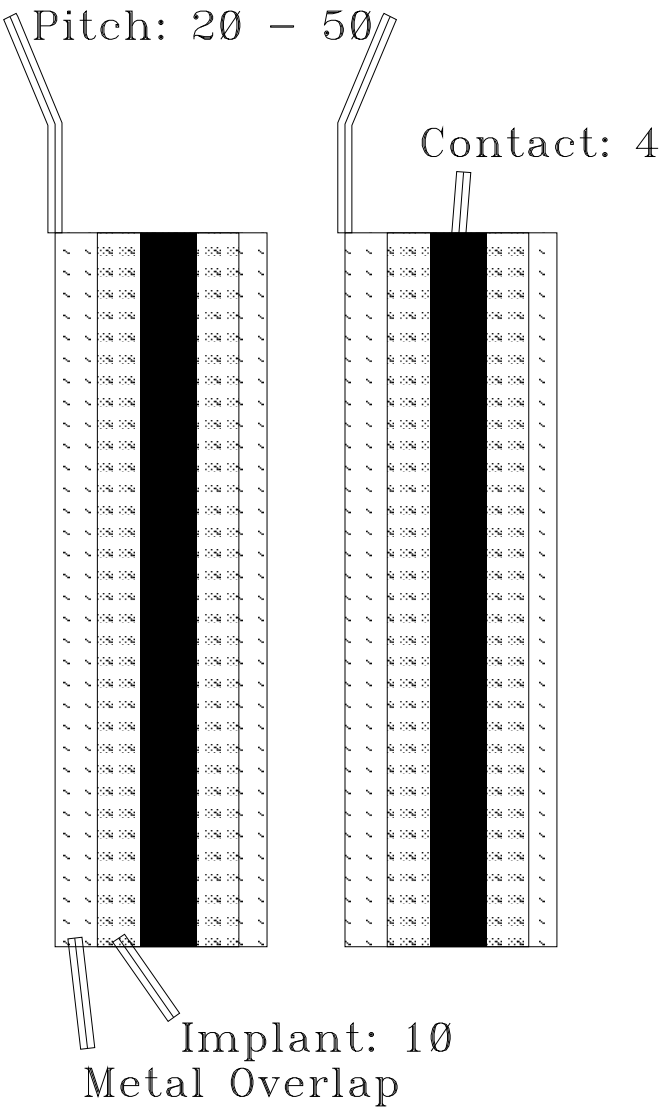

Figure 6a: Detail of the p-side guard ring.

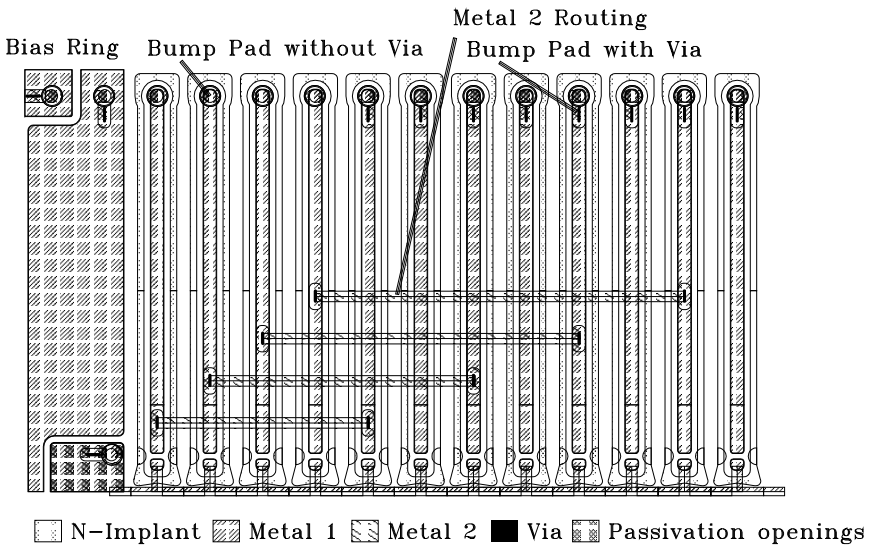

Figure 7: The Metal 2 routing.

References

[1] The ATLAS Collaboration, *ATLAS Inner Detector Technical Design Report*, CERN/LHCC/97-17, April 1997.

[2] T. Rohe et al., *Sensor Design for the ATLAS-Pixel Detector*, Proc. Seventh Pisa Meeting on Advanced Detectors, Isola d'Elba, May 1997, submitted to *Nucl. Instr. and Meth.*

[3] A. Bischoff et al., *Nucl. Instr. and Meth.* A 326 (1993) 27-37; B.S. Avset, *Nucl. Instr. and Meth.* A 377 (1996) 397-403.