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The ADAM CHIP

Specification and Measurement Results

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The first prototype of an integrated Front-End readout chip for the silicon tracker of the ATLAS Inner Detector for the LHC at CERN, the ADAM chip, has been fabricated and tested with a probe station for its direct performance and general functionality and with a full test bench laboratory set up using a data acquisition system. The chip integrates the NICON pre-amplifier, the DHARP analog pipeline of 32 channels by 112 cells deep memory, the CRIAD Analog to Digital Converter, the digital read-out memory, and associated control logic. Sophisticated tests have been made to access its functionality and feasibility of performance at the 40 MHz bunch crossing speed of the LHC.

We measure a sensitivity of over 20 mV per 4 fC of injected charge[1] with an rms noise of less than 1.8 mV. The resolution of two closely separated signals is 25 ns, which is the LHC bunch crossing clock.

[1] The injected charge of 4 mV on 1 pF load capacitance was used as one MIP signal.

1. The ADAM Chip

1.1 The ADAM chip for the ATLAS Inner Detector

The ADAM[2] chip has been designed and fabricated as a prototype for the Front End readout electronics of the ATLAS[1] inner detector at the LHC. With high energy and luminosity the LHC offers a large range of new physics opportunities. One important requirement of the inner detector is efficient tracking at a high luminosity for lepton momentum measurements and for electron and photon identification. The very high track detection at LHC, with the requirement of good momentum resolution, demands for the use of high-granularity detectors. Those requirements are satisfied by the use of semiconductor (Si or GaAs) detectors. The associated readout electronics is extremely dense, and because of the LHC bunch spacing, it must be very fast.

The performance specification for the inner detector readout electronics demands low noise (<1500 electrons equivalent noise charge), low power consumption, high signal to noise ratio, operation at an interaction rate at 40 MHz, operation with a 2 μs level 1 trigger latency, and an event acceptance rate up to 100 kHz. The inner detector will have over 2 million channels of readout and it require to have minimum material to reduce the material volume in the tracking media. It also require low power dissipation per unit readout within the tracker volume for cooling reasons.

The ADAM chip has been designed to satisfy those requirements, and the specification and performance results are presented in this note.

1.2 The Architecture of ADAM

The architecture of the ADAM is an integration of various components which have been individually developed and tested. The ADAM chip is composed of:

- Front-End Amplifier; NICON,
- Analog signal pipeline memory; DHARP,
- Analog pipeline control logic; APC3,
- Analog to Digital Converter; CRIAD,
- Digital buffer for Readout; OFIFO,
- Readout Logic for digital buffer; ROL, and
- General chip control logic, CCL.

The architecture schematics of the ADAM chip is shown in figure 1.1. With exception of sparsed data readout, the architecture contains all the components required for digital readout at LHC. Of particular interest in this architecture is the inclusion of on-chip of analog memory, digital control, and digitization functions.

- [2]Atlas Detector Analog Memory.

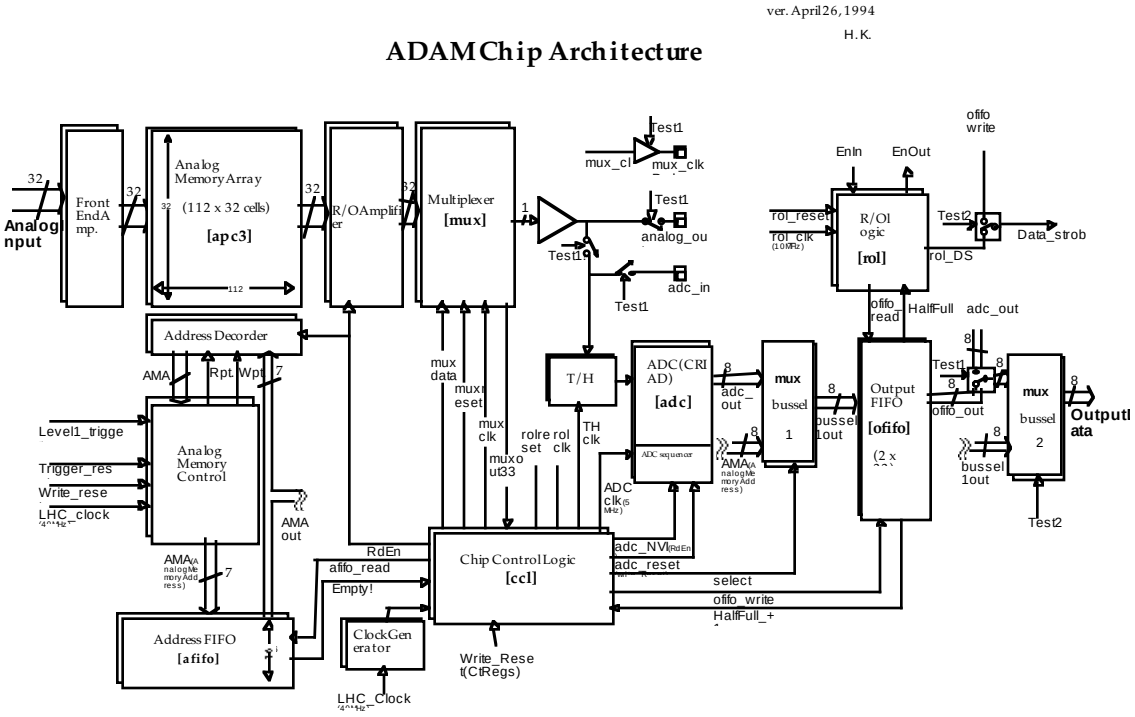


Figure 1.1: ADAM Chip Architecture.

The chip has been designed and simulated with Verilog[2]simulation software and verified its digital functionality. A brief description of each component is presented in following sections[3].

1.3 NICON

The previous version of the ICON[3] Front-End amplifier has been improved to operate at a 3 GHz gain-bandwidth current mode amplifier stage, NICON (see Figure 1.2) for this integrated chip. The n-MOSFET M1 channel input is a grounded gate transistor of size W/L=1500µm/1.5µm and operates in the weak inversion region, at a drain current Id ≤ 80µA. The cascode MOSFET M2 n-channel conveys the input current on the integrating output node. The output node bias voltage is stabilized to Vref by the slow amplifier *A* which does the stabilization by controlling the current *I* comp source. This technique offers the advantage to compensate the effect of the detector dark current in case of DC input connection. The NICON circuit has been fabricated in a 1.5 µm double poly, double metal CMOS process.

Figure 1.2: The Cascoded Grounded Gate amplifier (NICON)

A rise time (10 - 90%) of 13 ns is measured with an 8 pF input capacitance. The peak amplitude is 42 mV for 25000 electrons at the input, equivalent to a MIP signal. The power consumption of the circuit is measured as low as 400 µW.

3 For complete description of the individual components, see [3]

1.4 DHARP

Figure 1.3: Simplified schematic of DHARP.

The analog memory is configured to provide the necessary shaping function after the NICON Front-End amplifier. The shaping is performed during the readout process by a correlated double sampling technique (CDS). The basic diagram of the analog memory with CDS is shown in figure 1.3. Two consecutive voltage samples V1 and V2 of the NICON output are stored in the two capacitors C1 and C2 of one memory cell. The first experimental DHARP chip contained 64 cells per channel. A second version of the DHARP (DHARP2) was designed with 112 cells. The LHC requirement of at least 2μs trigger latency corresponds to 80 cells, or time columns, with 40 MHz clock. The ADAM was fabricated with 112 time columns to satisfy this 2 μs latency, plus 32 cells of memory to hold any incoming triggers with minimum dead time.

The clocking scheme is such that all cells are periodically re-addressed. A particular cell can be protected against further sampling, when it is marked by the positive level 1 Trigger signal. At read out the two capacitors of two different cell are connected to the inputs of a differential readout amplifier. The output of the amplifier represents the voltage difference between the two consecutive samples. The differentiation process (shaping) is thus performed with a shaping time equal to the interval between two samples (25ns). The differentiation being done by the simultaneous readout of two consecutive samples, a good rejection of parasitic common mode noise (from substrate, clock lines or power supplies) is expected.

The DHARP2 circuit with 32 channels of 112 cells has been fabricated and tested. The chip is fully functional at 40 MHz sampling rate[4]. The measured signal amplitude and the noise performance did not reach the full specification values because of mismatch in DC levels and a asymmetric structure in the implementation of two capacitors at the inputs of the readout amplifier. These problems are now identified and we expect the corrected version to provide an analog performance following the pipeline in accordance with these measured on the NICON prototype.

The characterization shows that the full signal is contained in one readout sample, with a power consumption per channel of less than 2 mW; the common mode noise at the output is 1.5 mV rms. and the offset variation from capacitor to capacitor is 2 mV rm.'s.

1.5 CRIAD

The CRIAD[5] ADC consists of a 6 bit ADC with 2 bits of segment specification. The consequent 64 non-linear segments of ADC covers 2048 mV of range. The first segment has resolution of 1 mV, covering 64 mV of range, second with 2 mV resolution for 128 mV range, third with 8 mV resolution for 512 mV, and the last segment with 32 mV resolution covers 2048 mV. The ADC takes the sampling first with the flash part to determine the input range of the signal and process the digitization with appropriate segment.

The architecture (see figure 1.4) consists of one track & hold (T&H) and a two-step analog-to-digital converter. During the first step, a 2-bit flash nonlinear conversion is performed. The dynamic range is divided into four unequal parts by a resistor string: R-R-6R-24R. This allows a determination of the corresponding range (segmentation) of the input signal. The second step is

performed by a 6-bit linear charge-redistribution ADC in the range previously indicated by the 2-bit flash converter.

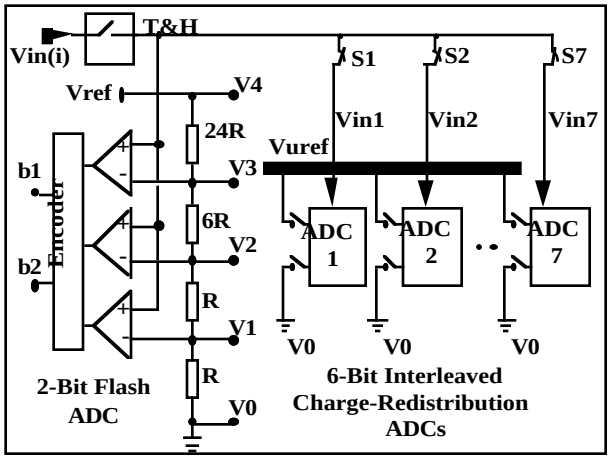


Figure 1.4: Architecture of the piece wise linear ADC

In order to reach the required data throughput of the system, seven time-interleaved charge-redistribution A/D (ADC 1 to 7 on figure 1.4) converters are needed behind the FADC. Each ADC makes a comparison decision each clock cycle, and requires 7 clock cycles (1 clock cycle for sampling and 6 clock cycles for 6-bit digitization). This architecture provides a full 8-bit digitized output at each clock cycle. 2 bits indicate the range value, the 6 last bits are the conversion outputs.

Table 1.5: CRIAD experimental results.

Characteristics	Value
Max. Resolution	8 bits piecewise linear (11-bits effective)
Sampling rate	5 MHz
Differential Non-Linearity	± 0.5 LSB
Integral Non-Linearity	± 0.5 LSB
Input Range	0 to -2.048 V
Power Supply	± 2.5 V
Power consumption	25 mW
Active area	5 mm2
Technology	1.5 µm CMOS

The CRIAD has been fabricated and fully tested[6], and table 1.5 summarizes the results. Figure 1.6 shows a 6 KHz, sinusoidal signal with 800 mV amplitude, reconstructed from the digital outputs of the ADC running at 5 Msamples/sec with the flash part operating and automatic segment switching. The variation of the quantification step depends automatically on the signal amplitude that is observed, or can be manually fixed.

Figure 1.6: Output code for a 800 mV amplitude.

The CRIAD structure, implemented in the ADAM chip, allows a full characterization of the analog performance, including noise, pedestals and dynamic range. If a 6 bit dynamic range is sufficient in the readout of a tracker at LHC, the flash part can removed from the final electronics implementation with a consequent reduction in power consumption.

1.6 APC3 Logic and Pipeline Address

An APC3[7] chip was designed to integrate the digital logic necessary to retrieve the data from a level 1 trigger. It was fabricated at the beginning of 1993 and tested during the remainder of that year both at RAL and at CERN. The chip consists of an analog section containing the pre-amplifiers, an analog memory array, and a multiplexer and a digital section with the memory management logic that is common to all channels. The major components of this logic are shown in figure 1.7.

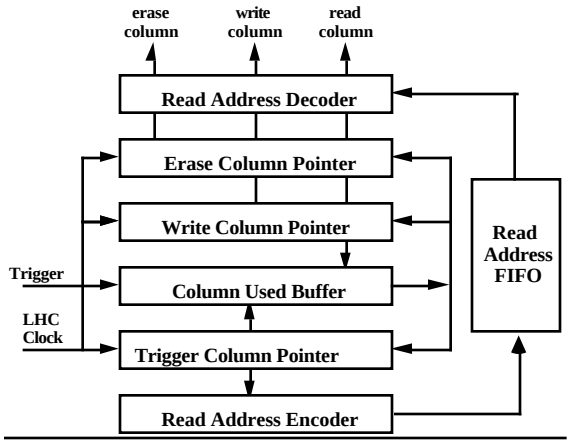


Figure 1.7: Memory management logic in PAC-3 chip

The functionality of the digital logic was tested at 66 MHz using a HP82000 200 MHz digital IC tester at RAL. Then extensive measurements of the chip's analog performance were made using a VME based data acquisition system. All measurements were performed using continuous write and read operations, with a write frequency of 40 MHz and a read frequency of 5 MHz.

Address Progression

The address of the analog memory is readout by APC3 logic control[4]. In the initial prototype version of PAC logic, the write and read pointers progress along the analog memory in the order of physical layout. At the end of the pipeline cell, the pointers will be returned to the first cell of the memory. This jumping logic at the end of the pipeline caused unstable pedestal and high noise immediately after the jump of the pointers. For integration within ADAM, a modification was developed and applied in this chip. The write and read pointers will progress in non-linear order with groups of 4 time slots as shown in Figure 1.8.

[4] David Campbell, RAL.

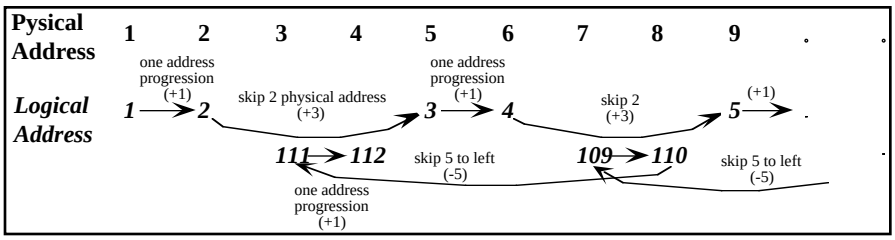


FIGURE 1.8: the APC3 new logic for address pointers.

1.7 ADAM Chip Specifications

Below in figure 1.9 shows the floor plan of the ADAM chip, and table 1.10 shows the specification of the ADAM chip.

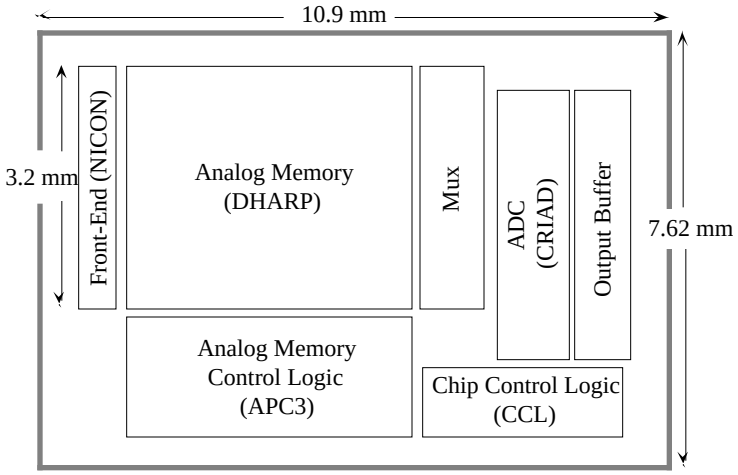


FIGURE 1.9: ADAM floor plan. Components are drawn to approximately proportional size.

TABLE 1.10: specification of the ADAM.

2. The ADAM Test Setup

The Adam Test Setup is a stand alone system to characterize the ADAM chip with its full functionality. The setup consists of three main components; the ADAM chip on the "piggy back board", the Adam Testing Board, and Test Board Controller. The plan over view of the test bench set up is shown in Figure 2.1.

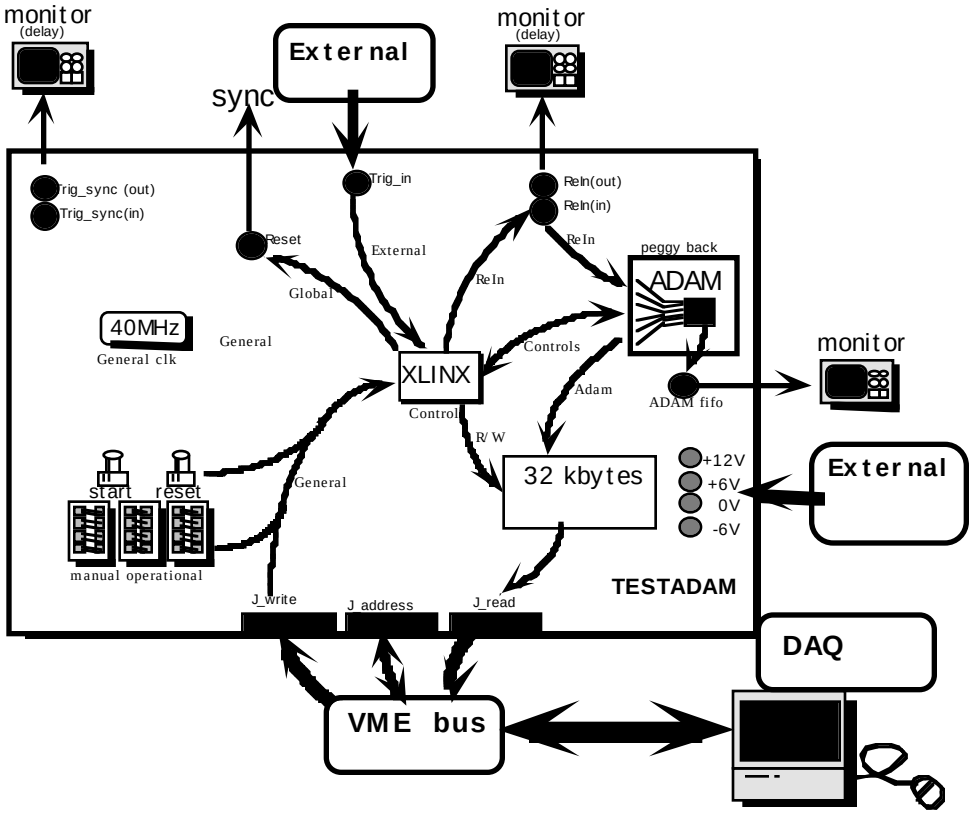


Figure 2.1: ADAM Test Setup.

2.1 The ADAM Test board

We have built an electronic circuit board providing an interface to the ADAM chip, the TESTADAM_DPNC-158, developed at University of Geneva[5]. The board allows the ADAM chip to operate either manually or from DAQ system via a VME interface. The manual operation permits the board to operate without a VME interfaced DAQ system, which is useful to study the functionality of the ADAM at a probe station. An appropriate card has been developed to probe the chips under test.

[5] Annie Leger, University of Geneva.

The ADAM test board generates a 40 MHz clock and synchronizes the external signals before they are sent to the ADAM chip. The on-board generator also supplies the master 40 MHz clock of the chip.

The board uses XLINX programmable logic to control its operation. The XLINX can be programmed from an external source to verify the operation of the board logic, or charged with fixed logic on board. In normal testing operation at the test bench, the XLINX logic is read from on-board memory at the time of power turn-on. However, this can be changed or monitored with on-line analysis software for studying further functionality and performance of either the board or the ADAM chip.

ADAM Test board Sequence

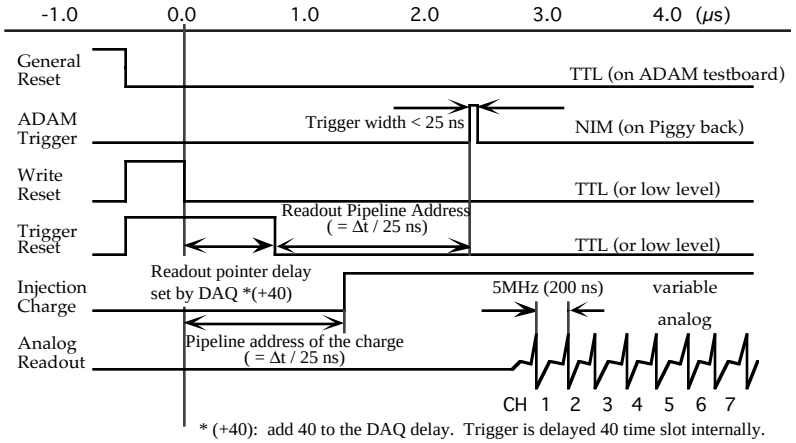
The ADAM test board with its programmable control interfaces via the VME data transfer bus and a 32k output data buffer, providing various options for the operational mode of the ADAM chip. The control logic of the XLINX reads the operation mode and sends the specification and control sequence to the ADAM chip. The logic sequence is:

0). Global reset.
1). Waits for the start signal.
2). Reset the memory bus and send a reset to ADAM.
3). Sends end-of-reset flag.
4). Trigger waiting, then send it to ADAM.
5). Store the data in the on-board memory and wait for the end-of-block from ADAM.
6). Go back to (1) if no data transfer is specified.
7). Transfer the data from the on-board memory to the VME bus.
8). Wait for the end-of-data flag from the memory.
9). Go back to (0) for manual operation, (1) for auto operation with reset, (4) for auto operation without resetting.

Analog Memory Control Sequence

With the DAQ system on the laboratory test bench setup, the control signals are sent via a VME bus. The LabView software was used to develop the control sequence on the Macintosh computer.

Figure 2.3 shows the various timings of I/O signals to the ADAM chip. The DAQ system has the flexibility of changing the timings of various control signals to study the ADAM chip with precise timings.



* (+40): add 40 to the DAQ delay. Trigger is delayed 40 time slot internally.

FIGURE 2.3: Timings of the control and output signals to the ADAM chip.

The ADAM analog memory control sequence proceeds as follows. First, the general reset signal is sent from DAQ via VME to start the cycle of the data acquisition. The ADAM test board received this signal and sends the Trigger Reset to the ADAM synchronized with general 40 MHz clock. Immediately after the Write Reset signal is sent, the write pointer (APC3) logic on the ADAM will start writing the data into the analog pipeline (DHARP). With the delay set by DAQ, the ADAM test board will release the Trigger Reset which starts the read pointer (APC3), progressing parallel with the write pointer. The APC3 logic was designed such that the write pointer and read pointer will have 40 Time Slot of delay (25 ns for one time slot) if the write-read delay is set to zero via DAQ.

The readout sequence is triggered by sending an external trigger to the ADAM chip. The Trigger width should not be longer than one time slot length (25 ns). A trigger over 25 ns will invoke the second readout sequence. The delay between the trigger reset and the external trigger will determine the read out time column of the analog pipeline. The delay between the write reset and injection charge will determine the address of the pipeline in which the injected charge is written to the ADAM analog memory array.

We hope to reduce the pointer location dependent noise in the ADAM chip. The result of the noise depending on the address pointer location will be presented in the following section.

2.2 The Piggy Back

The ADAM chip is bonded onto a separate board directly with charge injection capacitance. This board plugs directly onto the ADAM testing board. This method, the "piggy back board", has been adapted for the ADAM testing bench to minimize any external noise and parallel capacitance which can be caused by using an extra socket to mount the chip to the system. Figure 2.2 shows the connection map of this Piggy Back interface to the ADAM testing mother board.

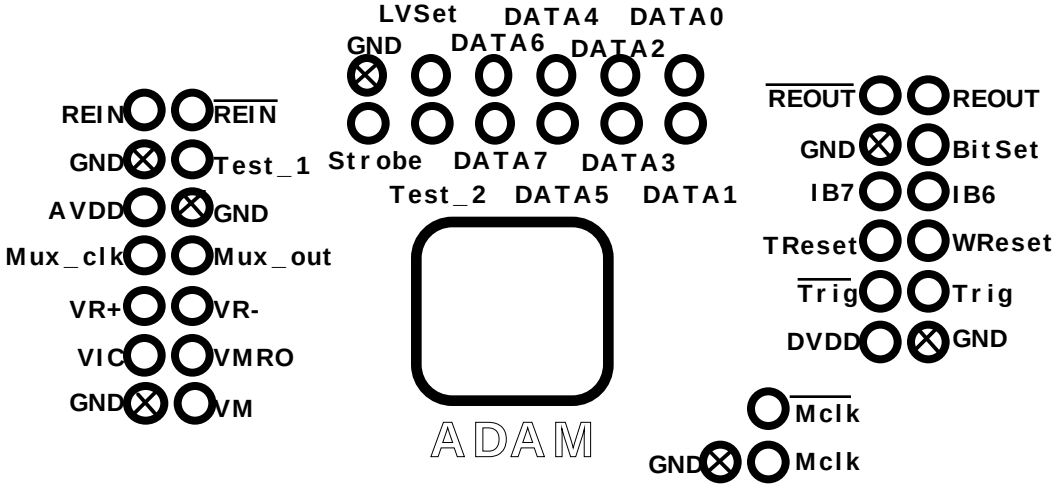


FIGURE 2.2: Piggy back board interface pin connection layout

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The direct input/output signals from the ADAM chip can be probed from the piggy back board.

2.3 DAQ Systems

A DAQ software with LabView using a Macintosh computer has been developed within the RD2 collaboration[6]. It manages the control sequence to the ADAM test bench, collects the data from ADAM test board, and analyzes the data on line.

The module sends I/O control signals through the VME bus which manages the data transfer from the chip. The reset and trigger signals require a precise timing and they are generated with an external pulse generator, controlled by a GPIB bus. The user interface software sends control sequences for those signals to the generator, and the signal generation is triggered directly from the ADAM test board.

The data which is collected in the on-board memory of the ADAM test board is transferred via VME bus to the on-line analysis system. The basic tasks for the on-line DAQ consists of a pedestal and noise analysis, a study of analog memory structures, monitoring raw data, and data storage for later off-line analysis, etc.

Furthermore 8 of the ADAM chips connected in parallel with readout bus is tested in the test beam environment, using Read Out Controller (ROC) module, linked with optical fiber cable to the DAQ system[7]. The ROC can receive the master clock and trigger signals from two optical links and broadcasts them to the 8 chips on board. In this test beam setup, the detector boards are isolated from the DAC electronics. In principle the clock, trigger, and control information could be send to each ROC via a single optical, though this is not planned at this stage of the development.

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[6] A flexible DAQ software, Gollum, developed by R. Bonino, is used.

[7] For further information of the ADAM test beam, refer,
http://atlasinfo.cern.ch/Atlas/GROUPS/INNER_DETECTOR/SCTstrips/OTP/OTP.book_1.html

3. Measurement Results of ADAM chip

In this section, some basic measurement results of the ADAM chip characterization are presented. The analog pipeline, pedestal, noise, and baseline have been studied in detail. We present the overall ADAM chip performance, and the performance of the separate components.

3.1 CRIAD Measurement Results

The CRIAD is used as the Analog to Digital Converter (ADC) in the ADAM chip. As noted previously, this component was designed and fabricated for individual testing in previous development, and the detailed functionality has been measured[6]. The ADAM can be operated in a test mode such that the CRIAD can be tested individually with its analog input signal and direct digitized output. The CRIAD functionality was as expected from the previous measurements.

Non-Linearity Measurement

A Least Significant Bit (LSB) is defined as the range of the ADC divided by the number of ADC bins[8]. The width of all bins are ideally equal, and also equal to one LSB. However, the real ADC dynamics will not be perfect, generating non-linearity in the response. The Differential Non-Linearity (DNL) is defined as the difference between the measured bin width of an ADC and the theoretical width, or one LSB. The DNL is measured for all bins. The maximum value of the DNL is used to evaluate the performance of the ADC. The Integral Non-Linearity (INL) for a given bin n is calculated by summing the DNL from the first bin to the *n*th bin:

$$INL(n) = \sum_{i=0}^{n} DNL(i) \quad . \qquad (1)$$

As with DNL, INL is calculated for all bins of the ADC and the maximum value is normally taken for the evaluation of the ADC performance. Figure 3.1 shows the measurement of non-linearity for the CRIAD as implanted in the ADAM chip, and running at 5MHz clock speed.

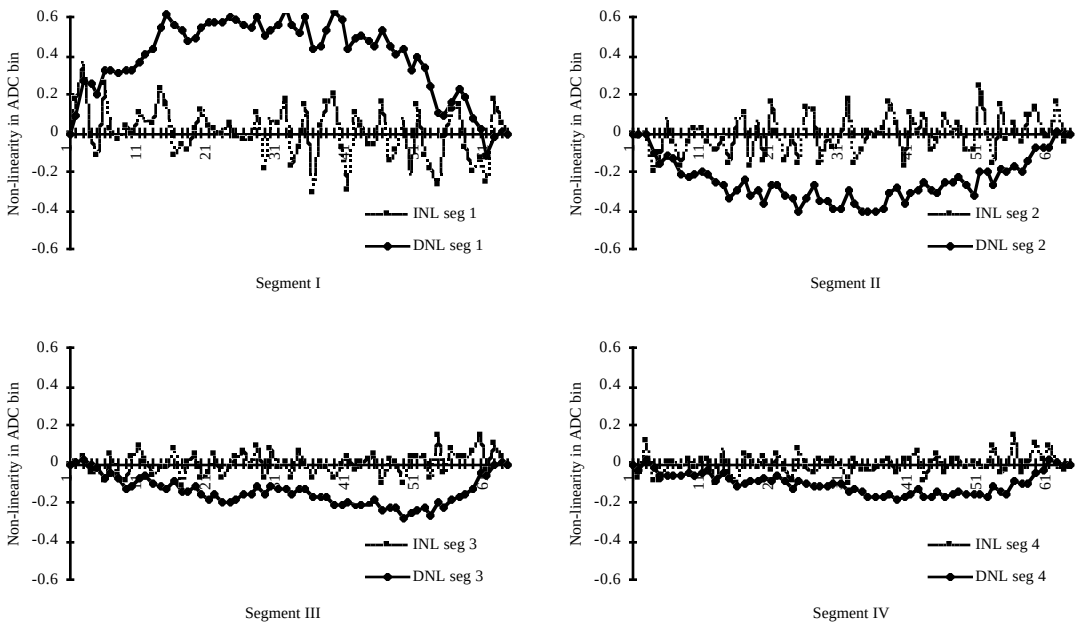


FIGURE 3.1: Non-linearity measurement of the CRIAD in the ADAM.

The Table 3.2 presents the maximum values of non-linearity of the CRIAD, extracted from above figure.

TABLE 3.2: Non-linearity of the CRIAD.

3.2 The Baseline—Time Column Dependent Pedestal

The analog pipeline with HARP technology has been installed in the ADAM chip and it is important to understand the pedestal fluctuation of this analog memory array. The known problem from the last version of the pipeline, the DHARP2 [4] , was the baseline fluctuation where all 32 input channels had the same pedestal structure, but with a common offset fluctuation. The major cause of this fluctuation was determined to be from internal cross-talk and/or analog pick-up at the input amplifier. Further study is necessary to solve this problem completely. This baseline is the average value of 32 channels for each event with null signal and it is calculated by off-line software and subtracted for each event. Hence the fluctuation can be suppressed by off-line even though the direct cause is not completely determined. In the ADAM measurements we found that a major part of this baseline fluctuation is from the time column dependent pedestal shift and it comes from the Front-End amplifier (NICON) pick up. The time column dependent pedestal shift is only observed when the pedestal measurement was taken together with the Front-End amplifier.

Pedestal with NICON amplifier

Figure 3.3 shows the pedestal of one channel for all 112 time columns, with full functionality of the ADAM chip. The analog pipeline is fed by the Front-End amplifier, with null signal input. No baseline subtraction is made. The plotted time column number corresponds to the logical (as read out) address of the analog memory.

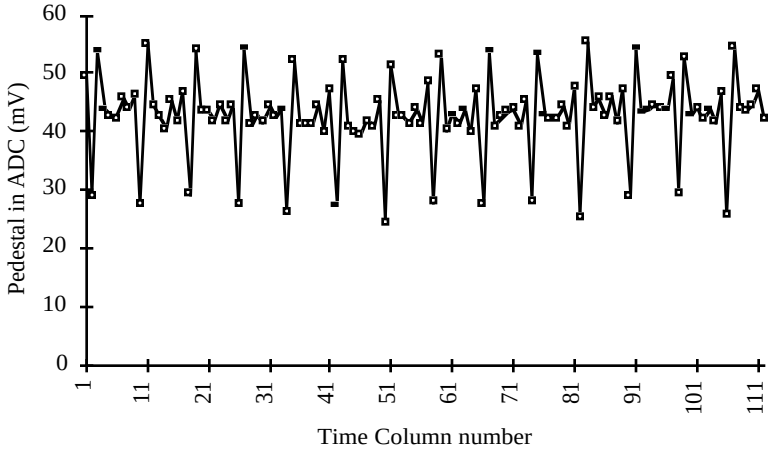


FIGURE 3.3: Pedestal for all 112 Time slot on Channel 8, no baseline subtraction, with NICON.

A time column dependent repeated pattern of the pedestal structure is observed from this figure. The structure consists of group of 8 logical addresses: one low cell at ~30, one high cell ~50, and 6 consecutive cells at middle range ~40. The corresponding noise measurement shows higher noise on the high and low cells.

The timings of the triggers and various reset signals were adjusted to study the effect on this pedestal structure, yet no correlation has been found. The jump of the pedestal every 8 cells comes from the physical location of the pipeline addresses, not perturbed by the trigger arrival time respect to write or read pointers.

This repeated structure of group of 8 pedestal dependency does not correspond to the APC3 address skipping progression logic explained in the previous section. The PAC address progression logic has a group of 4 structure.

Figure 3.4 shows the pedestal measurement when the bias current supply to the last source follower of the NICON is disconnected[8].

[8] The NICON front-end Amplifier consist of two amplification with feed back and two source follower for the output. We have disconnected the bias current supply to the last source follower, thereby ensuring that the output from the NICON will not follow the input signal.

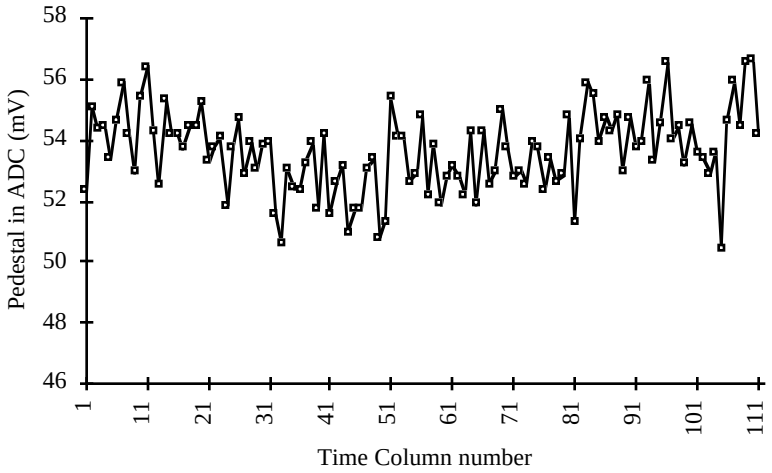


FIGURE 3.4: Pedestal for all 112 Time slot on Channel 8, no baseline subtraction, without NICON. RMS = 1.38 (mV)

From above figure, the rms pedestal fluctuation of a single channel for all time column can be evaluated, and it is measured to be 1.38 mV.

The repeated structure of the pedestal disappears in this setup. That is, the NICON causes an obvious baseline jump correlating to every 8 analog memory address. This possibly results from cross-talk with the encoding of the analog memory, the APC3 address progression logic, etc., picked up by the Front-End Amplifier. The address progression of the APC3 logic, described in the section 1.6, however, has grouping of 4, which does not correspond to this obvious baseline jump correlation observed. Further detail studies are in progress to understand the exact cause of this time column dependent pedestal fluctuation with the NICON.

However, without the NICON pick-up on the time column dependent pedestal fluctuation, there still remains a slow structure of the pedestal. The two ends of the logical address of the pipeline have a higher pedestal value than the middle cells, by ~2 mV. When this figure is plotted as a function of the physical address of the analog memory (refer to the previous section on the APC3 address progressing logic), the pedestal is higher on the beginning of the pipeline.

Pedestal and Noise with Baseline Subtraction

We can eliminate the above time column dependent pedestal fluctuation by performing off-line baseline subtraction. Figure 3.5 below shows the pedestal and noise of the ADAM with its full functionality, after off-line baseline subtraction.

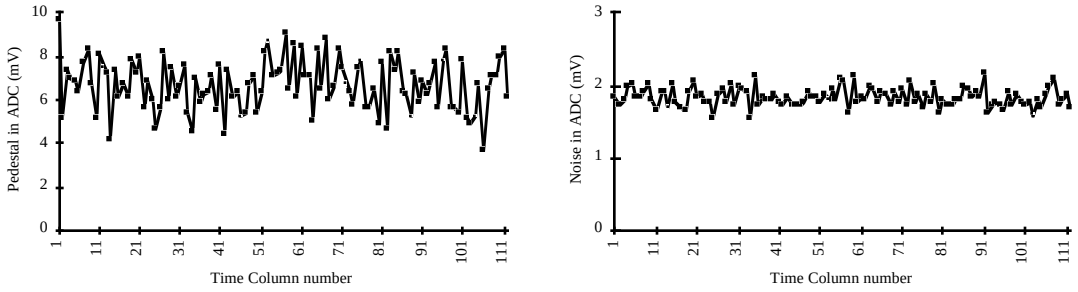


FIGURE 3.5: Pedestal (left) and Noise (right) for all time slot on Channel 8, with baseline subtraction.

Both noise and pedestal shows a stable distribution and no obvious structure depending on the time column is observed. The baseline shift variation or time column dependent pedestal RMS, has been measured to be 0.7 mV in this setup. This parameter has been significantly improved compared to the earlier developments. It is one of the features optimized by choosing a full differential readout structure within the analog storage array. Above figure yields:

Pedestal RMS on a single channel	1.16 mV
Average Noise level for all Time Column	1.83 mV
RMS of the Noise level for all Time Column	0.126 mV
Analog memory baseline fluctuation	0.7 mV

TABLE 3.6: Noise and pedestal with baseline subtraction.

Figure 3.7 shows the pedestal and noise on a single time column for all 32 channels. There is a clear difference between the first 16 channels and last 16 channels, due to the different Front-End amplifier layouts. Within each group, it shows a stable pedestal distribution.

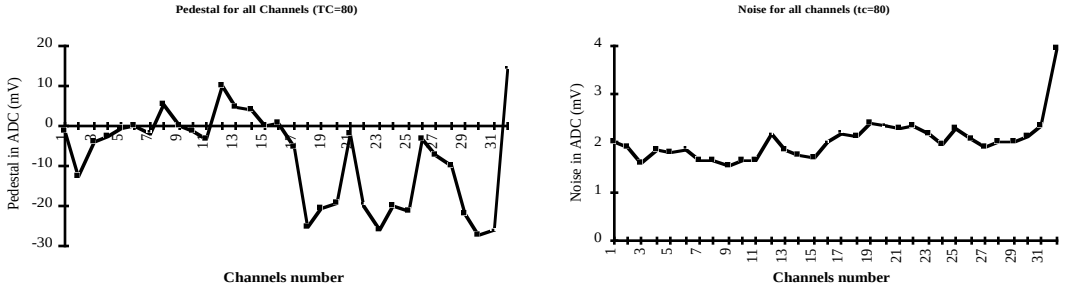


FIGURE 3.7: Pedestal (left) and Noise (right) on a single time column, with baseline subtraction.

When averaged over all time columns, the channel to channel pedestal variation is measured to be 4.3 mV on channels 1 to 16.

The pedestal fluctuation and noise depends mainly on two components of the ADAM chip, the Front End preamplifier and the pipeline. We have determined that the common baseline fluctuation by event comes from the Front-End preamplifier pickup, and it is closely associated with pipeline addressing logic, the APC3. The fluctuation of the pipeline alone has been measured by disabling the Front-End, and it yields a satisfactory result.

In the future development plan, a bipolar Front-End amplifier with lower noise and less external pickup than NICON amplifier is planning to be associated with DHARP pipeline to eliminate this common offset fluctuation problem.

3.3 Linearity

Linearity is measured by injecting a test pulse charge on a 1 pF load capacitance mounted on the Piggy Back board. Figure 3.8 shows the response of the ADAM with its full functionality.

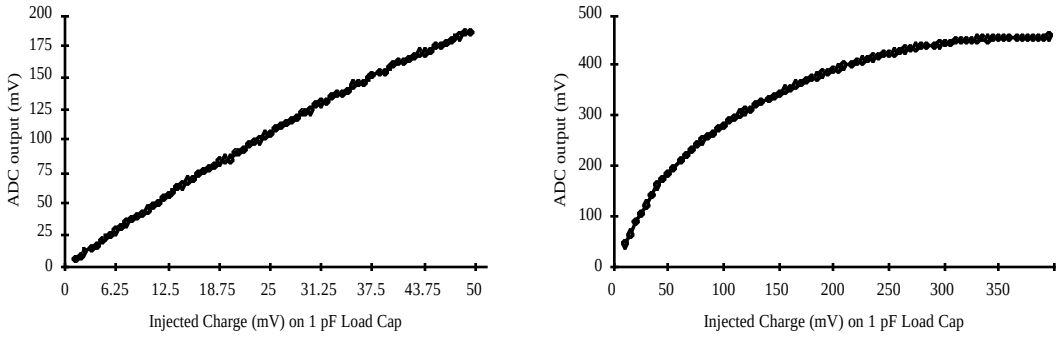


FIGURE 3.8: Linearity measurement. Linear region (left) and larger segment (right).

The measurement shown was taken with time column 44, channel 3. Other time columns and channels have been measured and they yields similar results. The injected charge is on a 1 pF injection capacitance, hence it yields 4 mV to 25000 electrons, or equivalent to one minimum ionizing particle deposed charge from detector (MIP). The figure above shows the good linearity response of the ADAM chip over 10 MIPs of injection change. It starts to saturate above a 20 MIP equivalent charge input.

In the linear region, the signal gain is measured to be ~20 mV per MIP of input, two times less than the amplitude measured at the output of the input preamplifier alone. That is, half of the charge is lost after the preamplifier output and before the pipeline output. This can either be on the charge transfer level between the NICON and the pipeline, the write amplifier of the pipeline capacitor, or the at the readout amplifier of the pipeline. The NICON output has been examined with a probe station, and verified that the output level of the pre-amplifier corresponds to the input signal. The strong possibility of this loss is at the write amplifier of the pipeline, thought it is not possible to access to this point directory. A further investigation to understand this gain is under way.

3.4 Gain Correspondence.

The gain difference on all time column and channels has been measured. A test pulse was injected to all channels and time slots to compare the gain dependency on the different capacitors of the analog memory. Figure 3.9 shows the dependence on the channel and time column on a single time column and channel.

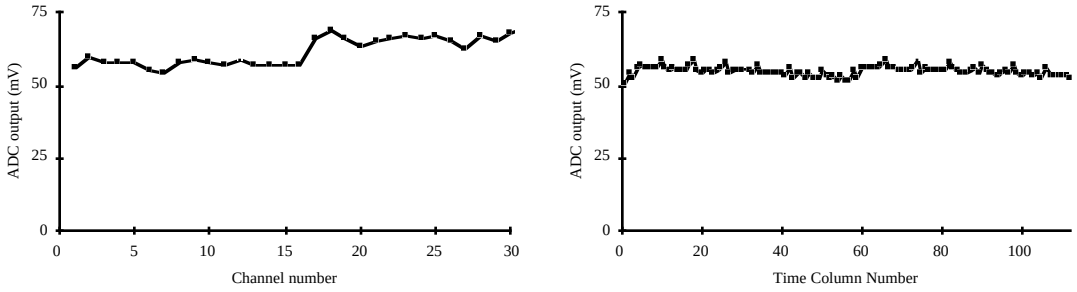


FIGURE 3.9: Gain. On a single time column (ts=44) for all channels (right) and on a single channel (ch=7) for all Time Column (left).

The channel to channel variation of the gain is plotted on the left. It shows the first 16 channels has lower gain than the last 16 channels due to the different Front-End amplifier. Within the 16 channels, it shows good gain stability. The time column dependency of the gain (on left) shows excellent over all stability, yet every 8^{th} time column has slightly higher gain than other addresses. These time columns correspond to the ones with higher pedestal explained in earlier section. However, the difference of the gain is less than 10%. Considering that the difference of the pedestal on every 8^{th} time column is only observed when the Front-End amplifier is connected, this time column dependent gain must also come from cross talk from the Front-End amplifier.

3.5 Load Capacitor and Noise Increase

We simulate the load capacitance of the detector installed with the ADAM chip and measured the noise parameter with the function of the load capacitance. Figure 3.10 shows the measured noise values of the Front-End amplifier only. The noise of the chip comes from several sources such as Front-End amplifier, the analog memory capacitors, read-out amplifier, ADC, etc. However two major contributors to the noise of the chip are the Front-End amplifier and the analog memory capacitance, and they add quadratically. We measured the internal noise of the ADAM chip without the Front-End amplifier by disabling its functionality, and subtracted quadratically from the global noise to determine the noise contribution of the Front-End amplifier only. In the figure, the 4.2 pF of the stray capacitance from the Piggy back board has been included.

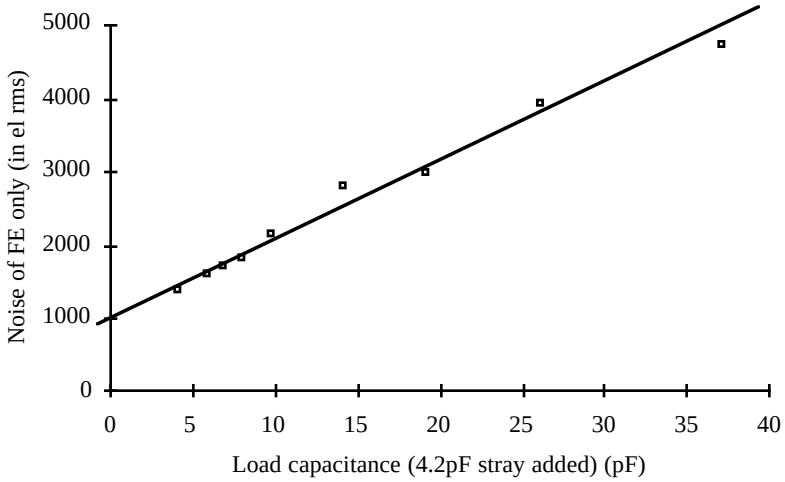


FIGURE 3.10: Noise vs.. load capacitance. Fit yields y=103x+1056.

The linear fit gives the slope and y-intersection. The slope is the increase of the noise per pF of added load capacitance, and y-intersection yields the bare noise value of the Front-End. The measured noise value is approximately 1000 electrons + 100 electrons/pF. This result is somewhat higher than what was measured with DHARP chip[9]. The overall signal over noise figure is > 10 for input capacitance below 10 pF, mainly because of the 6 dB gain loss observed in the channel, which makes the noise contributions of the readout stages non negligible.

Below in FIGURE 3.11 shows the pulse shape for various load capacitance.

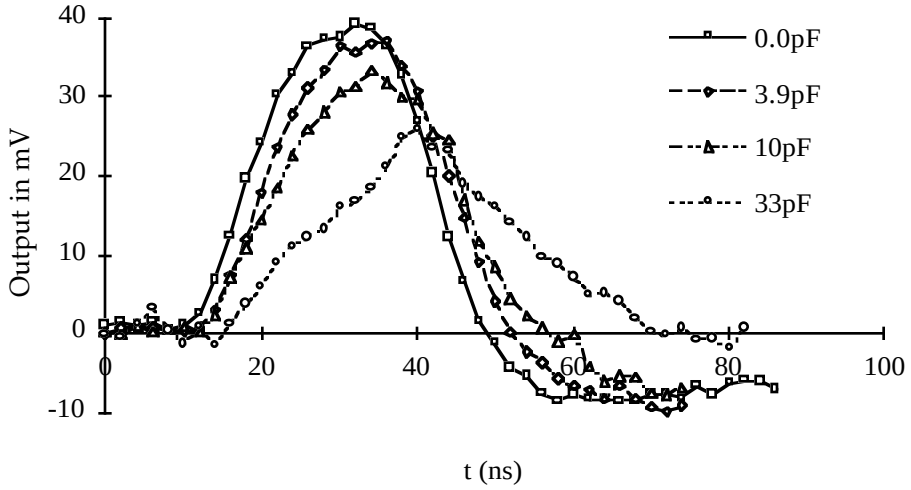


FIGURE 3.11: Comparison of the pulse shape of some load capacitance.

With additional load capacitance, there is more delay of the Front-End amplifier, and a loss of the gain, that reaches to 30 % in the extreme case of 33 pF load capacitance.

3.6 Multi-Trigger readout during the digitization and readout process

The ADAM chip accepts triggers without any dead time. The analog memory control logic has a skipping address logic which freezes the time column in which the data has been written when a trigger arrives, and continues writing the incoming analog data into the memory array, skipping the writing to this cell till the data has been digitized and readout of the chip. However, during the process of digitization and readout of digitized data the extra activities within the chip disturbs the analog memory writing, effecting the pedestal and noise of the analog memory array.

[9] In the DHARP measurement, it was measured to be 800 electrons + 60 electrons/pF.

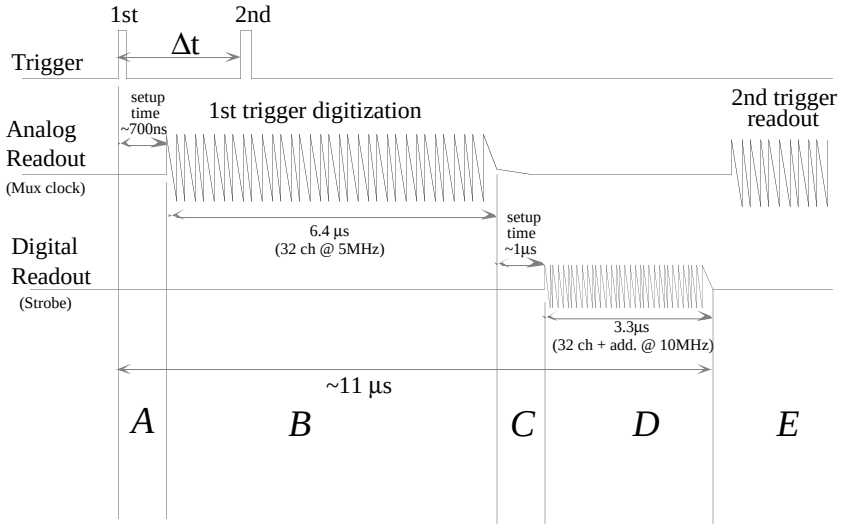


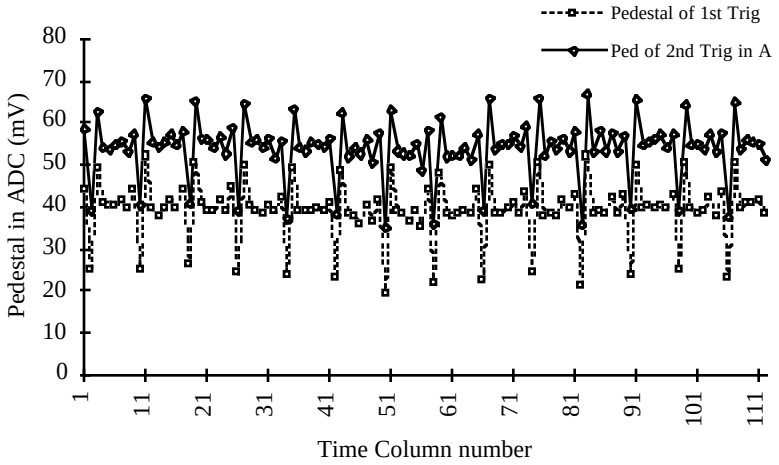
FIGURE 3.12: Consecutive trigger read out.

Figure 3.12 shows the timings of the multiple trigger readout. When the first trigger arrives, the ADAM chip takes some setup time for transferring the analog memory charge to the internal ADC, which is approximately 700 ns (***A*** in the figure). The digitization of 32 channels data follows, and in the case of 5 MHz ADC clock, it is 6.4 µs (***B***). During this period, the digital FIFO in the chip is being with the first trigger data. After the digitization has been processed, there is ~1 µs of set up time for read out logic control (***C***). Finally, the data is being read out to external bus from the chip at the speed of 10 MHz (***D***)[10]. This process takes 3.3 µs with 32 channels of data plus the address information of the analog memory. The whole process takes approximately 11 µs to complete.

The second trigger is sent during this process period. The analog memory is written while the ADAM chip process the analog data internally, and we have observed the effect on the pedestal and noise level for this second trigger.

With Icon, during setup time (A)

[10] The digital read out process will follow as described when the readout bus is ready to take the data from the ADAM, or REIN has been sent to the chip previous to this time.



With ICON, during digitization (B)

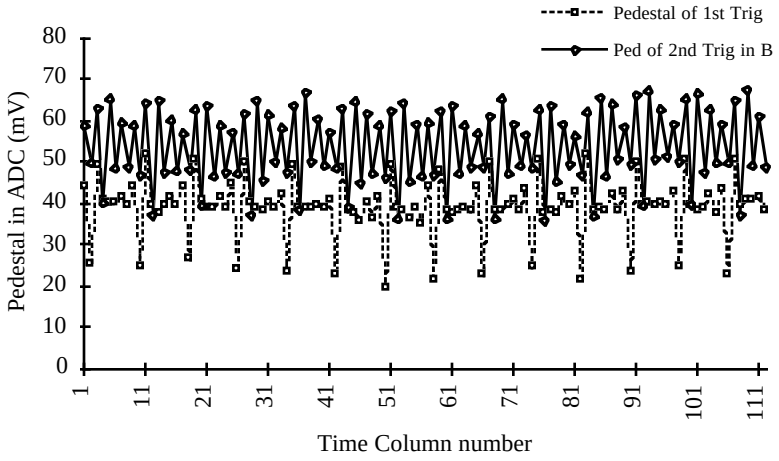


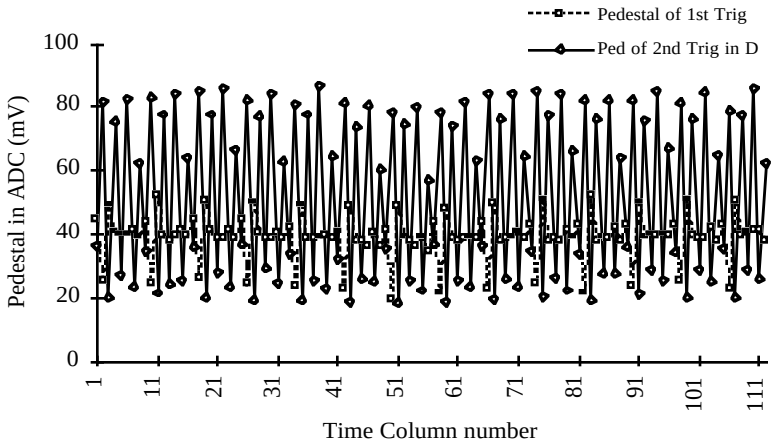
FIGURE 3.13: The pedestal comparison by time column during digitization. Channel 7.

Figure 3.13 shows the pedestal of the first trigger by time column on a single channel and of the second trigger, taken in the time interval of (A) and (B). The ICON is activated hence the effect of the internal pick up though the FE amplifier is also included in this figure. As discussed in the previous section, the repeated pedestal pattern in every 8 time columns comes from Front-End amplifier pick-up. During the setup time (A), the pedestal is shifted by ~ 15 ADC bins uniformly through out the analog array, keeping the same pedestal structure. Here the channel dependent pedestal structure (and noise) shows the same result. This effect is also observed when the ICON is disabled. However the corresponding noise associated with this pedestal (A) is not increased.

On the right (B) the pedestal during the digitization is plotted. Two effects on the pedestal are observed: the general increase on the pedestal bins as observed in case (A) and odd-even structure pattern along the time column. The analog memory noise has increased by factor of 2 to 3 in corresponding measurement. This odd-even structure of the pedestal is not observed when the Front-End amplifier is disabled, thus it is another result from the parasitic pick-up with the FE

amplifier. During this period (B) the noise is increased by factor of 2 to 3 compared with corresponding single-triggered measurements.

With ICON, during Readout time (D)



Without ICON, during Readout time (D)

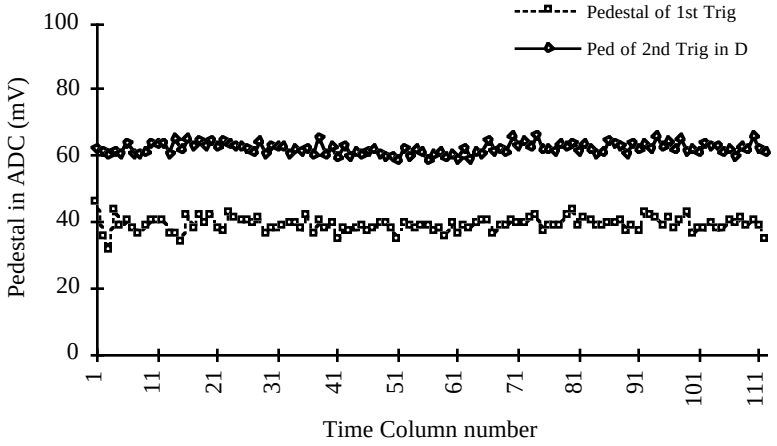


FIGURE 3.14: Pedestal comparison during readout, with and without ICON F.E. Channel 7.

Figure 3.14 shows the pedestal during the digital readout period to the external bus from the ADAM chip (D). The upper figure shows with Front-End amplifier operation, and right with ICON being disconnected. The odd-even structure which has been observed during digitization period (B) gets much larger during this period. The corresponding noise level increased by up to factor 4. This effect of Front-End pick-up is not observed when the ICON is disabled, plotted on the right. However the pedestal has been shifted up by ~ 20 ADC bins here.

In summary, the pedestal of the second trigger is perturbed if the second trigger arrives within 11 μs or during the first trigger data processing time. The second trigger pedestal is shifted up to 20 ADC bin (mV) from analog memory part through out this period. It also picks up a unique time column dependent structure due to parasitic pickup from the Front-End, and the structure depends on the functionality of the chip, possibly analog array addressing. However, the channel to

channel pedestal structure stays unchanged, hence the internal activity of the ADAM chip affects the pedestal in only a time dependent way. This baseline shift of the second trigger is not observed if $\Delta t > 11$ μs. The corresponding noise is increased during the first trigger data processing period as well.

The ADAM chip is designed to reduce possible source of noise and cross talk, as well as lowering the power consumption, by using low-level operation for which the input signals has a voltage swing of 200 mV, and a high level corresponding to 5 V TTL operation. The input signals which takes this low-level operation[11] are present at the moment of data writing/reading to the capacitor array of the chip, to eliminate any possible parasitic within the chip. With this low-level operation, however, this pedestal perturbation of the second trigger during the data processing time is also observed.

3.7 REIN delay

After the digitization for the analog memory has been performed, the digitized data is stored into the output digital buffer in the ADAM chip. The output buffer has a capacity of 2 blocks of data[12]. The digital readout logic (ROL) enables the digital readout when there is at least one block of data in the output digital buffer (half full) and a REIN (read enable in) signal has been received via external DAQ control. Under those two conditions, ROL sends out the digitized data with the strobe, at a 10 MHz clock speed provided from the general ADAM chip control.

The analog readout, however, is enabled when at least one block of the output buffer is free (half empty). If more than 2 blocks are requested by DAQ, at least one block of digitized data must be read out before third block can be processed. The analog memory control waits for the half empty flag is sent from ROL. Figure 3.15 shows this readout sequence.

FIGURE 3.15: REIN and analog/digital readout timings.

During the time after the completion of the second analog readout and the end of first digital readout, the analog signal is held in the analog memory capacitance. We have measured the pedestal and noise effect on the third time slot readout with the delay of REIN, up to 100 μs. No noticeable effect has been observed, proving a good stability and capability of keeping the charge in the analog memory capacitors.

3.8 Double Pulse Resolution

The time resolution of the Front-End readout is another important issue in the ATLAS detector of the LHC experiments. The bunch crossing is at 25 ns and it require a fast readout amplifier. The ADAM chip operates with 40 MHz master clock, or the LHC bunch crossing speed, and it demands the NICON Front-End amplifier to respond at equivalent speed.

FIGURE 3.16 shows the time resolution of the ADAM chip, with double pulse injection.

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[11] The low-level input signals are Mclk, Mclk_bar, Trig, and Trig_bar, REIN.

[12] One block of data consists of 33-8 bits word. 32 words for 32 channels and 1 word for analog memory address.

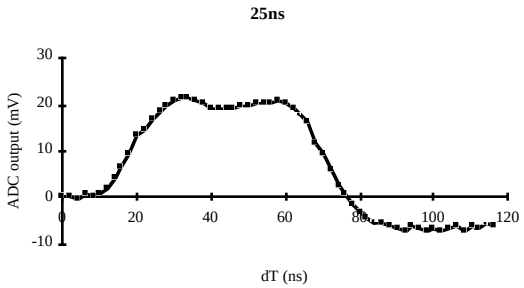

FIGURE 3.16: Double pulse resolution. Δt=50 ns (left) and Δt=25 ns (right)

It shows good resolution with a 50 ns time interval on the left figure. The pulse shape reaches at zero before the second pulse arrives, showing the chip functionality meets the specification for the ATLAS detector. The right figure shows the resolution of 25 ns time interval double pulse. It shows that the differentiation of those two pulses is possible.

3.11 Power Consumption

The power consumption of the ADAM chip is measured as 132 mW for Digital processing (at 6 V) and 128 mW for Analog part (at 6V) which includes the ADC. From previous measurement of CRIAD, the power consumption of the ADC operating at ADAM specification is 32 mW. Expanding this figure, the expected power consumption for future 128 channels integrated chip, per channel, will be 1.28 mW for digital part and 3.01 mW for analog part, yielding of 4.29 mW per channel.

4. Summary of Performance Measurements

Below in Table 4.1 shows the summery of performance measurements of the ADAM chip.

TABLE 4.1: Summary of performance measurements of the ADAM chip.

5. Conclusion

The ADAM, the first prototype of an integrated Front-End digital electronic readout chip for silicon tracker, has been tested for its functionality towards the ATLAS inner detector specification. The test showed full functionality at 40 MHz and characteristics of individual components were obtained.

The analysis of the analog memory showed a sufficiently low noise level for a single memory cell, and stable fluctuation in the time columns. It showed a good linearity response to the injected pulse. It obtained signal to noise ratio for a MIP signal to be over 10 with 10 pF input capacitance. The double pulse resolution reaches LHC bunch crossing spacing, which is at 25 ns. Power consumption for 128 channel ADAM chip, expanded from 32 channel version of ADAM, meets the ATLAS requirement.

However, it was found that the NICON Front-End amplifier picks up internal cross-talk during digitization of the analog memory and the digital readout period. Other options such as a bipolar Front-End amplifier in place of NICON have been considered. The baseline fluctuation, or time column dependent pedestal, previously observed in DHARP analog memory chip, has also been observed in this chip, though the amplitude of the fluctuation is less than 1 mV.

We have configured the ADAM chip on series with optical link controlled by Read Out Control (ROC), which replace the ADAM test board and other external controllers. the control signals, received by the ROC though an optical link, will be distributed to the chip through low level signal lines.

A telescope consisting of three prototype modules are installed and tested on a test beam in May, 1995, and the off-line analysis is in progress.

Acknowledgment

We would like to acknowledge those ATLAS RD2 collaboration members who has contributed their work and effort to the development of the ADAM chip. Also to the collaboration members at University of Geneva.

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