PART B

ATLAS Internal Note
INDET-NO-086 (1994)

15 December 1994

Pixel detector back-up Document to support the ATLAS Technical Proposal

P. Fischer, B. Raith, N. Wermes
University of Bonn, Germany

A. Lankford, S. Pier and B. Schmid
University of California, Irvine, USA

M. Campbell, P. Jarron, E. H. M. Heijne, P.[1] Middelkamp, W. Snoeys
CERN, Geneva, Switzerland

C.Arrighi, L. Blanquart, V. Bonzom, J-C. Clemens, M. Cohen-Solal, P. Delpierre, A. Fallou, E. [2]Grigoriev, M.C. Habrard, G. Hallewell, D. Labat, L. Lopez, A. Mekkaoui, T. Mouthuy, R. Potheau, M. Raymond, A. Rozanov, D. Sauvage, L. Vacavant.
CPPM, Centre de Physique des Particules de Marseille,France

D. Bintinger, A. Ciocio, K. Einsweiler, M. Gilchriese, O. Milgrome, J. Millaud, D. Nygren, M. Shapiro, J. Siegrist, H. Spieler, M. Wright
Lawrence Berkeley Laboratory, California, USA

G. Capannesi, M. Colucci, P.G. Pelfer, S. Sottini
INFN and Physics Department of Firenze University, Italy

D. Barberis, M. Bozzo, C. Caso, M. Dameri, G. Darbo, P. Morettini, P. Musico, B. Osculati, L. Rossi, G. Sette
INFN and Physics Department of Genova University, Italy

R. Bates, S. D'Auria, S. Gowdy, V. O'Shea, C. Raine, K.M. Smith
Glasgow University, UK

G. Bellini, M. di Corato, A. D'Avella, P. Inzani,D. Menasce, L. Moroni, D. Pedrini, L. Perasso, F. Ragusa, S. Sala, F. Tartarelli
INFN and Physics Department of Milano University, Italy

G. Cesura, D. Hauff, H. Hoernl, J. Kemmer, P. Lechner, G. Lutz, R. H. Richter, H. Seitz
MPI Halbleiterlabor, Munich, Germany

Y. Gao, J. Harton, R. Jared, M. Walsh, S. Wu
University of Wisconsin, Winsonsin, USA

K. H. Becks, K. W. Glitza, J. Heuser, S. Kersten
University of Wuppertal, Germany

[1]Also at University of Wuppertal
[2]On leave of absence from ITEP, Moscow, Russia

Cooling to the outer and inner edges of the wedges is provided by heat sinks that radiate out from the central cooling ring on the back of the wedges.

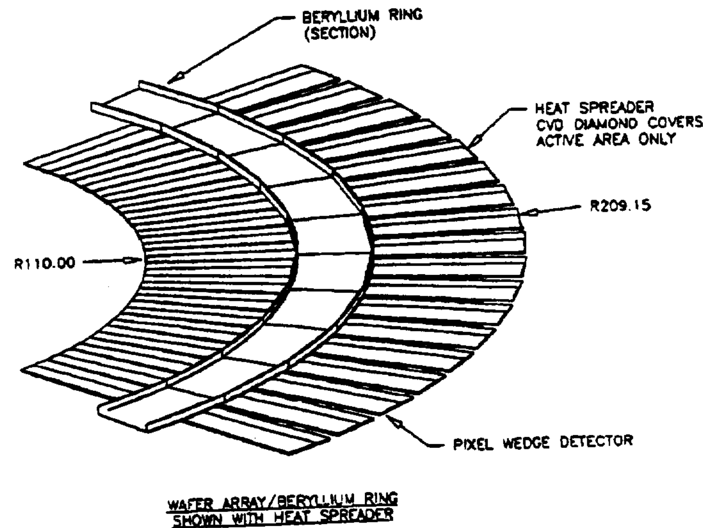


Figure 41: Section of one side of a disk showing heat spreaders of CVD diamond

Figure 41 presents a section of one side of a disk showing heat spreaders of CVD diamond. The temperature distribution along a wedge with a heat sink of CVD diamond from coolant ring to the outer edge of the disk and no heat sink to the inner edge has been calculated.

The temperature at the outer edge is 1.8°C whereas it is 14°C at the inner edge showing the need for heat removal to the extremities of the wedges. The same problems that occur in the barrel staves due to CTE mismatch occur here but are lessened by the smaller length over which the mismatch occurs. Also heat sinks can be made of material that more closely matches the CTE of silicon than beryllium. More design work, including simulations of stress and strain, is necessary to combine cooling for the disk with a support structure. Figure 42 shows a disk with supporting frame.

3.1.2.3 Pixel System Support Structure A space frame of graphite fiber composite is proposed as support for barrel and disk pixel systems. Figure 43 shows a sketch of a space frame.

This structure is light weight and strong. No mechanical calculations for this structure have been done at present.

3.1.2.4 Radiation length estimates The number of radiation lengths in this design, including services, is shown in Figures 44 and 45 without and with the B-layer, respectively

3.2 Cooling and Temperature Stability

3.2.1 Pixel Cooling studies at LBL

A cooling analysis of a barrel stave has been done using a water glycol mixture and a binary ice solution as coolant. We assume an operational temperature of approximately 0°C for the

silicon. The water glycol mixture will be discussed first. A 30% by weight ethylene glycol and water solution with a freezing point of −14°C is used. The stave for this calculation consisted of 12 barrel modules with a total heat load of 15.0 watts based on a per pixel heat load of 17 microwatts. Rectangular and circular channel cross sections have been studied but only the circular will be reported on here. The rectangular tube gives a lower velocity and Reynolds number than the circular tube. The system is considered as running below atmospheric pressure to minimize leaks, hence pressure drop along a stave is limited to approximat

Flow- cc's/min versus ΔT

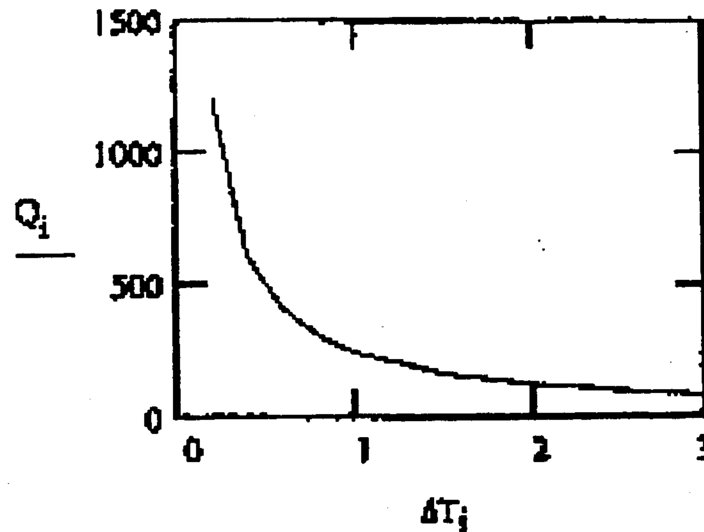


Figure 46: Flow (cc/min) along a stave versus temperature (°C) increase

Figure 46 presents flow along a stave versus temperature increase. As can be seen from the plot the flow is quite low for a temperature increase of 1°C.

Figure 47 presents channel diameter versus temperature rise. A channel diameter of 2.2 mm gives approximately a temperature rise of 0.6°C. Figure 48 presents flow velocity and Fig. 49 presents Reynolds number for a tube diameter of 2.2 mm.

The flow velocity is modest. The Reynolds number is very low indicating laminar flow. This condition is not optimal for heat transfer. A method to create turbulent flow may be necessary.

For the binary ice coolant calculations we assume the same stave heat load. The carrier solution for the ice is 10% by weight propylene glycol and water with a freezing point of −3.3°C. The incoming ice concentration is taken to be approximately 8%. We specify the system as running below atmospheric pressure to minimize leaks, hence pressure drop along a stave is limited to approximately one third of atmospheric pressure. We also desire a

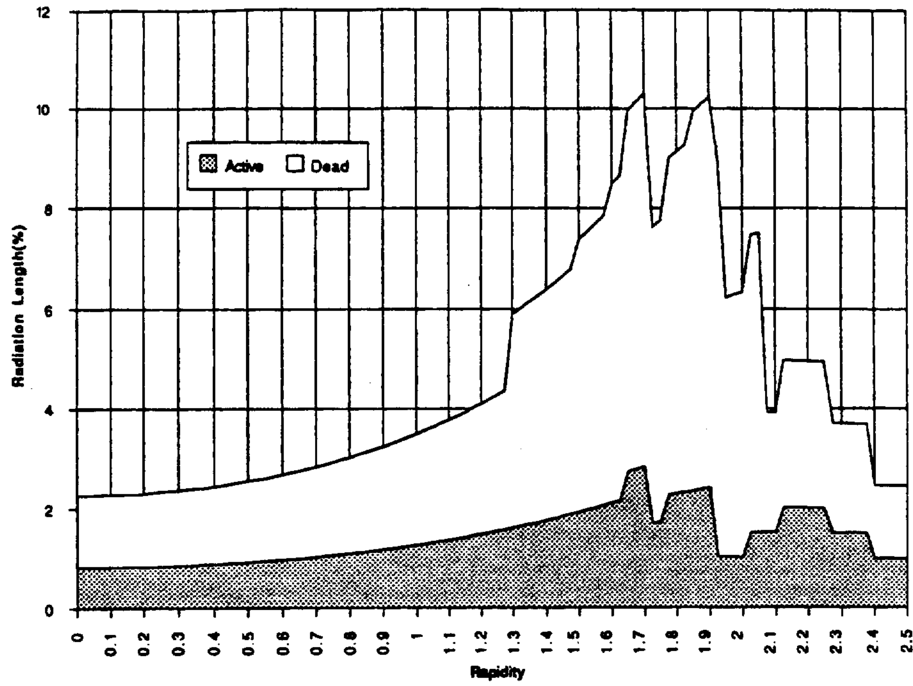


Figure 44: Radiation length due to the pixel system versus rapidity . Layout without the B-layer

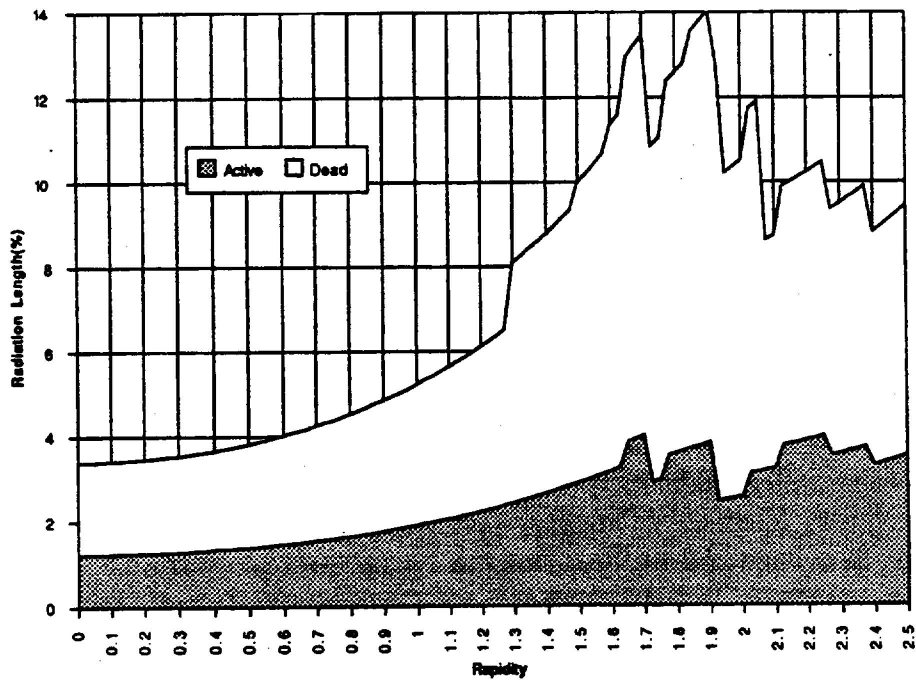


Figure 45: Radiation length due to the pixel system versus rapidity, including the pixel B-layer

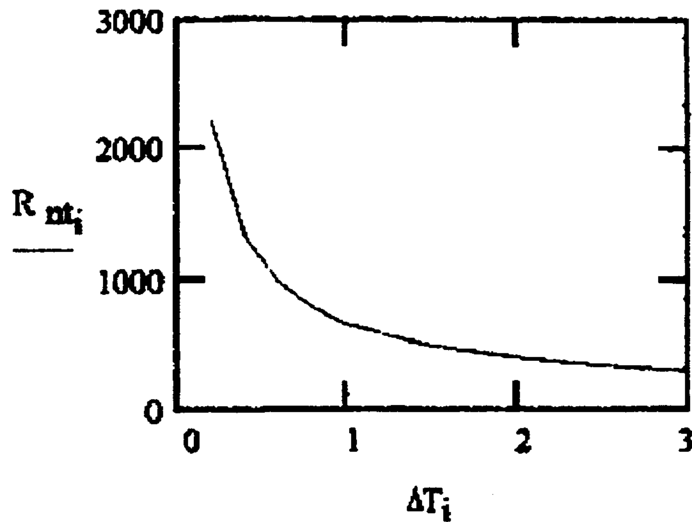


Figure 49: Reynolds number for a tube diameter of 2.2 mm versus temperature increase (°C)

coolant velocity greater than 0.7 meters per second for good heat transfer into the fluid as recommended. We calculate the tube flow diameter as a function of the change in ice concentration in the coolant. Figure 50 presents tube diameter as a function of the change in concentration.

Figure 51 presents flow velocity as a function of the change in concentration.

We see that a change in ice concentration of 4% gives a tube flow diameter of 1.2 mm and a flow velocity of approximately 0.9 meters per second. Again as in the case of the water glycol mixture the flow will be laminar with a Reynolds number of approximately 400. The tube diameter is a weak function of change in ice concentration. We see that the required tube diameter for binary ice is less than for the single phase water glycol mixture.

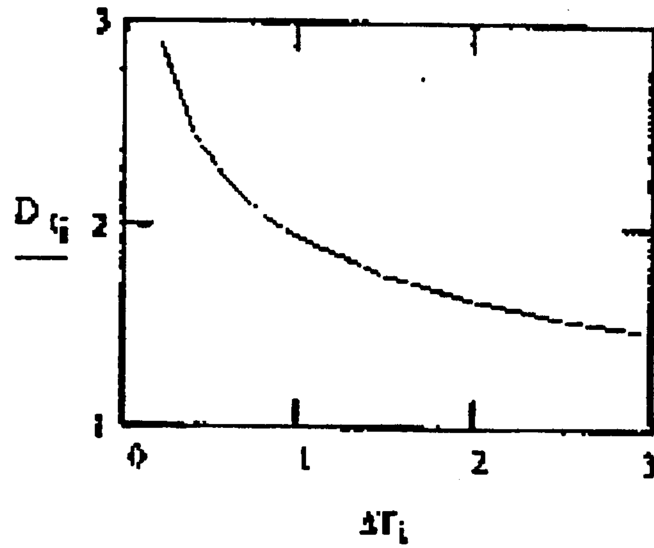
A cooling analysis for a disk has also been done utilizing both a water glycol mixture and a binary ice mixture. We first look at the water glycol mixture with a freezing point of −14°C. A disk has a total heat load of approximately 111 watts based on a per pixel heat load of 17 microwatts. The coolant channel for a disk is a ring of rectangular cross section approximately half way between inner and outer radii. The rectangular passage was chosen to have a width (in contact with the silicon) to depth ratio of 8. The system is considered as running below atmospheric pressure hence a pressure drop for a disk is limited to approximately one third of atmospheric pressure. Figure 52 presents cooling flow in a disk versus temperature increase.

The flow is approximately 1500 cc per minute for a temperature increase of 1°C. Figure 53 presents channel width and depth versus temperature rise for the aspect ratio of 8 and a pressure drop of approximately one third atmosphere.

Channel dimensions of 16 mm by 2 mm give approximately a temperature rise of 0.2°C. Figure 54 presents flow velocity and Fig. 55 presents Reynolds number.

The Reynolds number for a temperature rise of 0.2°C is on the edge of turbulent flow which is optimal for heat transfer. A higher temperature rise could be tolerated by the

Tube Diameter-mm vs ΔT-Deg. C



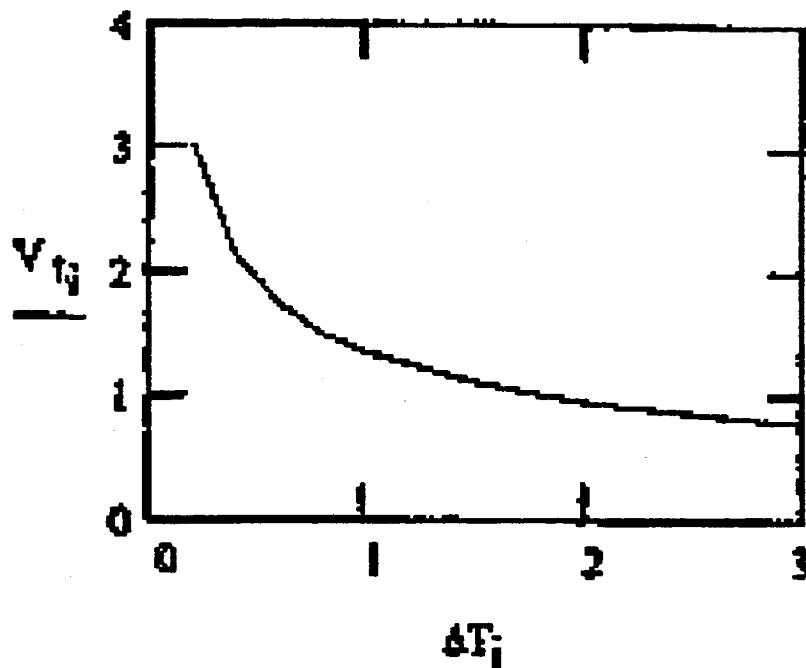


Figure 48: Flow velocity (m/sec) for a cooling tube of 2.2 mm diameter

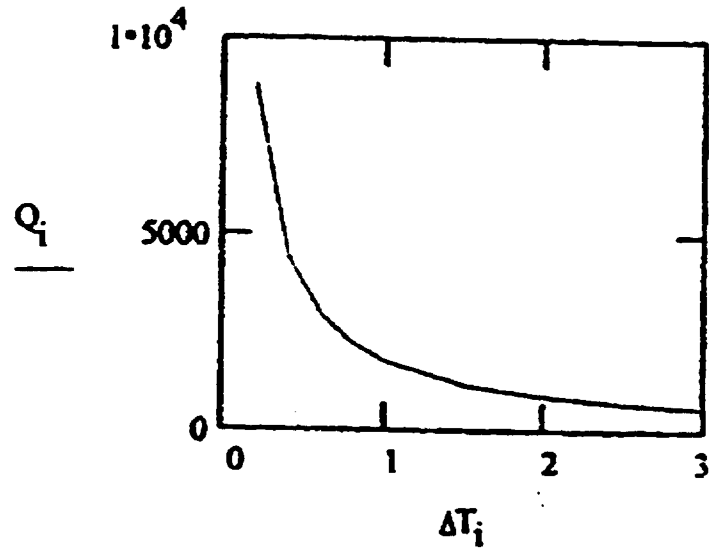


Figure 52: Cooling flow (cc/min) in a disk versus temperature increase (°C)

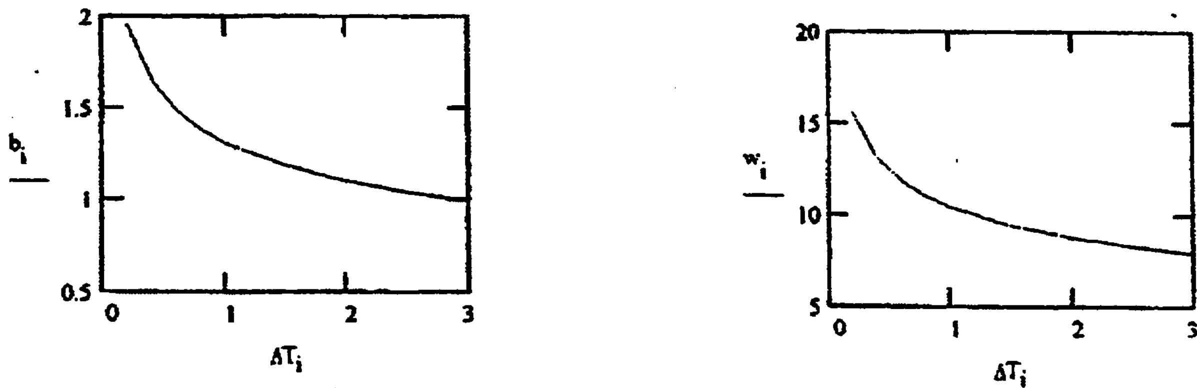


Figure 53: Channel depth (mm) and width (mm) versus temperature rise for the aspect ratio of 8 and a pressure drop of approximately one third atmosphere

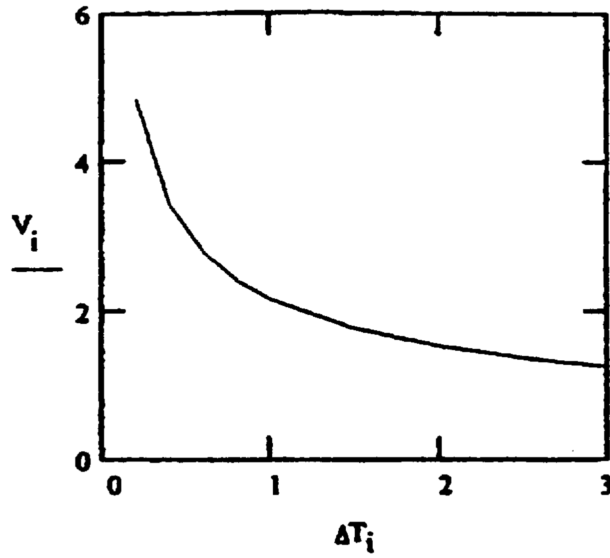


Figure 54: Flow velocity (m/sec) for a 16mm by 2 mm cooling channel

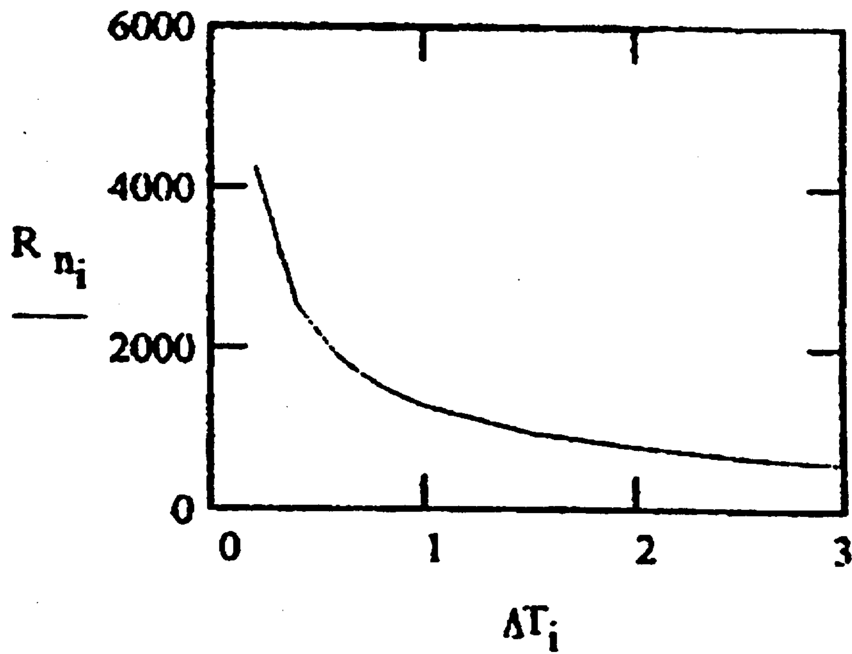


Figure 55: Reynolds number for a 16mm by 2 mm cooling channel versus temperature increase (°C)

silicon implying laminar flow which may be acceptable as heat is presented to both sides of the coolant passage.

For the disk binary ice coolant calculations we assume the same heat load of 111 watts per disk. The carrier solution for the ice is 10% by weight propylene glycol and water with a freezing point of −3.3°C. The incoming ice concentration is taken to be approximately 8%. We specify the system as running below atmospheric pressure to minimize leaks, hence pressure drop in a disk is limited to approximately one third of atmospheric pressure. We also desire a coolant velocity greater than 0.7 meters per second for good heat transfer into the fluid as recommended. We calculate the tube flow dimensions as a function of the change in ice conc passage with a wid

Channel Depth-mm's versus Ice Concentration

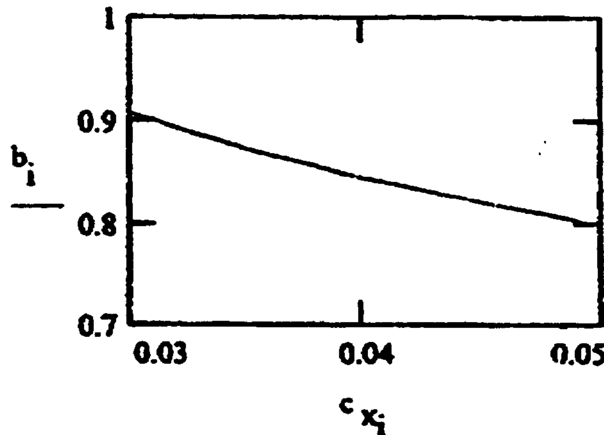


Figure 56: Tube depth (mm) as a function of ice concentration

Figure 56 presents tube depth as a function of the change in ice concentration. We see that a change in ice concentration of 4% gives a tube flow depth of 0.85 mm and hence a width of 6.8 mm. The flow is expected to be laminar. The tube depth is a weak function of the change in ice concentration. We see that the required tube dimensions for binary ice are less than for the single phase water glycol mixture. Further work on cooling system design is necessary. At this point, however, both a single phase water glycol mixture and a binary ice solution are at least reasonable options.

3.2.2 Pixel cooling studies at CPPM

3.2.2.1 Two-phase liquid-gas cooling for silicon pixel detectors A programme of research and development is under way at CPPM to develop a cooling system that can evacuate the power dissipated by the readout electronics of the pixel detectors, with the addition of the minimum possible extra material.

The thermal dissipation of the flip-chip bonded readout electronics on a pixel tile is expected to be around 0.4 Wcm^{-2}. The pixel detector operating temperature must be

maintained close to 0°C, with a temperature variation of no more than ± 2.5°C over the silicon detector surface. To avoid condensation, the ATLAS inner detector volume will also be flushed with dry nitrogen at a temperature around 0°C.

3.2.2.2 Studies of evaporative cooling One proposed cooling technology for silicon detectors is based on the use of the latent heat of vapourisation of a cooling fluid that is channeled in liquid form to the ("evaporator") surfaces to be cooled, and recovered in vapour form for recirculation. The recirculation system may be sealed, with no other moving components, as in the case of a heat pipe, or may be pump driven.

Evaporative cooling studies at CPPM have focussed on both types of recirculation system:

- a two-phase liquid-gas test bench was built to investigate cooling with evaporating "fluorinert" FC-72 fluorocarbon liquid [predominantly perfluoro-hexane: (C_6F_{14})]
- the performance of heat pipes using water as the evaporative coolant have been investigated

3.2.2.3 The Cooling System Table 10 shows the thermal characteristics based on 0.4 Wcm^{-2} of the pixel layers at 4.0, 11.5 and 16.5 cm.

The cooling system for these detector layers must:

1. evacuate around 6 kW of dissipated heat from the detector to external heat exchangers, which will probably be situated 30-50 m away, outside the experimental area;
2. maintain a temperature gradient of no more than ± 2.5°C over the entire detection surface, about the operating temperature, of 0°C;
3. induce minimal vibration (both in amplitude and frequency) into the structure - from either mechanical (pumps etc) or thermal (cyclic expansion) effects;
4. be leak-tight to a high degree to avoid contaminating the detectors with leaking refrigerants, or a failure of cooling in part of the detector.

Table 10: Thermal characteristics of the pixel layers at 4.0, 11.5 and 16.5 cm

Layer Radius (mm)	No Ladders	No modules / ladder	No modules total	Active area / ladder (cm^2)	Total active area (cm^2)	Power diss./ adder (W)	Total power diss. (W)
40	16	11	176	112.86	1806	45.2	723
115	48	11	528	112.86	5417	45.2	2170
165	64	13	832	133.38	8536	53.4	3418
All layers		1536			15759		6311

Both systems make use of a liquid-gas bi-phase flow, with the saturated vapour pressure at the point of liquid evaporation controlling the temperature, and with the amount of heat that can be removed being directly proportional to refrigerant liquid flow into the evaporator.

Table 11: Physical properties of selected refrigerants

	Boiling Temp. (°C) (1 atm)	Density (g/cm^3)	Viscosity (dyn. cs) at 25°C (mbar)	Vapour pressure (J/g°C)	Heat Capacity vapouris. (J/g)	Latent Heat of (W/m°C)	Therm. Conduct. ($x10^{-5}$ N/cm)	Surface Tension
Water	100	1.0	1.0	32	4.2	2257	0.58	72
FC-87	30	1.63	0.4	813	1.05	100.5	0.056	12
FC-72	56	1.68	0.4	308	1.05	90	0.057	12
Ammonia	-33	0.68	0.14	10	2.06	130	0.47	20

The planned evaporator consists of the network of aluminium cooling tubes in parallel arranged around the detector layers with a pair for each ladder of detectors. The tubes contain capillaries to help maintain a thin film of liquid in contact with the tube wall in which the liquid - vapour phase change is driven by the heat absorbed from the electronics. A good match of the capillary mesh pore size to the surface tension of the chosen refrigerant should allow the formation of a stable and uniform fluid film.

3.2.2.4 The Prototype Evaporator Figures 58 and 59 shows the prototype (single tube) evaporator, in which have started to study cooling with FC72 refrigerant. A cylindrical capillary mesh (50 μm pore size, 80 μm pitch) is inserted inside a pyrex tube of 4 mm internal diameter. The FC72 refrigerant enters at one end of the tube, entrained as an aerosol mist in a flow of dry nitrogen carrier gas. The mist impinges on the wick, and FC72 liquid preferentially moves along the inner surface of the tube by capillarity, while the nitrogen passes through the center of the tube. The exhaust mixture of nitrogen and vapour evolved from the tube walls is evacuated with a pump. The pressure in the tube is measured with an electronic pressure gauge.

The use of a nitrogen carrier confers several advantages:

- easier control of the pressure in the cooling channels via the equilibrium between the pumping speed and the combined supply speed of the nitrogen and evolving refrigerant vapour;
- more uniform wetting of the capillary mesh and more uniform observed temperature gradient along the tube.

In one of the pair of cooling channels per detector ladder 30, the mass flow, m_l, of evaporative liquid refrigerant necessary to remove the dissipated heat, P_l , is given by;

$$m_l = 0.5 P_l / h_l \quad (2)$$

where h_l is the latent heat of vapourisation of the liquid. As an example, a ladder dissipating 60 W and cooled by evaporation of FC72 (h_l =90 J/g) will require a liquid mass flow of 0.34 g/s.

From knowledge of the geometry of the capillary mesh and the tube, it is possible to calculate the thickness and linear flow velocity of the liquid film along the interior of the tube. In the case of the prototype evaporator tube, we estimate that the minimum space between the mesh and the inner surface of the tube is 0.1 mm.

The maximum liquid laminar flow velocity, u_l , is given by

$$u_l = m_l / (A_l \rho_l) \quad (3)$$

where A_l is the cross sectional area of the liquid film, and ρ_l is the liquid density.

In the example above, for the prototype tube, the FC72 flow velocity is $u_l = 0.145$ m/s.

At the tube exit, assuming that all the liquid supplied has been vapourised, the vapour volume flow, q_v, is given by

$$q_v.\rho_v = q_l.\rho_l \quad (4)$$

where ρ_v is the vapour density. In the example above, for the prototype tube, the FC72 vapour flow rate is 15.4 cm^3/s with a corresponding linear (laminar) flow rate (for a 4 mm internal diameter cooling tube) of u_v =1.2 m/s.

3.2.2.5 Observed temperature regulation in the prototype evaporator Around an operation point of 0°C, we were able to see that a small change in the flow of injected nitrogen was sufficient to vary the temperature profile along the tube. Several mechanisms could be responsible for this:

- a variation in the partial pressure of FC72 active refrigerant present in the nitrogen/FC72 mixture (fig. 57).
- a change in the dynamics of the phase transition - evacuation of the evolving FC72 vapour or in the geometry of the liquid film on the interior of the tube;
- a variation in the forced convection in the tube, and consequently in the heat transfer characteristic.

3.2.2.6 Condenser In the proposed system, the nitrogen carrier gas will be vented, while the refrigerant may be recondensed for recirculation. Recondensed refrigerant will held in a reservoir, and will be pumped back to the evaporators in liquid form at ambient temperature.

The heat source in our preliminary test was just the temperature difference between ambient room air at 27°C and the cooled tube. A big change in the thermal load to be evacuated will require an adjustment of the amount of liquid refrigerant injected into the system. To be sure that sufficient liquid is being injected it is advisable to tune the system so that a small amount of liquid is present at the output. The liquid presence could be verified by (for example) a small immersed resistive element, which could be used to control the flow of liquid at the injection point. A small flow of liquid at the exit should not impede the bi-phase cooling performance of the system. An ultrasonic (speed of sound) gas analyser cell installed in the exhaust of the array of cooling tubes can provide a very accurate measure of the relative concentrations of FC72 (C_6F_{14}) vapour and nitrogen in the exhaust mixture: in conjunction with the known input nitrogen flow rate, this can indicate the amount of power being removed by the cooling system. Such analysers have been demonstrated to provide a mixture measurement accurate to 1 part in 10^4 for FC87 (C_5F_{12}) vapour/nitrogen mixtures [43].

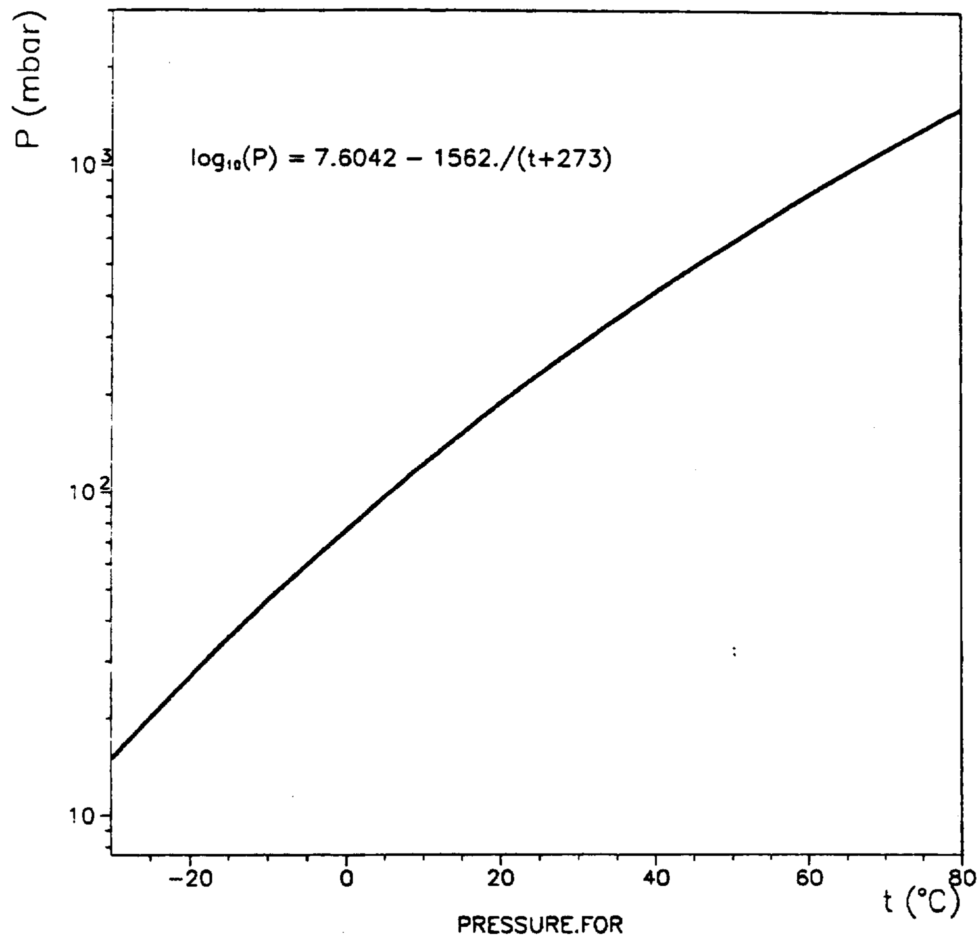


Figure 57: Vapour Pressure Curve for fluorinert FC72

3.2.2.7 Performance Summary We have found in preliminary studies with the cooling system of fig 58 and 59;

- a temperature variation of 1.25°C along the length of the 750 mm test cooling tube when operated at a temperature of 0°C [at a corresponding (total) tube input pressure of 75 torr (99 mbar)]; the total pressure established with the aid of a slow flow of nitrogen gas (fig 60).
- a temperature variation of 1.9°C along the length of the 750 mm test cooling tube when operated at a temperature near 5°C [corresponding tube input pressure of 97 torr (128 mbar)], with slow nitrogen flow;
- that the thickness of the capillary film in the tube is of the order of 100 μm, a factor of 10-20 thinner than the material presented by an all liquid cooling system;

- that the capillary liquid film operates in a regime of laminar flow, so that vibrations introduced by a cooling system of this type are expected to be insignificant. We plan, however, to make vibration studies using a laser interferometer to be sure of this.

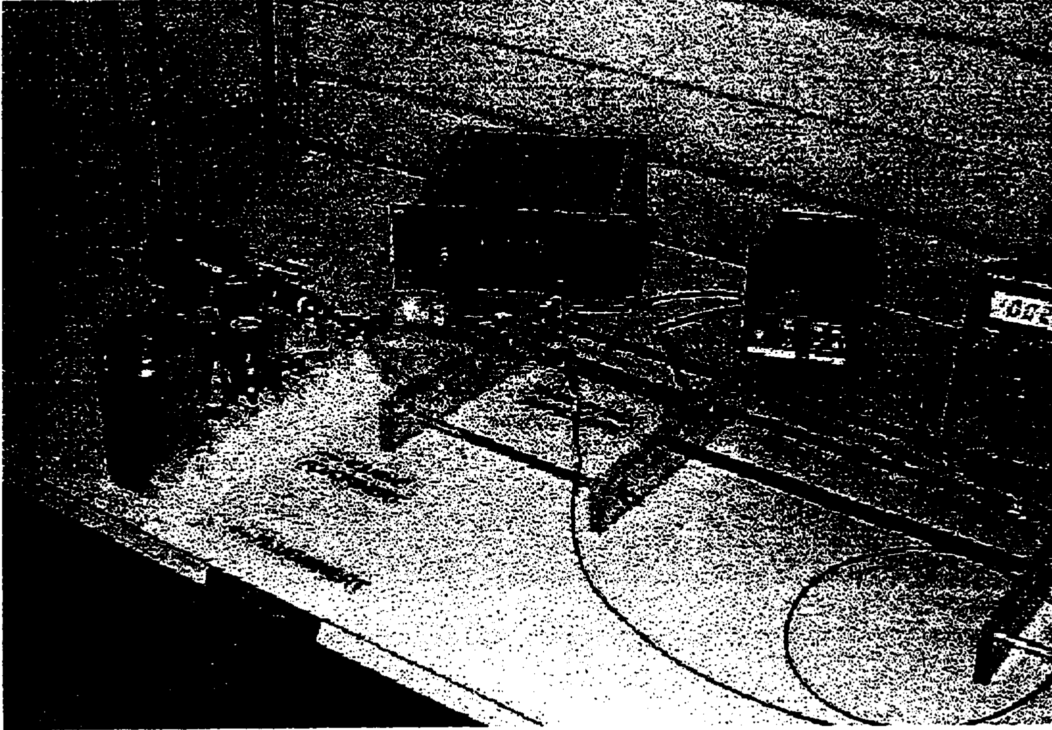


Figure 58: General view of the bi-phase cooling measurement system.

The advantages of such a bi-phase cooling system are two-fold;

1. delivery of the refrigerant and carrier at the ambient detector temperature, eliminating the need for thick insulation on the refrigerant delivery tubing, which would add more dead material in the sensitive detector volume;
2. reduced probability of detector contamination from leaking coolant, since the system operating pressure (the saturated vapour pressure of the refrigerant plus that of the nitrogen added) is below atmospheric pressure

3.2.2.8 Heat Pipe Cooling Studies Prior to our studies with a pumped bi-phase cooling system, we had made a series of cooling studies of a test structure cooled with an array of miniature heat-pipes. It was planned to use heat pipes to evacuate the heat dissipated on silicon detector wafers into axial liquid cooling channels. Figure 61 shows a support and cooling structure to implement heat pipe cooling.

In this scheme, the liquid coolant transports the dissipated heat out of the detector, while the heat pipes assure a uniform temperature distribution across the silicon detector tiles.

In a performance study of the best miniature heat pipe we tested (Thermacore type XH5 copper envelope, cross section 2.5 x 9 mm, water filled), we measured temperature gradient

Figure 59: The liquid and gas injection region, with the control valves.

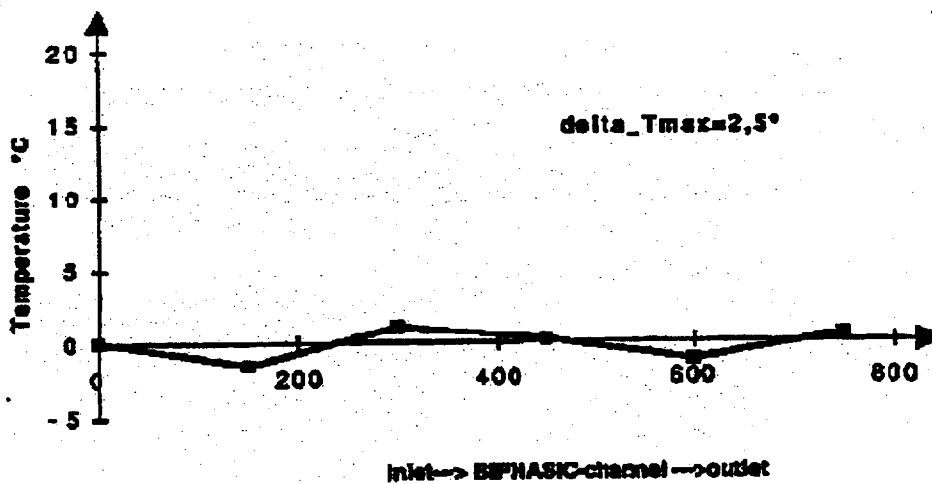


Figure 60: Temperature variation along the length of the pyrex cooling tube: operating temperature 0°C.

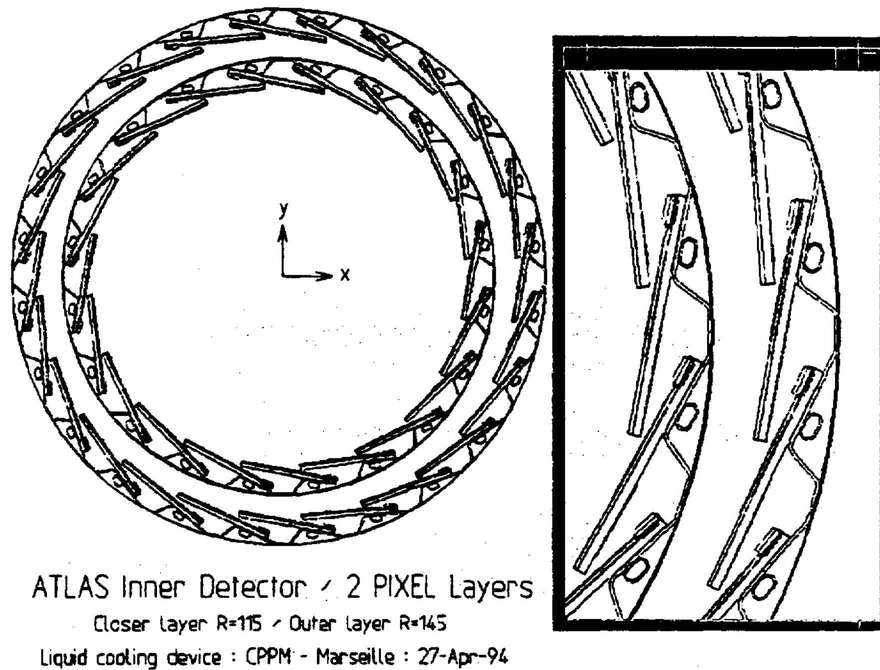


Figure 61: Heat pipe cooling scheme for a geometry of pixel detector layers at 11.5 and 14.5 cm, showing the positions of the miniature heat pipes, silicon detector tiles and axial coolant channels.

consistent with a thermal conductivity significantly superior to that of copper (fig 62). A study of the temperature distribution on a pair of pixel detector tiles (fig. 63) cooled by a pair XH5 heat pipes showed a temperature gradient of about 2°C for a simulated tile power dissipation of 0.4 Wcm^{-2}. This is within the acceptable detector temperature gradient specification. The power dissipation was simulated with heater elements glued to (2 x 6) cm silicon wafers, and the coolant in the condenser was water at 20°C.

Although having the advantage of being passive, sealed heat sink elements, requiring no external recirculation system, miniature heat-pipes were eventually discarded in favour of a lighter cooling structure.

3.3 Detector characteristics and radiation levels

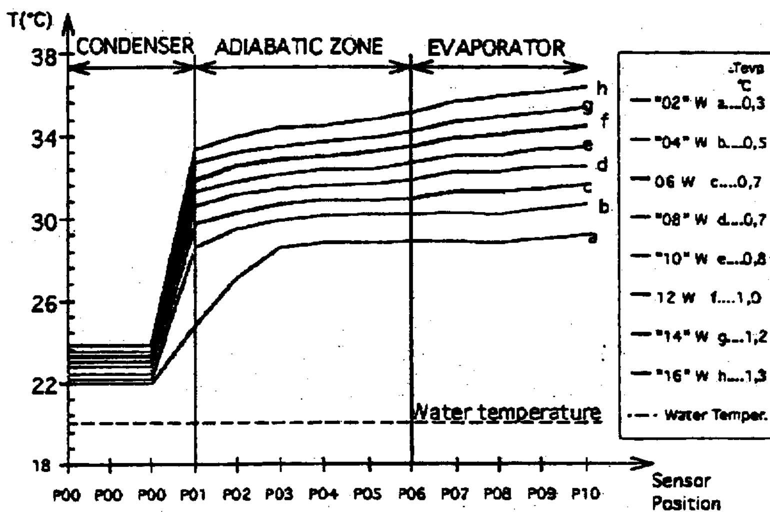
Taking a mean luminosity of 10^{34} cm^{-2} s^{-1} the particle fluxes in the pixel layer at a radius of 11.5 cm is given in table 12 according to [4]. These fluxes, according to Van Ginnecken calculations [45], could be expressed in equivalent dose and 1 MeV neutron equivalent fluence.

For the innermost layer that gives :

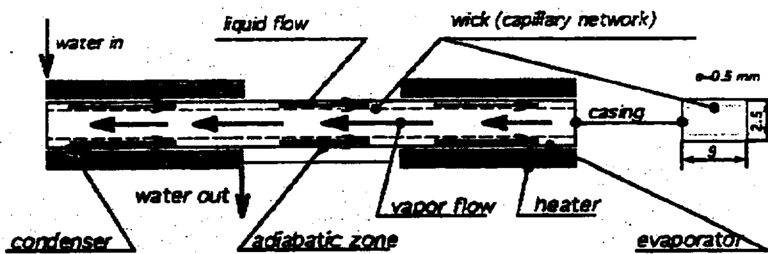
- Dose = 22 KGy/year
- Fluence = 6.4 10^{13} neutrons (1 MeV) cm^{-2} yr^{-1}

So, for 10 years operation, the ATLAS pixel detector must be able to survive at a fluence up to 5 10^{14} particles/cm^{-2} (in 1 MeV neutrons equivalent).

Heat-pipe Performance Test
cppm Marseille, 27 Avril 1993



Temperature profiles along the heat-pipe



Heat-pipe performance test rig

Figure 62: Performance measurements on a Thermacore XH5 heat pipe

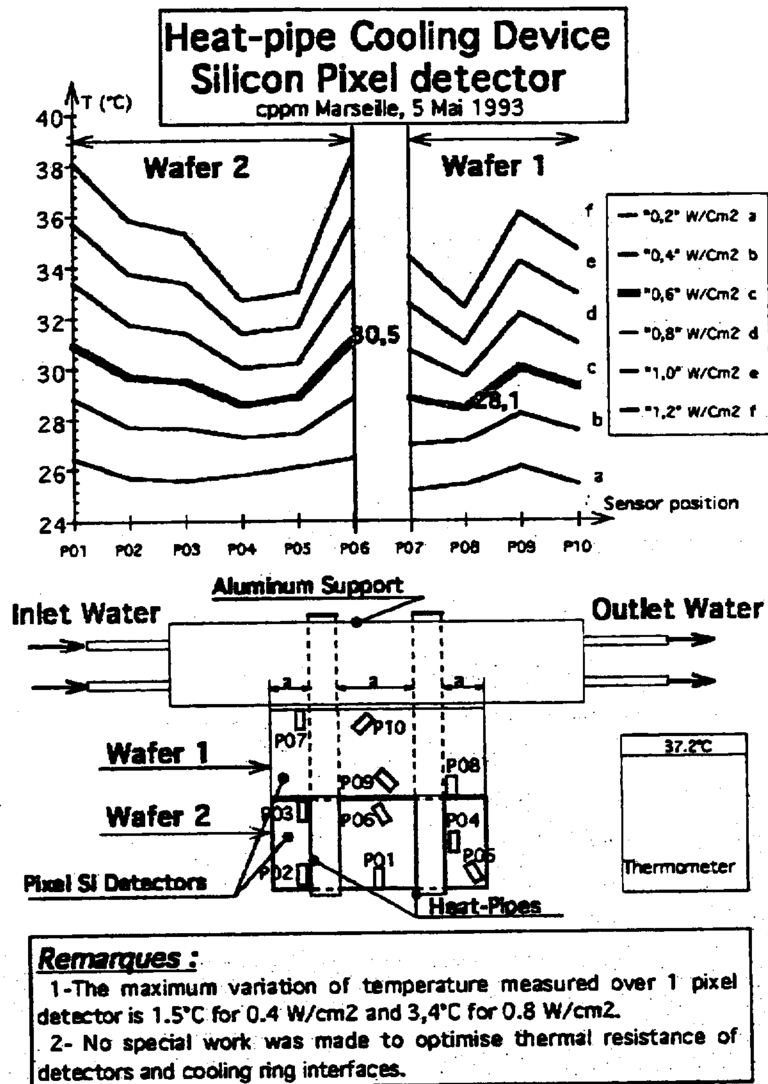


Figure 63: Temperature distribution on a pair of pixel tiles cooled by a pair of Thermacore XH5 heat pipes.

Table 12: Expected radiations on the first layer of the ATLAS Inner Detector at the nominal luminosity of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

	E (MeV)	FLUX 10^{13} cm^{-2} yr^{-1}
protons	850	0.34
Kaons	1200	0.38
Pions	700	4.7
Electrons	100	0.95
Gammas	350	6.2
Neutrons		
direct	750	0.39
albedo	1	0.35

3.3.1 Expected effects on detector performances

The global behaviour of a silicon detector suffering irradiation damage can be mainly summarised by the following two points:

1. Reverse leakage current :

   The leakage current density I_r/v increases quite linearly with the particle fluence Φ according to the equation :

   $$I_r/v = \alpha\Phi \tag{5}$$

   where v is the volume of the silicon detector.

   This leakage current is the main source of parallel noise in the preamplifier input. Nevertheless, since the shaping time constants to be used in ATLAS configuration are very short (about 20 ns), and thanks to the reduced pixel dimension this contribution should be kept at an insignificant level.

   Taking the commonly used α value of 8 10^{-17} A cm^{-1} at 20 °C the leakage current of an ATLAS pixel (150 μm thick) would be about 100 nA after 10 years of operation. However, operation at near 0 °C reduces the leakage current to about 15 nA. This current gives in turn a parallel noise of about 60 e^- rms in the preamp input which is less than the serial noise currently achieved in pixel electronics [29]. Consequently the induced degradation of signal to noise ratio is less than a factor of 2.

   However, as the pixel detector has to be DC coupled, this current flows into the preamplifier input, so that careful design to avoid DC operating point shifts is needed. Some solutions have already been reported and tested [29, 46].

2. Depletion Voltage :

   The depletion voltage of a silicon detector is linearly related to the effective impurity concentration N_{eff}, which is the difference between the donor concentration N_d and the acceptor concentration N_a. In commonly used n-type silicon, the donor concentration is initially slightly higher. Irradiation introduces additional levels in the silicon bandgap, acting like acceptor or donor levels. However, the "donor defects" anneal

rapidly at room temperature unlike the "acceptor defects" which remain stable for a long time. Therefore, the starting n-type material becomes more and more compensated under irradiation, reaches complete compensation (the fluence value for complete compensation depends on the starting material but is usually about 2 10^{12} n.cm^{-2}): afterwards the material becomes gradually more and more p-type material [47, 48, 49] (fig 64).

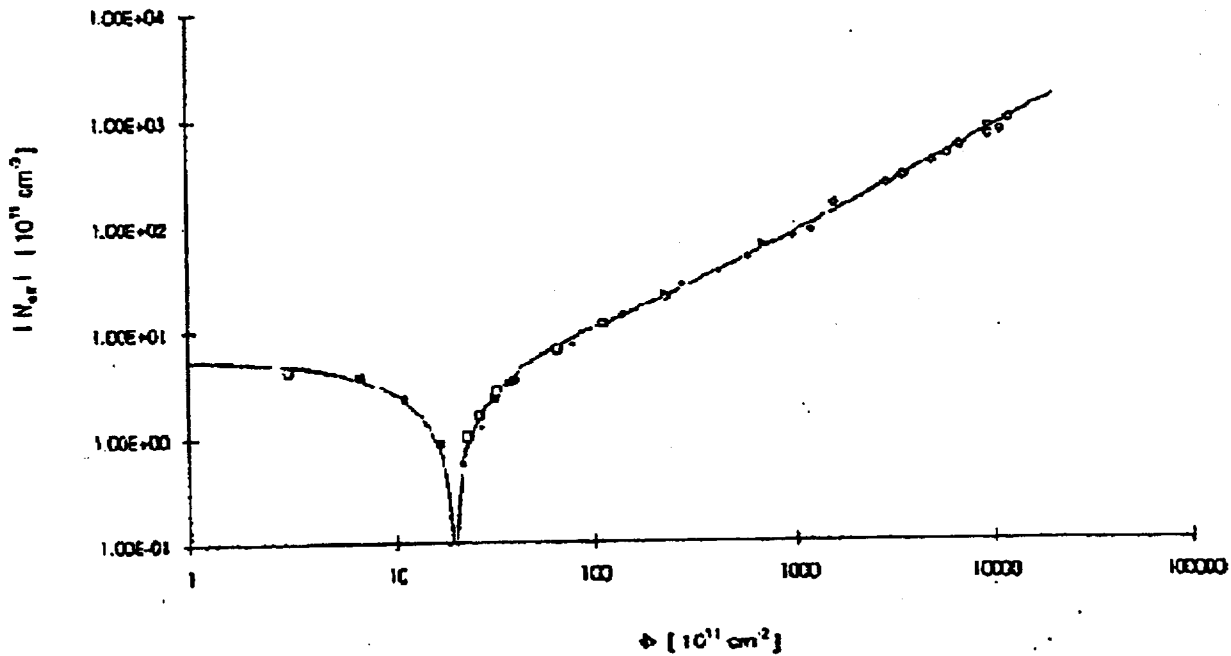


Figure 64: Effective impurity concentration vs neutron fluence.

Consequently the depletion voltage of an n-type detector decreases during the first period of irradiation and then increases rapidly. At the same time, due to type inversion, when the bias voltage is applied the depletion region of the detector (which grew initially from the p+ implant) starts now from the backplane.

Without self-annealing effects, this increase of depletion voltage should be a dramatic problem. According to the fig 64, a 150 μm thick, n-type silicon detector with an initial depletion voltage of about 10 Volts would need around 800 Volts for complete depletion after 5 10^{14} n.cm^{-2}.

Fortunately, the initial damage is known to anneal out in a relatively short time whatever the temperature. Measured values of the depletion voltages are reduced by a factor of 3 a week after irradiation for a detector kept at the room temperature. However, measurements taken over a long period after irradiation showed an important reverse annealing, strongly temperature dependent (fig 65 [50]).

In order to evaluate the long term depletion voltage evolution of a LHC detector, we have to make some assumptions on the LHC operation. Scenario-1 of fig 66 is based on 3 years

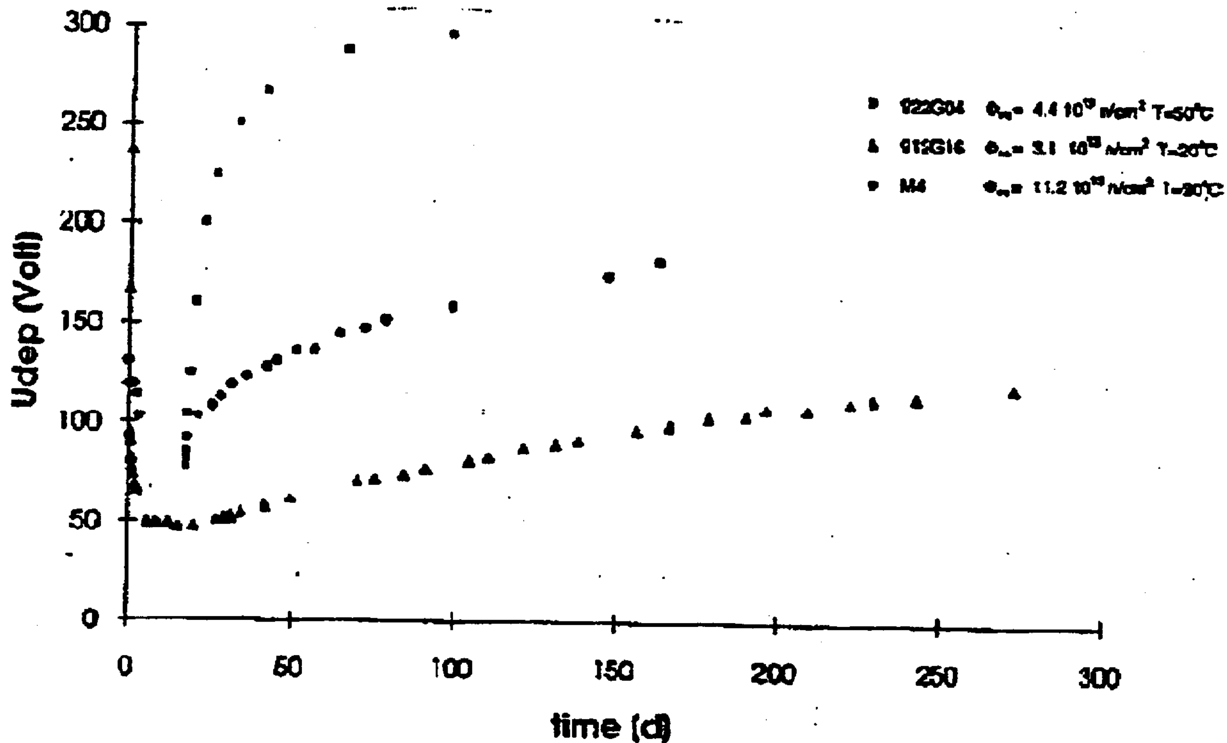


Figure 65: Depletion voltage vs time after irradiation.

at L = 10^{33} and 7 years at 10^{34} at 0°C and with 1 month at 20°C each year (maintenance period). A more realistic scenario is presented in fig 67) with 1 year at 5 10^{32}, 1 year at 10^{33}, 1 year at 5 10^{33} and 7 years at 10^{34} always at 0°C except 1 month at 20°C during the 2 first years of operation and 1 month every two years subsequently. Such scenarios are of major importance to determine the ability of the detector to survive to radiation damages and to fix the optimum operating temperature.

3.3.2 Pixel structure irradiations (CPPM activities)

During the last year we made irradiations on CSEM detector test structures (fig 68). These structures include diodes of various dimensions from (2×2 mm^2) down to (440×90 μm^2). These structures are all made in n-type, 300 μm thick silicon of typical resistivity 5 kΩ cm.

They have been irradiated with 3 types of particles :

- Neutrons using the SARA (ISN Grenoble) irradiation facility up to 2.72 10^{14} n.cm^{-2}. The SARA neutron spectrum has a 6.2 MeV mean energy. The estimated damage coefficient is a factor of about 2 higher than for 1 MeV neutrons.
- 300 MeV protons using the SATURNE (CEN-SACLAY) beam up to 3 10^{14} p.cm^{-2}.
- 238 MeV Pions using the PSI cyclotron beam up to 1.5 10^{14} π^+ cm^{-2}.

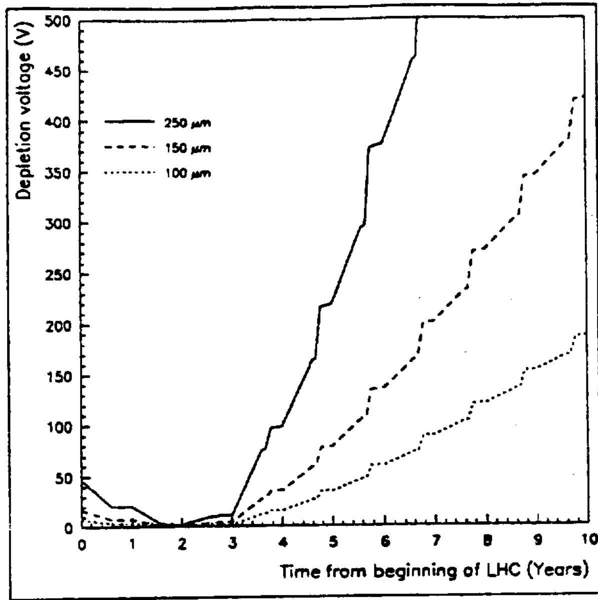


Figure 66: Scenario 1.

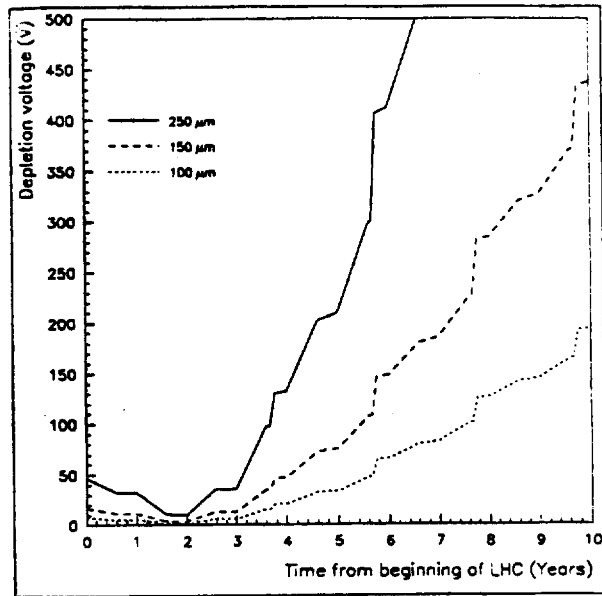


Figure 67: Scenario 2.

During all these irradiations the detector structures were kept at a temperature of 0°C ± 3°C. Immediately after the irradiation the detectors were maintained at a temperature of -18°C in order to suppress the long term reverse annealing effects.

Previous irradiations on CANBERRA and SI structures with 340 × 340 μm^2 diodes had been made with neutrons and protons at room temperature.

Measurements of these irradiated structures are still under way. However some interesting preliminary results can be reported.

3.3.3 Results

1. Leakage current:

   As it can be seen in fig 68, the test structures can be separated into 3 types:

   (a) Individual diodes with individual guard rings (an additional guard ring surrounding all the structures is present but not powered during measurement);

   (b) Individual diodes with a common guard ring ;

   (c) Diode matrices.

   At the first glance, the behaviour of structures (a) and (b) should be the same. However, leakage current measurements exhibit strong differences.

   Figures 69 and 70 show the leakage current density versus reverse voltage for 3 diodes in configuration (a) and (b) respectively, irradiated at 4 10^{13} n(6.2 MeV) cm^{-2}.

   The structures in configuration (a) exhibit a strong current peak located around 100 V which gradually disappears with the increase of the reverse voltage. This peak is absent in the diodes of configuration (b).

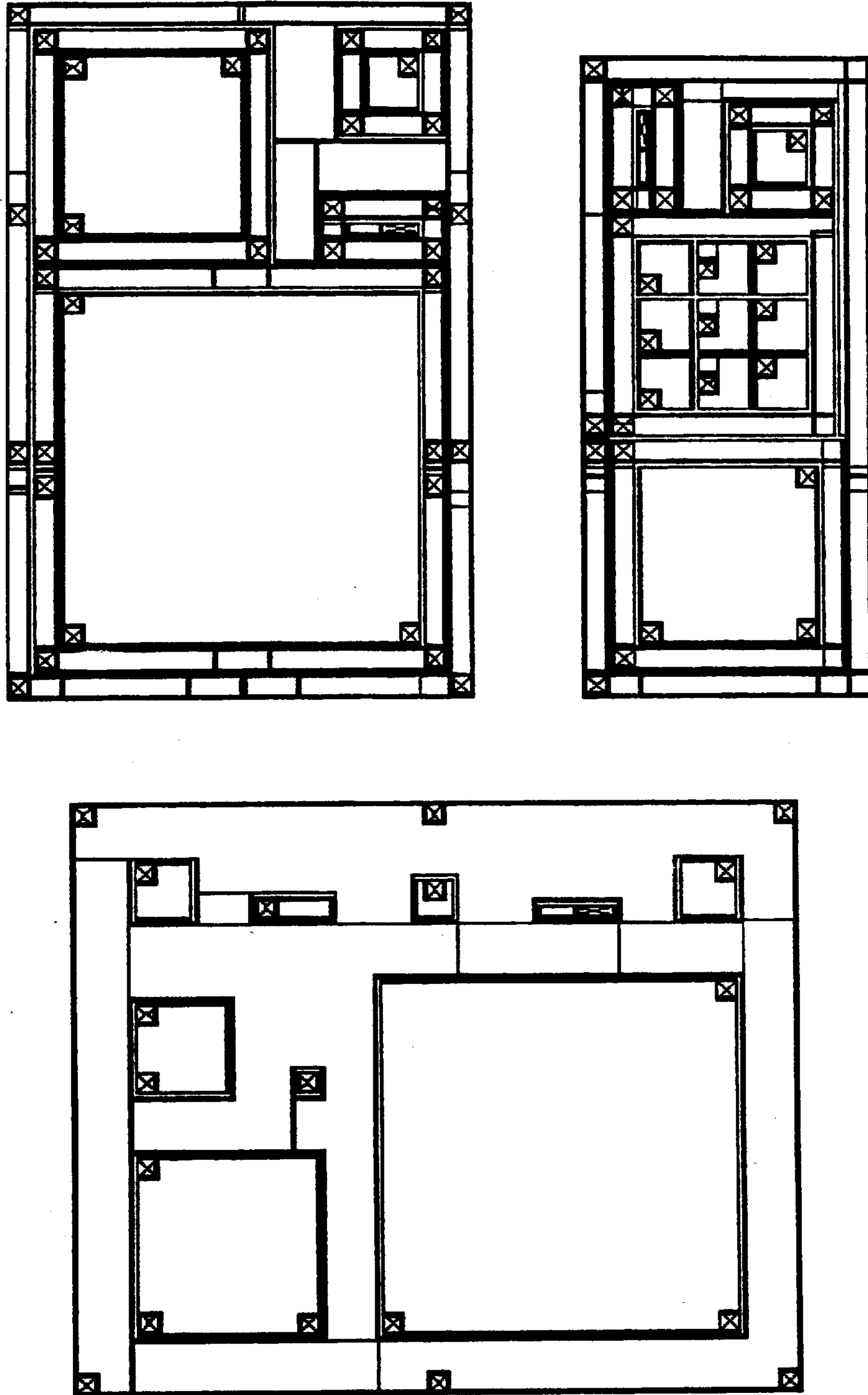


Figure 68: Test structures: with (a) individual Guard ring (upper) and with (b) common Guard ring (lower).

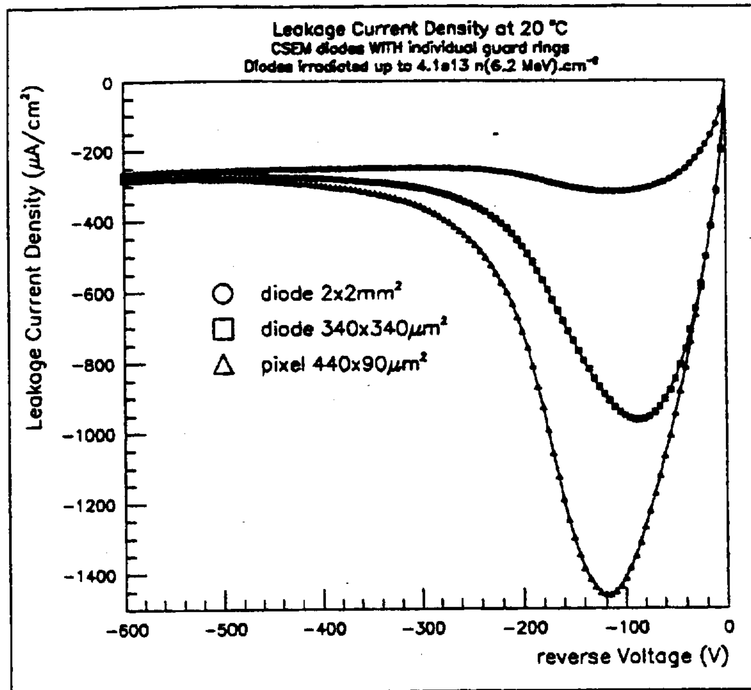


Figure 69: Leakage current density vs reverse voltage for three diodes with individual guard rings, irradiated up to 4 10^{13} n cm^{-2}.

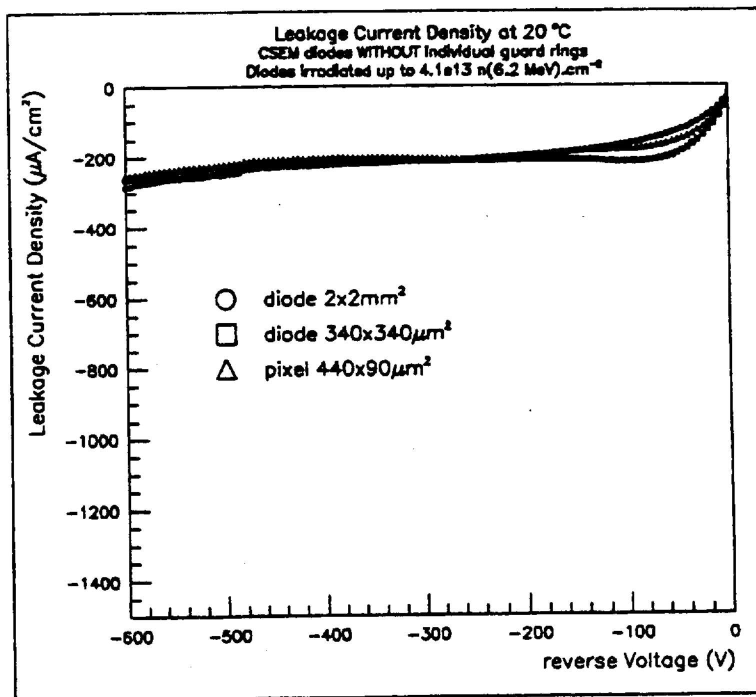


Figure 70: Leakage current density vs reverse voltage for three diodes with a common guard ring, irradiated up to 4 10^{13} n cm^{-2}.

Apart from the peak, the leakage current densities are the same in both configurations.

The origin of this peak is not clearly understood yet; It seems to be due to the conductive layer facing the p+ implant when the detector is not fully depleted (at this irradiation level type inversion has already occurred) allowing charges which are not generated in front of the implants to reach them. In this case, the peak position would be related to the depletion voltage. The peak position also increases quite linearly with the neutron fluence (fig 71) supporting this tentative hypothesis.

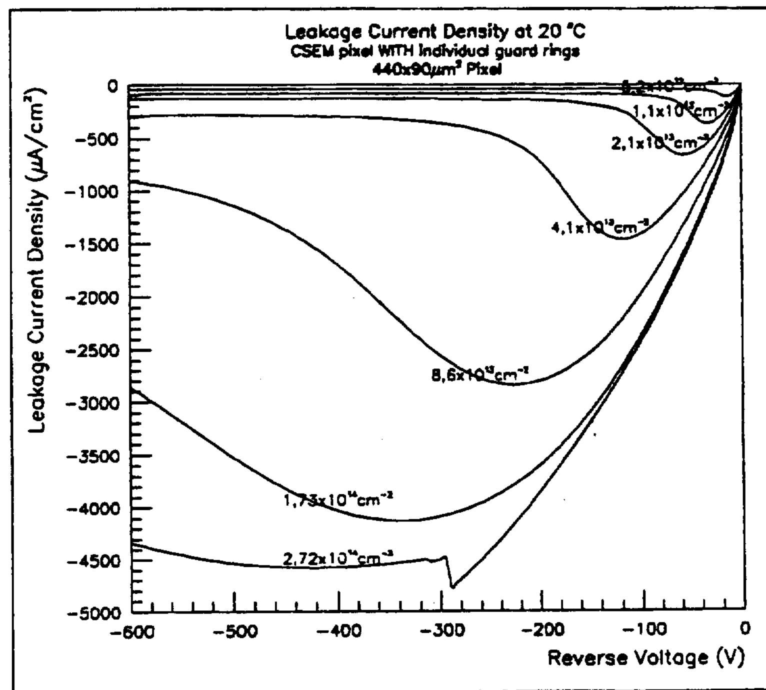


Figure 71: Leakage current density at 20°C for pixels with individual guard rings irradiated up to 2.7 10^{14} n cm^{-2}.

If this is confirmed, the measurement of the voltage at which this peak disappears, could be an indirect method to measure depletion voltage in pixel like structures which cannot be measured easily by conventional method (C-V curves).

2. Determination of radiation damage coefficients

   The damage coefficients α have been determined for 6 MeV neutrons and for pions by fitting reverse current densities for diodes of various dimensions in configuration 2 at 500 V. These data and the best fits are shown in fig 72 and 73 for 6 MeV neutrons and for 238 MeV pions. The damage coefficients are then α = 17 10^{-17} for 6 MeV neutrons and α = 8.2 10^{-17} for pions, in good agreement with the damage coefficients measured by other groups [51].

3. Signal collection

   Signal collection efficiency has been measured in 2 $\times$ 2 mm^2 diodes irradiated up 10^{14} n cm^{-2} using Ru 106 β's. The degradation of the signal collection at this level is

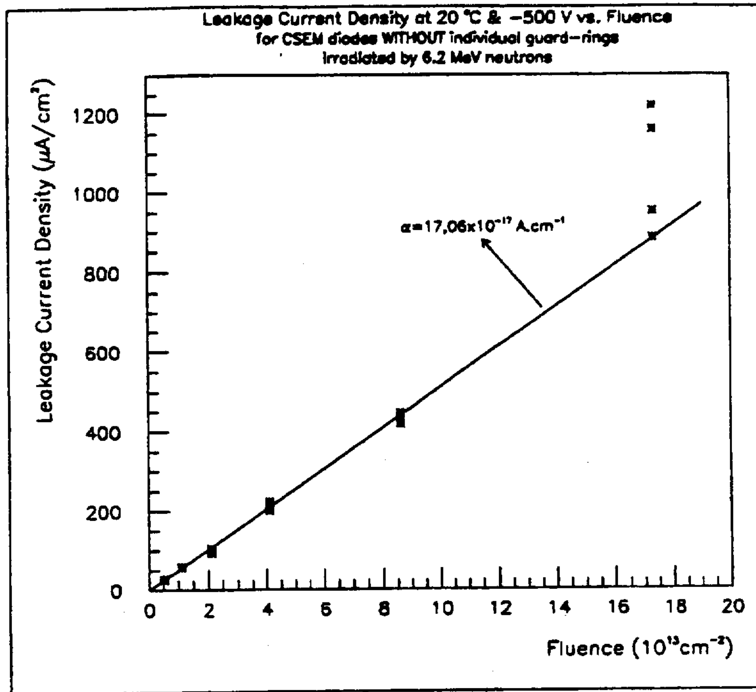


Figure 72: Damage coefficients for 6 MeV neutron irradiation of pixels at 20°C - see text.

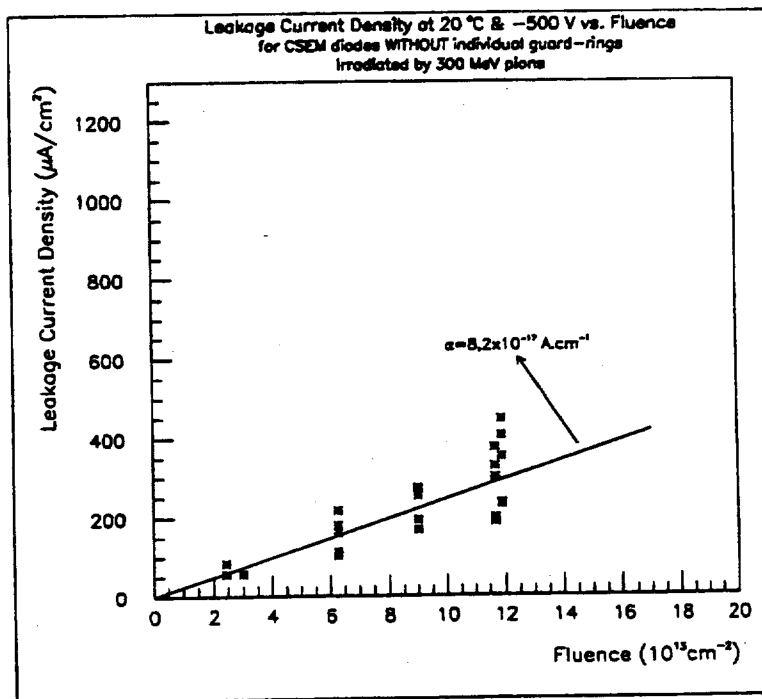


Figure 73: Damage coefficients for 238 MeV pion irradiation of pixels at 20°C - see text.

less than 10 % (fig 74). F. Lemeilleur et al. [51] report similar results. On the more irradiated samples, the extraction of the signal in such large diodes becomes more and more difficult due to increase of reverse current. The small pixel structures will be more adapted to this measurement but extensive measurements cannot be done yet due to the lack of an preamplifier with analogue output well adapted to the pixel dimensions. Moreover, the reduced pixel dimensions add complexity for triggering.

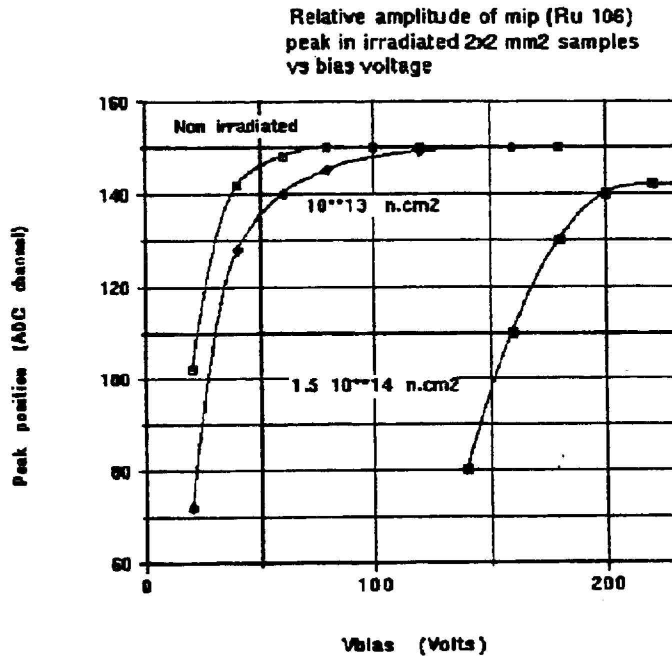


Figure 74: Signal collection efficiency in $2 \otimes 2$ mm^2 diodes irradiated up to 10^{14} n cm^{-2}; measured using ^{106}Ru β's.

Our group has developed a pixel preamplifier suitable for this kind of measurements. This preamplifier is based on a Rad-Hard technology and may even be employed for in-line measurements.

3.3.4 Conclusions and prospects

Like all silicon detectors, pixels suffer radiation damage. However, because of their reduced dimensions they are still the only candidate expected to survive at the very high particle fluxes encountered in the innermost layer of the ATLAS tracker at the nominal LHC luminosity.

Nevertheless, even though the reverse current seems to be manageable, the depletion voltage increase remains a challenging problem. This increase could be managed in various ways : a conservative approach might be to adjust the initial donor concentration of the silicon in order to optimise the depletion voltage variation with respect to the LHC scenario [52]. This approach, combined with a careful study of breakdown voltage of the detector, which is the limiting point for increasing bias, seems to be quite straightforward. An alternative solution might be to decrease the silicon thickness to reduce the final depletion voltage value. The

price to be paid would be a reducted signal to noise ratio, even at the beginning of operation. To avoid this inconvenience, another solution might be to use p-type silicon. In this case, even if the depletion voltage behaviour remains unchanged, we avoid the type inversion problem. Even after radiation damage, the depletion region starts from the implant side. Therefore it might be acceptable to start with a completely depleted detector and to work after few years in partial depletion. The degradation of the signal to noise ratio will start only at this time.

3.4 Bump Bonding and the Multi-chip Module Technique

3.4.1 Introduction

Pixel modules produced at a realistic price, in large enough quantities and sizes to match present microvertex detector typical areas, require at least two state-of-the-art technologies: fine-pitch flip-chip bonding techniques and multi-layered thin film deposited laminates. Indeed, die sizes are very different when considering the detector chip and the electronic chip. Sixteen chips will typically be needed to fill a standard detector module area. Because diodes cover the entire area of the detector, electrical connections between sensitive elements and electronic cells are needed over the full surface of the substrate, which implies the necessity of some flip-chip technique. On the other hand, connections between these chips to the outside have to be provided requiring a high performance interconnection layer deposited over the sensitive substrate.

3.4.2 Flip-chip bonding

Flip-chip techniques have been widely investigated already, through various in-house processes (z-axis conductive adhesives, screen printing of conductive glue) and several proprietary industrial processes (gold ball bumping, solder bumping). Some of these technologies may or may not meet the requirements of ATLAS pixel dimensions (a typical bump diameter of 15 μm is foreseen) Table 13 comparises the various techniques. We plan, however, to continue to study the techniques developed for the WA-97 pixel detector (solder bumping - see for example [53]) and for the DELPHI VFT, including the Seïko/Sony anisotropic film bonding technique since this group proposes a new film with much higher grain density (table 13). Several manufacturers have already proven their ability to produce large areas of bumps of various sizes on detector wafers, but, for the large area of the ATLAS pixel detectors, cost-effective solutions have to be found. Experience with GEC-Plessey is typical. Although they have successfully produced $\geq 10^5$ solder bumps on pixel detectors, they still rely on a manual placement machine, and do not plan yet to move to an automatic bonder. Also they still rely on a 3-mask process for the various metallic layers needed for the growing of the bump. All these points may not favour this technique today, but several changes and evolutions are discussed (cf. the MCM discussion).

For this reason, following the recent announcement by IBM of the release to individual customers of several of their in-house technologies, including the C4 process (controlled collapse chip connection), we have entered into a collaboration with them, in the context of DELPHI VFT upgrade. In this way, we hope to benefit from continuous improvements of the technique over 15 years (which for example allows the use of only one mask for all

the process steps), and of a production rate of 1200 wafers per month. More recently, we have also contacted the LETI, a leading French research laboratory in micro-electronics, to have access to their bump bonding knowledge. This is linked to the fact that this process is compatible with DMILL, a rad-hard technology under evaluation for the implantation of the one of the ATLAS ID electronic chips (see 3.5.2, and with an MCM-D process commercialised by Thomson Hydrides (see 3.4.3.

Two major parameters will be investigated with the various flip-chip techniques under evaluation. First is the bonding yield: we have seen in the DELPHI VFT upgrade project, that a yield better than 99.8 % is obligatory when the number of I/O pads per chip also connected to the substrate by bump-bonding exceeds 30. The other important parameter is the approach distance between two chips. Although we implant larger diodes in these areas to avoid dead zones, the spatial resolution is somewhat degraded, and this region has to be minimised. The ultimate approach distance depends on automatic bonders - that will be used for price and assembly time reduction - which are less precise than manual ones. Some tests have already been performed, with the collaboration of Research Devices Inc, a bonder manufacturer. A careful evaluation of what can be achieved in this field is planned.

Table 13: Comparison of various bumping technologies.

	Diameter/area mils/mils^2	Pitch mils	Pad resist. mΩ/pad	Ball density mm^{-2}	Current density A mm^{-2}
Screen printing conductive glue	30	≥ 10	≤ 200	n.a.	30
Epotek best glue	2	5		n.a.	
A.I.T. fine pitch film	2	3	≤ 200	1000	≥ 5
Seïko/Sony current film	10	15	≤ 1000	4000	
Seïko/Sony new film	2	3	≤ 200	16000	
IBM, as of today	4	9	30	n.a.	
IBM, as foreseen	1	2	≤ 50	n.a.	
gold ball bumps	1.8	2.8	≤ 50		
LETI/Hughes	0.6	2	≤ 60	n.a.	≥ 1

3.4.3 The MCM-D (Multi-chip Module, Deposited layers) approach

The second major concern is the extra space that must be devoted to bussing between the electronic chips, to carry and multiplex power and control lines in and data lines out from the readout logic. These areas present extra dead overlap material in the high acceptance pixel tracker. Also, to minimise the amount of material in the path of detected particles, we need to avoid the use of an extra mechanical substrate, as in the DELPHI VFT, because of the very demanding multiple scattering requirements of the ATLAS pixel detector.

Due to time and financial constraints in for the construction of DELPHI VFT, we chose to start from a proprietary two-metal process from CSEM, our detector supplier, that we improved in terms of line resistivity and dielectric thickness. Two layers are necessary for bussing several chips, and to multiplex their signals. This precludes the benefits of a layer for

shielding purposes, for power distribution with a good equipotential plane or for designing controlled impedance lines when needed. The layout of the power lines for example was very demanding, and two-metal lines were used as often as possible, at the expense of a better shielding/decoupling of the voltage supply. On the other hand we have demonstrated the feasibility of interconnections on a sensitive substrate. The measured voltage drops were compatible with calculations, though still too large to prevent spikes propagating through the electronic chips (to overcome this problem, we had to design a kapton PCB that delivered the supply voltage onto special pads laid out below each chip). The attenuation of logic signals was measured to be negligible. The rise time of the logic signals (driven by a 5 MHz clock) was slowed down by about 30 to 50 %, which was expected from the RC constant of the bussing. From this experience, it is clear that we reached the limits of what could be fabricated by our detector suppliers; the availability of good quality double-sided microstrip detectors is another clear example of these limitations.

For a high performance substrate for the Pixel detector for ATLAS, we obviously have to change our policy and move to the micro-electronics packaging world. In Table 14, we show a comparison of what we achieved in DELPHI, and what is foreseen for ATLAS. The main drawbacks of our previous choice are clearly seen. An MCM is, by definition, an ensemble of several chips interconnected to (or through) a common substrate, the term "chip" referring to a bare die. We will be mostly interested in what is referred as MCM-D, where a finished substrate (ceramic or silicon) is layered with deposited thin-film layers of conductive and dielectric materials, with lines, capacitors and pads patterned by photo-lithography. This differs, for example, from the MCM-C, where the ceramic substrate and the various layers are first stacked, then co-fired, thus the "C".

Table 14: Comparison of the DELPHI and an MCM substrate.

	DELPHI VFT substrate	type. MCM-D substrate
line width	10 μm	10 μm
line pitch	20 μm	20 μm
conductor thickness	1.5 μm	10 μm
conductor material	Al	Al, Cu or Au
ground/power layers	0	2-5
signal layers	2	3
dielectrics thickness	SiO_2 2 μm	Polyimide 25 μm
	Polyimide 5 μm	other polymeres available
via diameter	5 μm	10 μm
line resistance	1 Ω/mm	0.1 Ω/mm

A typical MCM stack is shown in fig 75.

Today's choice of an MCM manufacturer is really wide if we consider only conventional packaging (PLCC, QFP, BGA). Various mechanical support media are in use: conventional laminated PCB, ceramic or silicon isolated metallic substrates. On the other hand, various multi-layered laminates, with new dielectric and capacitive material, thicker conducting microstructures from new alloys, have been developed. Figure 76 shows the benefit of going from alumina to ever newer polymeres as far as frequency response is concerned. We will have to find the optimal combination of conductive and dielectric layers to build the inter-

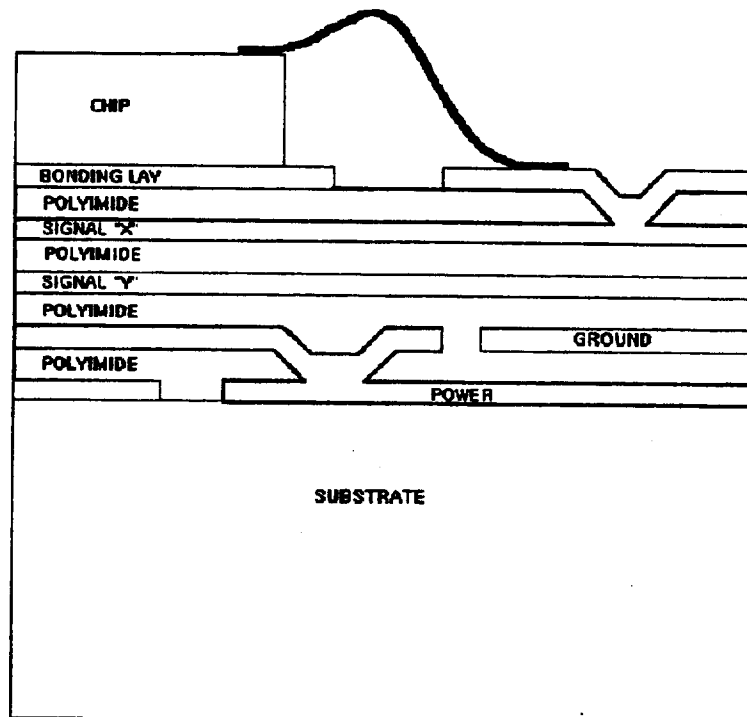


Figure 75: Typical MCM stacking.

connection substrate of our detector module. Several studies have been started with MCM-D manufacturers used to process laminates onto low-resistivity passive silicon wafers. Possible development programmes are being evaluated with GEC-Lincoln and Thomson THY, in particular. These two manufacturers also have additional proprietary flip-chip technologies. Our purpose is to provide these manufacturers with processed high-resistivity detector wafers, with one-metal finishing, so that they can implement a customised 4 or 5 metal layer process. A typical three-step iteration is foreseen. We will first test our detectors on wafers having undergone the full MCM process. Then we will validate the MCM circuitry, when operated on an active substrate. Finally, we will build a module prototype by adding the flip-chip finishing layer to our substrate, for chip bonding.

3.5 Radiation hardness of electronics

We ultimately require analogue circuits that will operate satisfactorily at doses up to about 22.5 Mrad (10 years at 11 cm from the beam) and 6.4 10^{14} n cm^{-2}. CPPM is participating in the development of the DMILL technology in the framework of the RD29 Collaboration [54], and involved in circuit design in the Thompson HSOI3-HD and DMILL technologies.

Several new processing technologies promising radiation resistance in the LHC application are under evaluation. The Thompson HSOI3-HD technology (which promises sufficiently high speed for LHC and survival after a total dose in excess of 10 Mrad [SiO2], and 10^{14} -10^{15} n cm^{-2}) is being studied at CERN (RD9 Collaboration: [55]) and CPPM. The "deep"

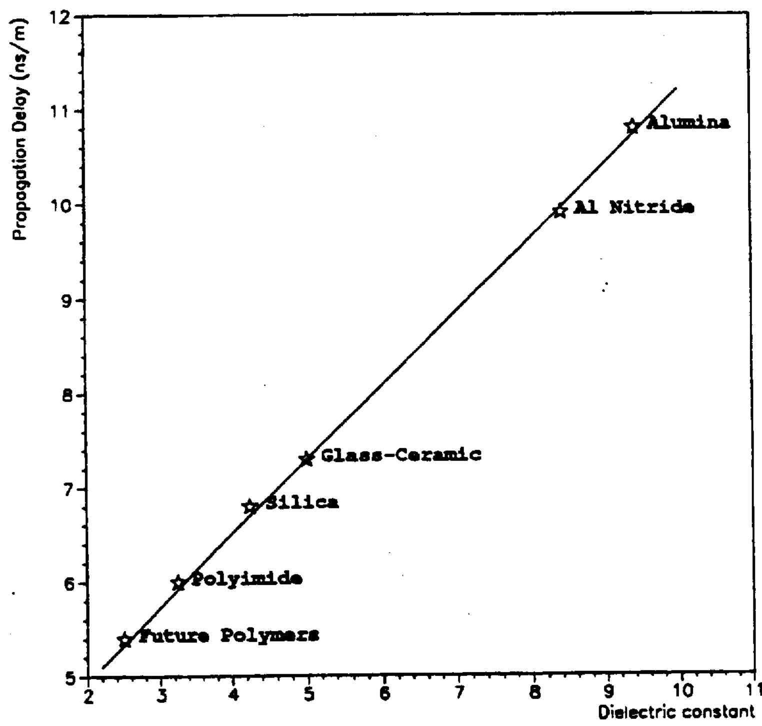


Figure 76: Signal propagation delay vs dielectric constant for commonly used substrate materials.

(1200) active silicon layer "DMILL" SOI technology under evaluation by the RD29 Collaboration [54], allows implementation of CMOS, JFET and bipolar elements for digital and analogue circuitry. The process appears hard to $\geq$ 10 Mrad [SiO2], and $\geq 5.10^{14}$ n cm^{-2}. A number of prototype pixel readout elements have been fabricated in the HSOI3-HD and DMILL technologies, and complete unit cell designs are planned. Other radiation hard processes under investigation in the United States for possible pixel readout include those of United Technologies Microelectronics Co., Harris and Honeywell.

In the following we describe the most important characteristics of the Thompson HSOI3-HD and DMILL technologies for pixels.

3.5.1 DMILL characteristics

DMILL [54] ("Durci Mixte sur Isolant Logico-Linéaire") is a radiation resistant technology for analogue and digital design. It has been under development since 1989, and it was recently announced (19/11/93: CERN Micro electronic User Group meeting) that the process is now available for use by the High Energy Physics community, with industrialisation planned for 1996. The DMILL substrate is a SOI (SIMOX) wafer but with an epitaxial layer of 1 μm. Present results from γ and neutron irradiations on elementary transistors in the four types (NMOS, PMOS, PJFET and NPN) currently available in DMILL show a high degree of radiation hardness. PJFETs, the most radiation hard transistors, show almost no change after γ irradiation up to at least 10 Mrad (SiO2):

- Pinch-off Voltage Shift : $\Delta V_p = 0$
- Transconductance : $\Delta g_m/g_m \leq$ -1 %
- Drain Current in OFF Mode: $I_{DOFF} \leq$ 20 pA;

and only a little change (ΔV_p = -300 mV; $\Delta g_m/g_m \leq$ -10 %) after neutron irradiation up to 5.10^{14} n cm^{-2}(1 MeV). Following an irradiation of DMILL PJFETs with 500 MeV protons from the SATURNE accelerator at Saclay, we observed a low sensitivity of these devices up to fluences of at least 5.10^{14} pcm^{-2}: (ΔV_p = -340 mV; $\Delta g_m/g_m \leq$ -10 %, $I_{DOFF} \leq$ 7 pA).

CMOS devices are almost insensitive to neutron irradiation. After a dose of 6.10^{14} n cm^{-2} (1 MeV), the observed degradations were: (ΔVt_n = -20 mV; ΔVt_p = -80 mV; $\Delta g_m/g_m = 0$). The devices are much more affected by ionisation however, with some changes in threshold voltage $\Delta Vt_{n,p}$ particularly if biased during irradiation. For a dose of 10 Mrad (SiO2), γ or protons, we have found:

- (ΔVt_p = -400 mV; $\Delta g_m/g_m \leq$ -10 %; $I_{DOFF} \leq$ 10 pA) for NMOS biased at V_G = +5 V;
- (ΔVt_p = -800 mV; $\Delta g_m/g_m \leq$ -25 %; $I_{DOFF} \leq$ 10 pA) for PMOS biased at V_G = -5 V.

If the circuits are unbiased during irradiation, the Vt shifts are much reduced.

Bipolar transistors are sensitive both to ionisation and displacement damage. We have found, however, that the gain of NPN transistors remains $\geq$ 30 after proton irradiation to at least 3.10^{14} p cm^{-2} (500 MeV): equivalent to 4.7 10^{14} n cm^{-2} (1 MeV), and 11 Mrad, which is acceptable for circuit design. Further irradiations with protons and pions are planned.

A number of prototype circuits have been implemented in the DMILL technology. Those so far tested include a charge amplifier incorporating PJFET, NPN and CMOS transistors, a CMOS dynamic shift register and a wide band BiCMOS analogue buffer. The amplifier has a (measured) rise time of 20 ns, power consumption of 50 μW and gain of 15 mV/e^-, for an area (50 x 50) μm^2. The shift register contains 33 dynamic stages, each of area (30 x 34) μm^2, and has a set up and hold time of about 1 ns. The wide band analogue buffer has performed satisfactorily at speeds up to 130 MHz with capacitive loads up to 12 pF. Also implemented is a complete RD19 pixel matrix, which in preliminary testing appears to perform as expected. It is planned to re-evaluated the performance of all these test circuits after realistic radiation doses, simulating the LHC environment. A gain change of 10 % is seen in the charge amplifier following (a very recent) irradiation with 20 Mrad of protons. With these developments, we aim to have this technology well tuned for the needs of LHC microelectronics.

3.5.2 Work on the Thomson HSOI3-HD process

In the LHC (Large Hadron Collider) project there is a very stringent need for radhard technologies, especially for systems close to the beam interaction. For inner detectors located at 11.5 cm from the beam pipe, extensive simulations have shown that doses as high as 22.5 Mrad(Si) and fluences as high as 6.4 10^{14} n/cm^2 are to be expected for ten years operation [4]. Specially hardened technologies are therefore needed. Furthermore, most applications require high speed, low noise and low power analogue and digital integrated systems. Consequently a huge amount of effort is to be put in the characterisation and qualification of the very few emerging radhard technologies.

SOI (Silicon On Insulator) technologies are believed to possess some intrinsic radhard properties. Furthermore, from the circuit design point of view, SOI has very interesting properties. Some of these features include latch-up free operation. Latch-up is a well known parasitic phenomenon that can be more annoying in a radiation environment. In SOI circuits the active volume is considerably less than that of equivalent bulk devices. Again this is a positive point where hardening is concerned: the impinging particles have less active volume to damage. Additional properties include reduced parasitic capacitances and junction size. This can help in high speed applications and also in reducing leakage currents. On the other hand SOI has some original drawbacks not present in the bulk case. One of the most important aspects is the presence of a thick back oxide in which charges can be created by ionising radiation. This tends to increase the sensitivity of SOI devices to this type of radiation. Extensive studies on the properties and drawbacks of SOI can be found in [56] and the references therein.

The purpose of this report is to present some results on the hardness of the Thomson SOI3HD, an SOI CMOS process, to protons and neutrons.

1. The SOI3HD process

   SOI3HD is a radiation hardened 1.4 μm, SOI-CMOS process developed by the LETI laboratory (of the French Atomic Energy Agency) and is now industrialised by

THOMSON-TCS [57, 58]. Figure 77 depicts a simple structure showing two transistors. The SOI material is obtained by oxygen implantation Notice the low active volume and the dielectric isolation of the devices. The silicon film is 150 nm thick.

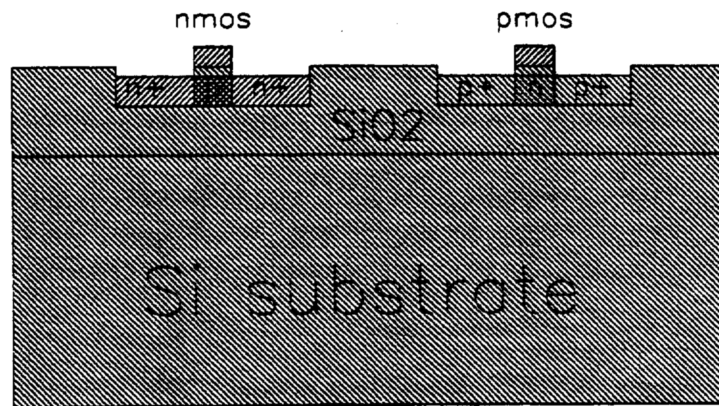


Figure 77: A simplified view of an SOI structure.

2. Proton irradiation

   In order to assess radiation hardness of any given process, a lot of characterisation effort has to be deployed. This is because the radiation interaction with the various devices is a very complex process. Various effects, different in nature, depend on many parameters like the nature of the irradiating particle, its energy, mass and charge. The damages depend also on the process and on the various fields present in the device. Protons are one of the most damaging particles. Their effects include both displacement damage (also be caused by neutrons), and ionising damage (direct and indirect). Their effects include the creation of energy levels in the bandgap, creation of scattering centers, photocurrents and, most importantly for SOI-CMOS, charge buildup. We have carried out two proton irradiation runs at 300 MeV and 500 MeV at the SATURNE national laboratory in Paris. Here we report only on the first batch. Results from the second batch were very similar.

   The pulsed proton beam, 2 cm in diameter, was monitored on-line and calibrated with activated carbon foil. The flux varied between 10^9 and 5 10^9 p/cm^2/sec. As consequence, the dose rate was not constant during the experiment. For the first 300 Krad the dose rate was about 200 Krad/hour From 300 Krad(Si) to 1 Mrad(Si) the rate was estimated to be 400 Krad/hour. From 1 Mrad(Si) to 3 Mrad(Si), it was 300 Krad/hour. An abrupt increase took place at the 6 Mrad(Si) point where the rate reached 2.3 Mrad(Si)/hour for few seconds. From then, and to the end, the irradiation carried on at a constant rate of about 1 Mrad/hour.

   For single devices, six measurement points are considered. The cumulated absorbed doses in silicon at these points along with corresponding proton fluences are as shown in table 15:

Table 15:

Dose(Mrad)	0.309	1.4	4.68	7.94	11.24	22.7
p/cm^2 (10^{14})	0.064	0.289	0.96	1.64	2.31	4.68

We first present the radiation effects on the basic device parameters: the threshold voltage, subthreshold slope, transconductance, etc... Unless otherwise indicated the results are for N and P transistors with (W/L) drawn=23.7/2.3 with lateral and central contacts. These are standard transistors drawn according the design rules provided by Thomson TCS. Effects on some simple circuits are also reported. All the following results, unless otherwise indicated, are from in-situ measurements. For each measurement point the irradiating beam was stopped to unplug the bias bus and connect the measurement one. The average time between the interruption of the beam and the end of the measurement was about 30 minutes. The only exception is at point number 5 (7.94 Mrad) where the time between the interruption and the measurement was, for safety reasons, about 5 hours. As a consequence, the results include the annealing effects during the dead time. This annealing is to be added to the normal annealing that occurs during irradiation.

3. Threshold voltage shift

The threshold voltage (VT) is the most important intrinsic parameter of a MOS device. It is also the main parameter affected by ionising radiation. Variations of threshold voltages alter directly the bias situation of any analogue circuit. This can cause the circuit to malfunction at the nominal supply voltages and bias currents. Transistors may quit the saturation region or may get more saturated, for example. This can lead to a variation in the input linear range, low frequency gain, bandwidth, noise and linearity. The speed of digital circuits is also directly related to this parameter.

Figure 78 depicts the evolution of the threshold voltage shift of biased and unbiased N devices versus ionising dose. The bias condition during irradiation are $V_D = V_S = V_{Back}=0$ for both devices, and $V_G=0$ for the unbiased device and $V_G=5V$ for the biased one. The threshold is extracted in the linear region at $V_{DS}=50$ mV. The maximum voltage shifts are -135 mV and -146 mV for the unbiased and biased transistors respectively. The former shows a faster recovery behaviour, to end up with a rebound of about 50 mV at the end of the irradiation period. These shifts are very low, showing a good hardness of these devices as far as this parameter are concerned. The non monotonic behaviour is a well known phenomenon [59]. It is related to the evolution and the kinematics of both interface traps and oxide traps. Nevertheless, annealing effects are to be at looked very carefully. We measured a maximum rebound of 0.4 V for an unbiased transistor after 6 months at room temperature. The positive threshold shift of all measured N devices that were biased during irradiation is found to be less than 0.1 V.

Figure 79 depicts back gate threshold voltage shift. This parameter drops very sharply during the first Mrad(Si) absorbed and decreases sub-linearly afterwards. The maximum shift is about -24 V for both biased an unbiased devices. The final back threshold is about 5.5 V. The behaviour of the back gate threshold is a very important factor. If

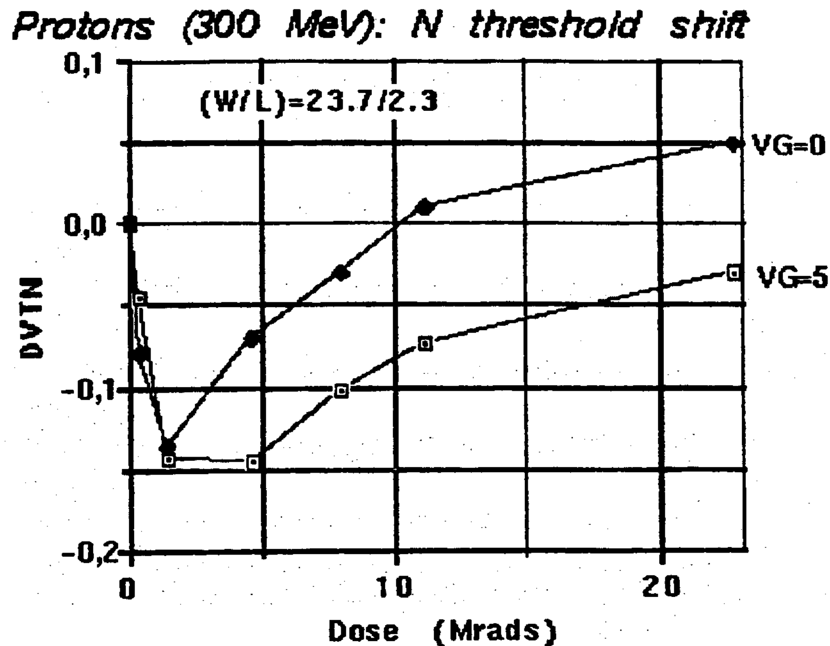


Figure 78: NMOS threshold voltage shift versus dose

it decreases to a certain level it can impede the circuit performance. Leakage current increases and back channel may become inverted. A back threshold voltage of 5 V is still an acceptable value if the back gate is biased accordingly. The back interface being initially in the accumulation mode would gradually move to a depletion mode as the irradiation lowers the back threshold voltage. The behaviour of the device (transconductance and noise) will change accordingly. A further study is needed to investigate this point.

Threshold voltage shifts versus dose of PMOS transistors are depicted in figure 80. The worst case occurs when the device is unbiased where the shift attains about -0.95 V. This is by far the most critical effect we encountered. Extreme care is to be taken in using and biasing this device. This effect is most harmful when the circuit supply is not adequately high. Special attention is to be given to the analysis of the PMOS device and its role in the overall circuit behaviour. For the biased transistor the maximum shift after about 23 Mrad(Si) is about -0.75 V. The rebound at point 6 is a rather an unusual behaviour which we cannot explain.

The evolution of the back gate threshold voltage is shown if figure 81. The shift at the end of the irradiation is about -22 V for both devices. It moves from -13 V to -35 V. This is a rather positive point for the PMOS. Radiation renders the back channel more and more blocked.

4. Subthreshold slope

The subthreshold slope is a very important parameter of analogue circuits designed with transistors operating in the subthreshold region (also called weak inversion re-

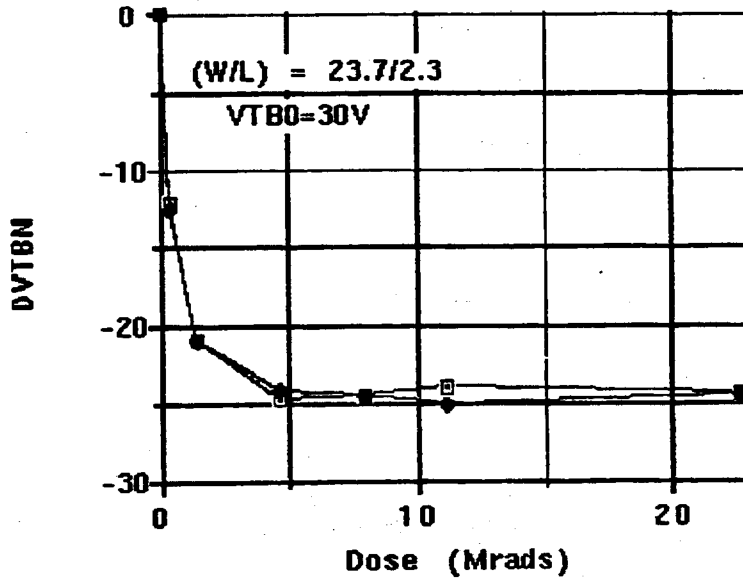


Figure 79: NMOS back threshold voltage shift versus dose

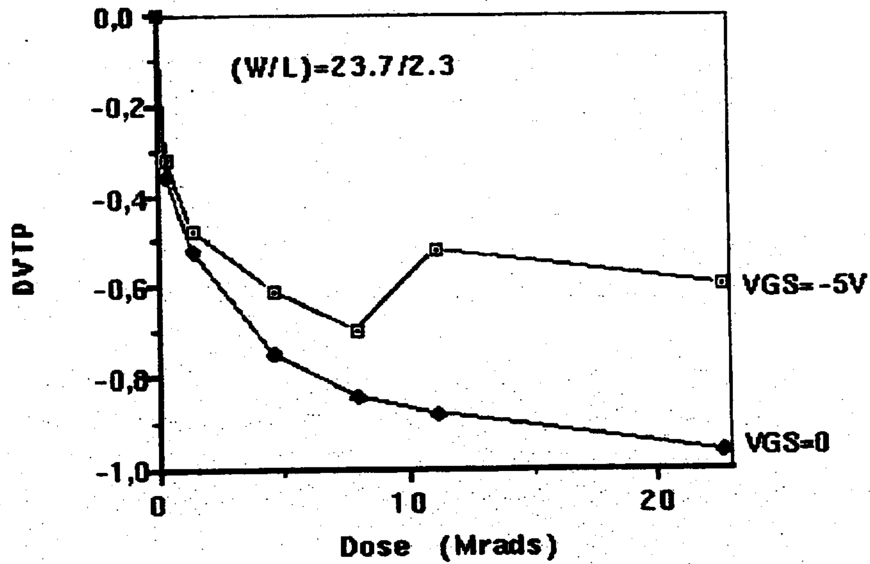


Figure 80: PMOS threshold voltage shift versus dose

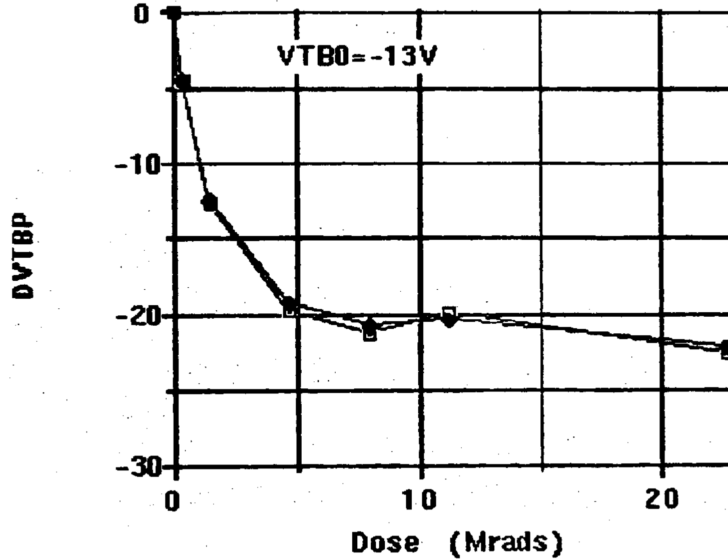


Figure 81: PMOS back threshold voltage shift versus dose

gion). It determines the maximum gain that can be achieved and gives an idea on how fast can a transistor be turned on. The subthreshold slope is defined as the inverse of $\delta VG/\delta logID$. It is given by [56, 59]:

$$S = (kT/q)ln(10)(1 + (C_D + C_{it})/C_{ox}) \tag{6}$$

where C_{ox} is the oxide capacitance, C_D is the depletion capacitance and C_{it} is the capacitance associated with interface traps (C_{it} = q N_{it}). This parameter is a major tool in analysing device behaviour because it is directly related to interface states. Some techniques, that use this region, have been suggested to extract the density of oxide and interface traps [59, 60]. The evolution and the kinematics of such traps determine those of the threshold voltage as mentioned earlier. Low frequency noise is also closely related to interface traps. An increase of these traps is synonymous to an increase of noise.

As shown in figures 82 and 83, S increases in absolute value with increasing dose for both the P and N transistors. Notice that The P device starts with a lower S and is less sensitive to irradiation than the N device. For the former, S begins at -81 mV/dec and reaches -143 mV/dec after 23 Mrad. For the N transistor it starts at 114 mV/dec and end up with 220 mV/dec. The PMOS shows a better behaviour than the NMOS as far as this parameter is concerned.

5. Transconductance (g_m)

   MOS transistors are chiefly used as voltage to current converters (transconductors). The gain-bandwidth product of an amplifying circuit is mainly determined by the

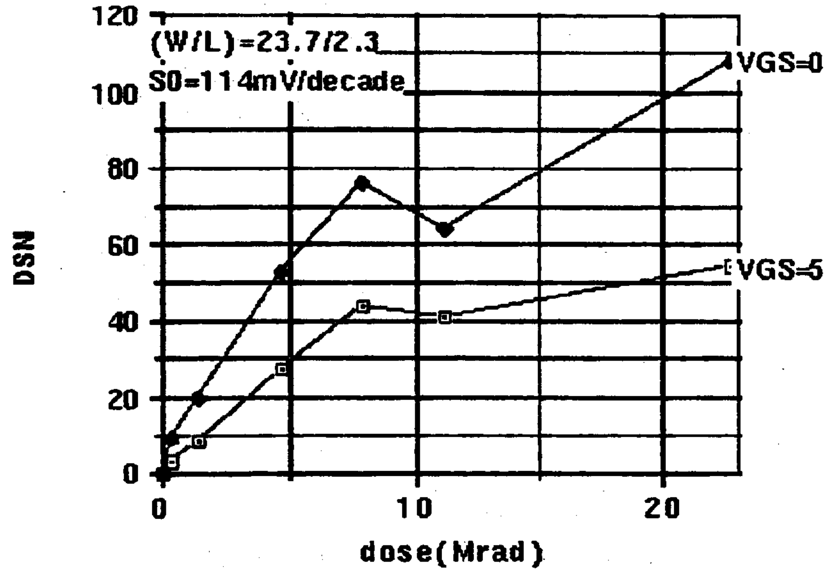


Figure 82: N subthreshold slope degradation

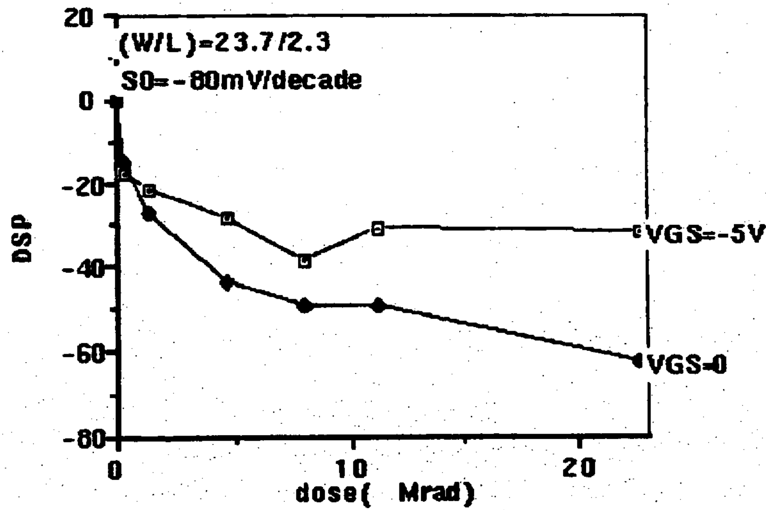


Figure 83: N subthreshold slope degradation

transconductance of the input device. So it is important to determine how this parameter changes with irradiation. At a given bias current, the transconductance can be degraded through the degradation of the carrier mobility. The mobility can change because of displacement damage (neutrons and protons) which results in an increase of scattering centers. An increase of the interface states can also lead to a degraded mobility. Figures 84 through 85 show the transconductance of N transistors versus drain current before and after irradiation at different doses. It is interesting to note that up to a certain threshold drain current the post-irradiation g_m is higher than the pre-irradiation one. Figure 84 and 85 show how the g_m of the same device changes as the dose increases. Above the threshold current, the transconductance is lower after irradiation. The latter effect would indicate that mobility degradation at this critical vertical field is no longer compensated by the increase of the transconductance. The maximum relative increase of g_m is about 5 % and 0.5 % for biased and unbiased devices respectively. The worst relative change (in the velocity saturation region) is -10 % and -15 % for the two transistors after 23 Mrad(Si).

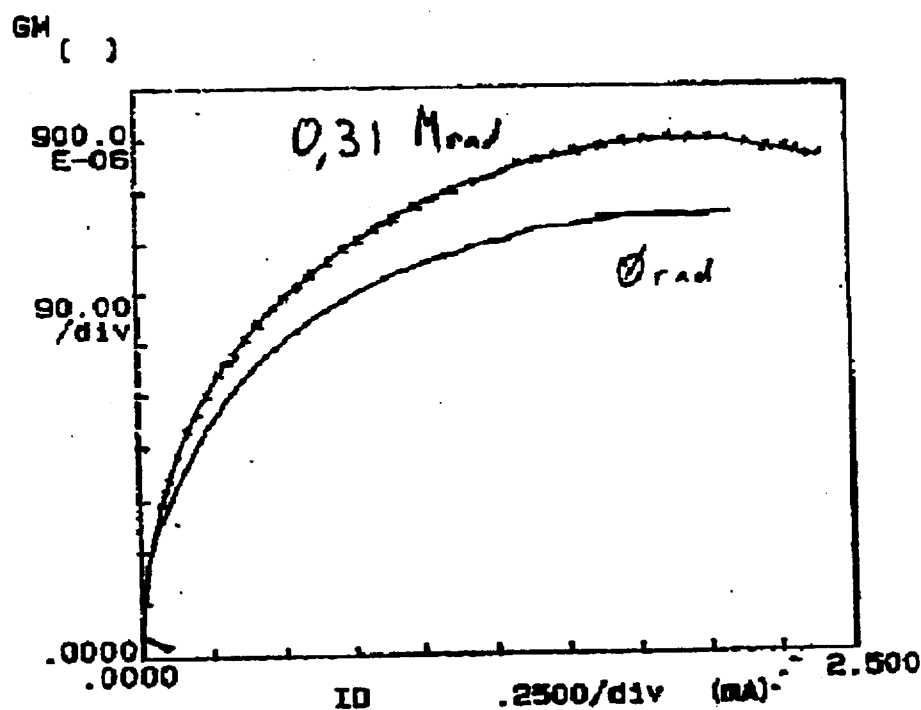


Figure 84: Transconductance of an NMOS versus drain current before and after irradiation (300 Krad).

Transconductances of a PMOS device before and after 23 Mrad(Si) are shown in figure 86. It always decreases with irradiation. The worst relative change is about -20 %.

We extracted the transconductance factor k = $\mu_{eff}C_{ox}$ in the linear region (v_{ds}=50 mV). Where μ_{eff} refers to the effective mobility. A plot of this parameter versus dose is shown in figure 87. The monotonic decrease of k reflects the mobility degradation due to irradiation.

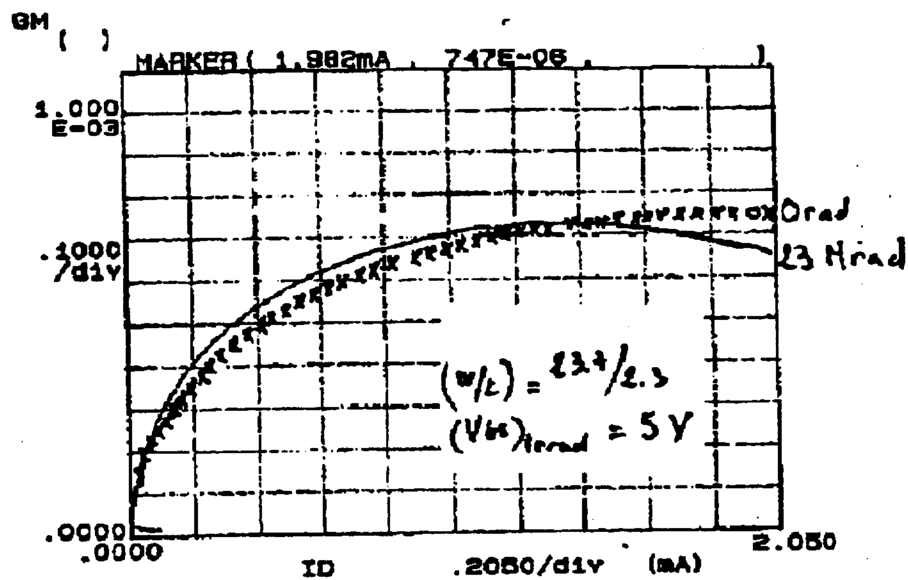


Figure 85: Transconductance of an NMOS versus drain current before and after irradiation (23 Mrad).

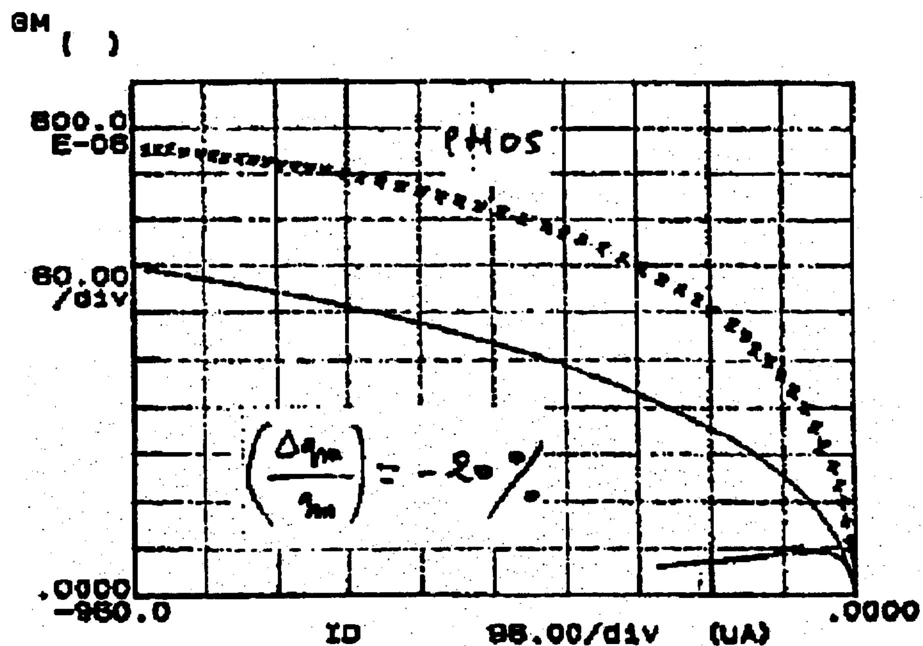


Figure 86: Transconductance of a PMOS versus drain current before and after irradiation (300 Krad).

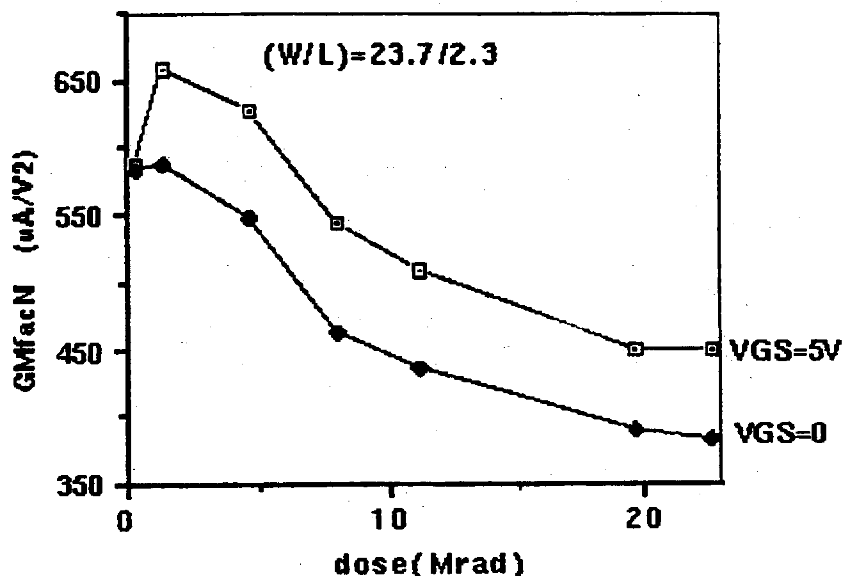


Figure 87: NMOS transconductance factor versus dose

We believe that the increase of the transconductance mentioned earlier is related the state of the back interface. This interface is initially accumulated, then gradually becomes - under the effect of irradiation - depleted. It is well known that a depleted SOI transistor with back accumulation has a lower transconductance than that with a depleted interface [56]. It is also known that the former device exhibits a more severe kink effect. As mentioned in a later section, the kink effect is also found to decrease with ionising irradiation. The hypothesis that this behaviour is related to the back interface can supported from measurements of non irradiated devices. As shown in figures 88 and 89, a transconductance increase and a kink decrease is observed when the device is operated at back gate voltages approaching the back gate threshold.

Supposing that μ_{eff} is the only parameter that changes in the expression of k, their relative decreases are about -23 % and -34 % for biased and unbiased devices. The transconductance factor of a PMOS device is shown in figure 90. The relative changes are 18 % and 28 % for biased and unbiased transistors at the end of the irradiation.

The conclusion is that a relative degradation in mobility of about 30 % is to be expected for both N and P devices after 23 Mrad(Si).

6. Output conductance (g_{ds})

   The output conductance of devices plays an essential role in the functioning of almost any analogue building block. Hence it is necessary to investigate the effect of radiation on this parameter. Because g_{ds} depends on the drain current, it is rather interesting to investigate the ratio g_{ds}/I_d at a constant drain voltage. g_{ds}/I_d is referred to, in some simulation models, as λ. The λ parameter models what is called the channel length

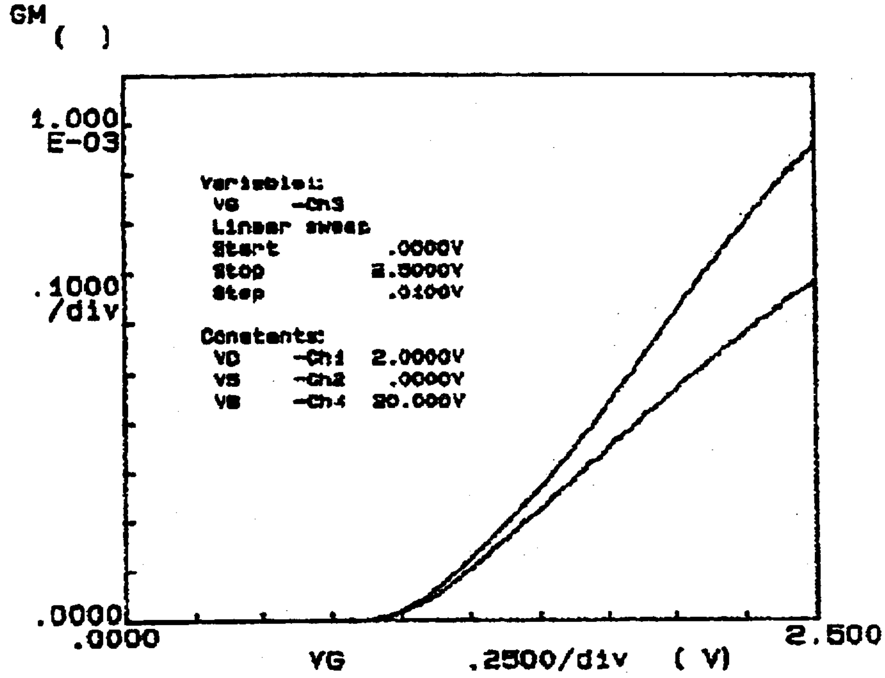


Figure 88: Transconductance of a non irradiated NMOS device (W/L = 65/5) @ Vback=0V (lower trace) and @ Vback=20V (upper trace). Back threshold voltage is 30V

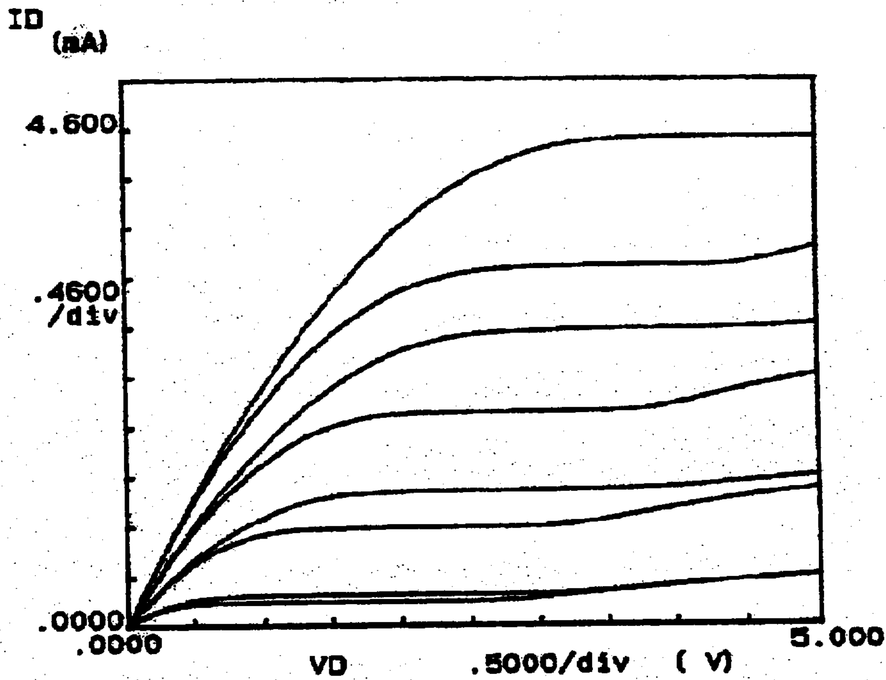


Figure 89: Ids Vs Vds for non irradiated NMOS device (W/L = 65/5) @ Vback=0 (lower trace with kink) and @ Vback=20V (upper trace). Back threshold voltage is 30V

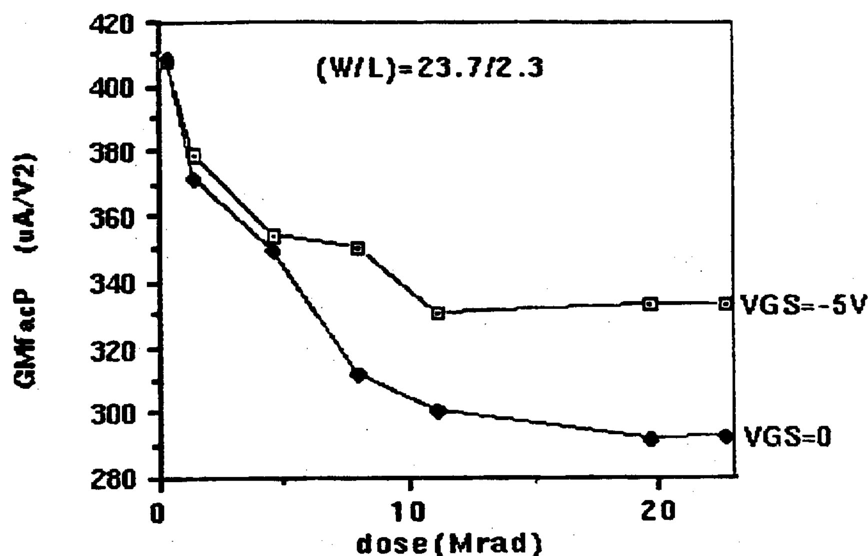


Figure 90: PMOS transconductance factor versus dose

modulation. It has units of 1/V and is the equivalent of the inverse "early voltage" in bipolar devices. A plot of λ as function of drain current for several irradiation doses is shown in figure 91 and 92 for biased and unbiased transistors respectively.

Both charts indicate, that at all irradiation levels, the output conductance is lower for irradiated devices at currents less than about 400 μA. At higher currents the pre-irradiation conductances are much lower than the post-irradiation values. This conclusion is of a paramount importance for circuit design: especially since similar results were obtained for the transconductance, where it was found that g_m is higher for irradiated devices for currents lower than a critical value. One should expect that small signal behaviour of circuits biased correctly would not suffer from irradiation. For PMOS transistors the post-irradiation output conductances are less than the pre-irradiation values for all currents investigated at doses higher than 500 Krad. Figure 93 shows results for the non biased transistor. PMOS devices are primarily to be used as load devices since their transconductance is more degraded than that of the NMOS transistors, while their output resistance becomes higher after being irradiated.

A related parameter is the kink conductance (g_{dk}), which is the abnormal increase of drain current with drain voltage. As mentioned earlier, this conductance is found to decrease after irradiation. Figure 94 depicts normalised g_{dk} versus absorbed dose. Figure 95 shows how the drain voltage (V_{dk}) at which the the kink phenomenon starts to be visible (V_{drain} at which $g_{dk} \geq g_{ds}$). This, along with the transconductance enhancement, are positive side effects of irradiation on NMOS device in this technology. Nevertheless a detailed analysis is needed to deeply investigate all the related phenomena (particularly noise).

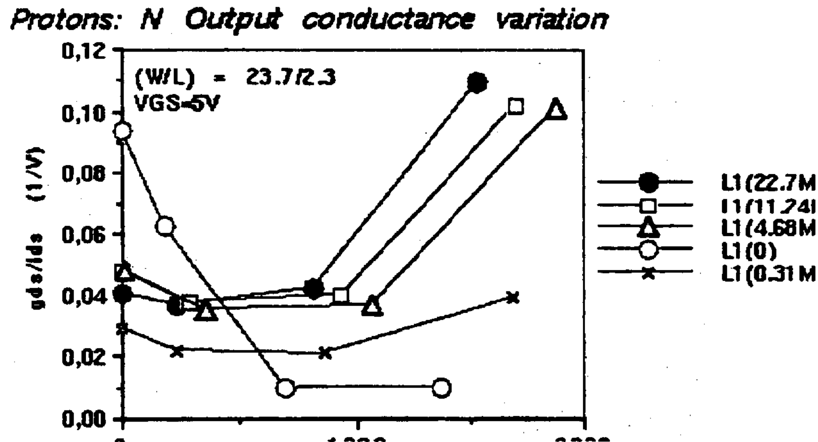


Figure 91: NMOS: g_{ds}/I_{ds} versus I_{ds} at V_{ds}=2.325 V. As indicated in legend the four curves correspond to doses of 310 Krad(Si), 4.68 Mrad(Si), 11.24 Mrad(Si), 22.7 Mrad(Si) along with the initial curve.

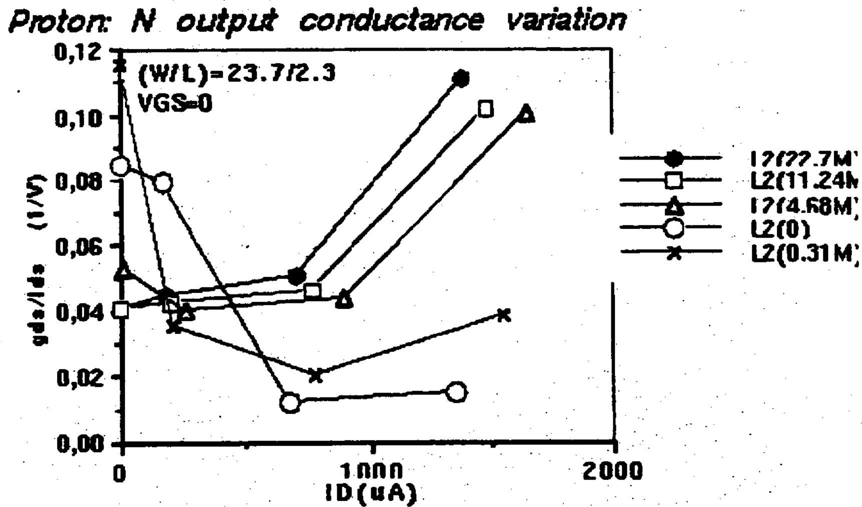


Figure 92: NMOS: g_{ds}/I_{ds} versus I_{ds} at V_{ds}=2.325 V. As indicated in legend the four curves correspond to doses of 310 Krad(Si), 4.68 Mrad(Si), 11.24 Mrad(Si), 22.7 Mrad(Si) along with the initial curve.

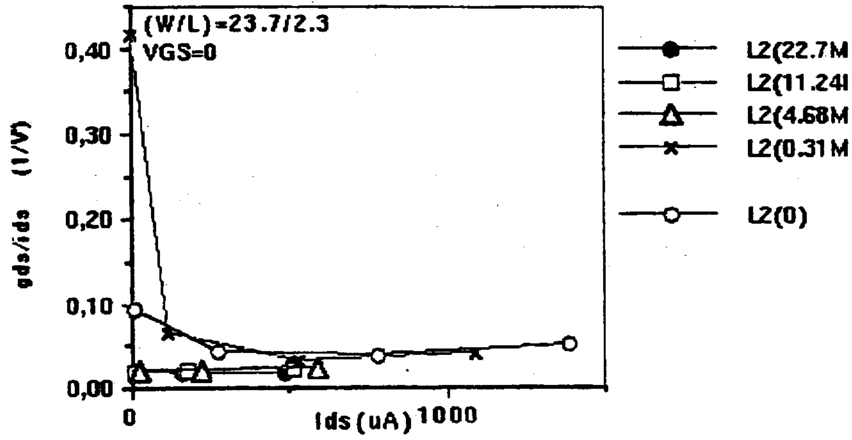


Figure 93: PMOS: g_{ds}/I_{ds} versus I_{ds} at V_{ds}=-2.25 V. As indicated in the legend the four curves correspond to doses of 310 Krad, 4.68 Mrad, 11.24 Mrad, 22.7 Mrad(Si) along with the initial curve.

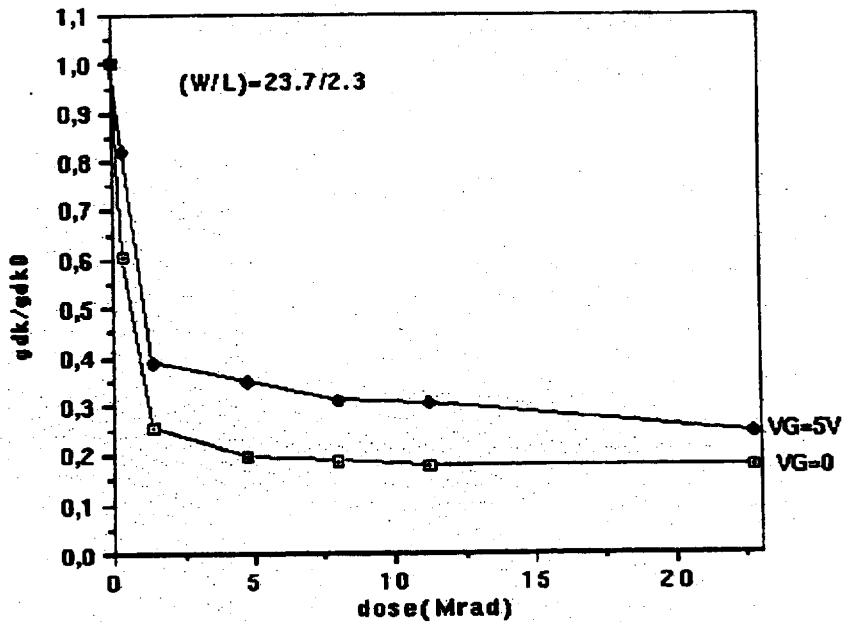


Figure 94: Normalised kink conductance of an NMOS versus dose.

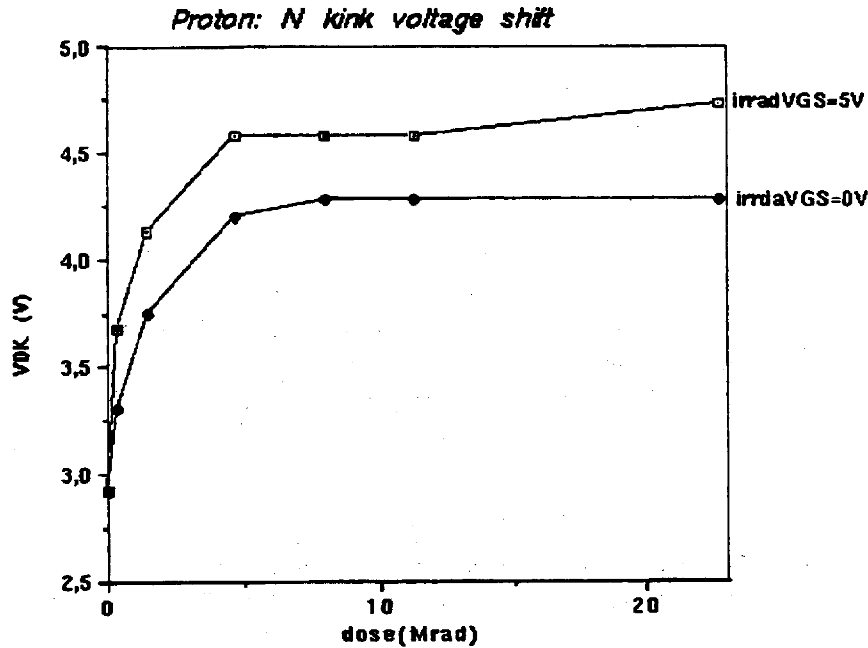


Figure 95: Kink voltage versus dose

7. Effects of radiation on a sample analogue circuit

   A simple OTA (Output Transconductance Amplifier) circuit has been included in the test circuit. The main measured characteristics are shown in table 16. At all doses an increase of the DC gain is observed. This is consistent with the behaviour of the transconductance and the output conductance of single devices. The decreased kink effect can be also held responsible of the improvement in DC gain. The 3 dB bandwidth increased slightly for the circuit irradiated at 300 Krad(Si) and decreased by about 15 % for circuits irradiated at 10 Mrad and 23 Mrad.

Table 16: Radiation effects on a simple amplifier.

Circuit	A0 (DC gain)	f(3db) at 0 rad	Dose (Mrad)	A0 @ dose	f(3db) @ dose	DA0/A0	Df(3db)/f(3db)
1	520	2.4 MHz	0.31	940	2.6 MHz	80.7 %	8.3 %
2	500	2.8 MHz	10	1160	2.4 MHz	132 %	-14.8 %
3	560	2.6 MHz	23	1115	2.2 MHz	99 %	-15.4 %

   The noise of this OTA has been measured. For both circuit 1 (10 Mrad) and circuit 2 (23 Mrad), the noise power spectral density (PSD) at frequencies higher than 60 KHz is not altered by the irradiation, while the low frequency PSD increases considerably. For circuit 1 the noise PSD increased by about 37 % at 10 KHz. A much higher increase (150 %) is observed for circuit 2 at the same frequency. The highest frequency considered is 100 KHz. Detailed noise analysis of elementary devices is underway.

8. Effect on digital circuit speed

The degradation of the speed of digital circuits has been estimated from the frequency of oscillation of a 35 stage ring oscillator. Table 17 depicts the results for 3 different circuits irradiated at different doses. The basic cell being a simple inverter, one can infer the average gate delay from the frequency of oscillation [61]. The oscillator frequency depends directly on the threshold voltages of the N and P devices. For circuit 1, irradiated at 300 Krad, the frequency increased very slightly because VT shifts are not so important, and the enhencement could be achieved through the increase of the transconductance of the NMOS device. For circuit 2 and 3 The shift in the PMOS threshold voltage is so significant that it results in a decrease in the frequency of oscillation. The positive side-effect is that a proportional decrease in supply current is to be expected. After 23 Mrad(Si), an increase in gate delay of about 23 % is to be expected.

Table 17:

Circuit	frequency1 at 0 rad	Dose	f at dose	$\delta D_f/f$
1	11.13 MHz	0.31 Mrad	11.2 MHz	+0.6 %
2	12.4 MHz	10 Mrad	9.8 MHz	-21 %
3	11.13 MHz	23 Mrad	8.6 MHz	-22.7 %

9. Neutron irradiation

Similar circuits to those mentioned above, have been irradiated with neutrons (6 10^{14} n/cm^2, 1 MeV equivalent). Only minor effects have been observed. These effects are found to be equivalent to effects produced by about 500 Krad of ionising radiation: consistent with the expected level of parasitic ionising particles in the neutron beam.

10. Present work

We are still evaluating the radiation hardness of SOI3HD. A recently irradiated chip (from a different batch) will be measured in the near future. The circuit contains test devices and structures, charge amplifiers and pixel prototype circuits. Charge amplifiers from this batch, have been already used to test radiation hardness of pixel particle detectors. No abnormal behaviour has been observed in the operation of the electronics (from a qualitative macroscopic observation) up to about 6 Mrad(Si).

11. Conclusion

The presented results indicate that the SOI3HD process is a potential candidate for systems exposed to high levels of radiation. Nevertheless, further characterisation work is to be continued. Knowledge of device and circuit behaviour when exposed to radiation is a must. It can help in coping with some radiation-induced problems at the design levels (schematic and/or layout associated with a biasing strategy). For analogue circuits, careful attention is to be given to the biasing of the different devices. One has to be sure that the devices do not quit the desired operating region, because of the VT shifts. NMOS devices with central body ties should always operate in the kink free region ($V_{DS} \leq 2.5$ V). Although the irradiation would not worsen this situation. For digital circuits, one has to foresee the speed degradation due to irradiation. In

performing worst case simulations, the designer has to tune the circuit parameters so that it meets the expected performance at the end of the expected lifetime.

3.6 Front end electronics

3.6.1 Front-End circuits in SOI3HD

In this report, we only very briefly describe the ongoing work in SOI3HD.

For the 1993 SOI3HD run, we designed prototype pixel front-end circuits, along with test structures necessary to investigate the possibilities and radiation hardness of this technology. A specially designed small pixel array is being used to investigate properties of silicon pixel detectors. Some results can be found in [62]. More results concerning this chip will be provided in a more complete report in the near future.

Presently we are preparing more complete pixel systems for implementation (analogue front-end + digital readout) in the 1994 run. For the analogue, we are testing several circuit architectures and ideas, satisfying different compromises. Here we present the architecture whose design has been completed at the time of the writing. All simulation results presented here are from the ELDO simulator. These are post-layout simulations using a special transistor model provided by the manufacturer (THOMSON TCS). The input signal is simulated by a current pulse with 1 ns rise and fall time and 10 ns duration. The input capacitance is assumed to be 250 fF. The leakage current is indicated in the simulation charts.

The general diagram is shown in figure 96. The two stage architecture will help in tuning the system for the best signal over noise ratio. It also renders the subsequent stage insensitive to the DC level shift due leakage current. This configuration minimises inter-pixel coupling. A single stage system will require a relatively high gain from the first stage. Because of the (necessarily) limited bandwidth, the input impedance would be such that high voltage swings could be present at the input node. This would induce charges in the neighbouring pixels. For the pre-amplifier, four versions are implemented (P and N common source and P and N cascode configurations).

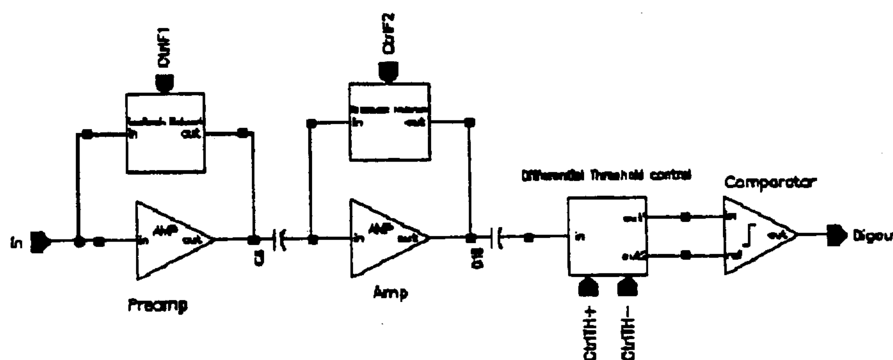


Figure 96: The block diagram of the analogue front-end cell.

The feedback network is tunable, and is such that high leakage currents are tolerated. The maximum acceptable leakage current is function of the control signal "CtrlF1" and is

nominally set to 100 nA though it could reach the microamp range. (See simulation results in figures 97 and 98.)

The final block is threshold-controllable discriminator. It is composed of a low gain differential amplifier followed by a differential to single ended amplifier. The threshold is set externally by a differential signal. This technique will considerably reduce the threshold sensitivity to noise and to process parameter variation. Figures 99 and 100 show the analogue and digital responses to signals form 1000 e^- to 20000 e^-.

Extremely high input charges can cause the circuit to misbehave. Simulation results for input charges of 2000,3000 and 100000 electrons are shown in figure 101 and 102.

Expected performances:

- Dimensions (including the bonding pad): 50 μm $\times$ 300 μm
- Rise time of the input preamplifier (10-90 %): 20 ns
- Total power consumption: 65 μW
- Threshold control: 500-100000 e^-
- Maximum tolerable leakage current: 100 nA
- Expected rms noise (not simulated): 200 e^-

The noise is estimated from measurements of an amplifier implemented in a previous circuit. More detailed analysis and comparisons will made in the future.

3.6.2 Front-End circuits in DMILL technology

1. Introduction

   As described in the RD29 R&D proposal [54], DMILL is supported by a consortium gathering three divisions of the CEA (French atomic energy agency): DSM-Saclay (Matter science Directorate), LETI-DTA (Advanced Technology Directorate) and Centre d'Etudes de Bruyères-le-châtel; the IN2P3 (National Institute for Nuclear Physics and Particle Physics) and THOMSON-TCS. These partners have merged their experience and competences to develop and industrialise DMILL technology, a new rad-hard analogue-digital technology specially dedicated to "high energy physics electronics". This development is based on a first study started in 1989 by LETI and Centre d'Etudes de Bruyères-le-châtel.

   In its present version, DMILL technology monolithically integrates analogue-digital CMOS, PJFET and NPN bipolar transistors (see Fig. 103). With the flexibility of design offered by the complementary properties of these three families of devices, this technology is foreseen to fulfill the very hard constraints of LHC readout electronics: MOS and bipolar transistors allow designs of analogue and digital rad-hard fast circuits, and JFET transistors, which are intrinsically rad-hard and low noise devices, permit designs of low noise very rad-hard circuits for room and cryogenic temperature operation. Refs. [63, 64] outline the history of DMILL.