PART A

ATLAS Internal Note
INDET-NO-086 (1994)

15 December 1994

Pixel detector back-up Document to support the ATLAS Technical Proposal

P. Fischer, B. Raith, N. Wermes
University of Bonn, Germany

A. Lankford, S. Pier and B. Schmid
University of California, Irvine, USA

M. Campbell, P. Jarron, E. H. M. Heijne, P.[1] Middelkamp, W. Snoeys
CERN, Geneva, Switzerland

C.Arrighi, L. Blanquart, V. Bonzom, J-C. Clemens, M. Cohen-Solal, P. Delpierre, A. Fallou, E. [2]Grigoriev, M.C. Habrard, G. Hallewell, D. Labat, L. Lopez, A. Mekkaoui, T. Mouthuy, R. Potheau, M. Raymond, A. Rozanov, D. Sauvage, L. Vacavant.
CPPM, Centre de Physique des Particules de Marseille,France

D. Bintinger, A. Ciocio, K. Einsweiler, M. Gilchriese, O. Milgrome, J. Millaud, D. Nygren, M. Shapiro, J. Siegrist, H. Spieler, M. Wright
Lawrence Berkeley Laboratory, California, USA

G. Capannesi, M. Colucci, P.G. Pelfer, S. Sottini
INFN and Physics Department of Firenze University, Italy

D. Barberis, M. Bozzo, C. Caso, M. Dameri, G. Darbo, P. Morettini, P. Musico, B. Osculati, L. Rossi, G. Sette
INFN and Physics Department of Genova University, Italy

R. Bates, S. D'Auria, S. Gowdy, V. O'Shea, C. Raine, K.M. Smith
Glasgow University, UK

G. Bellini, M. di Corato, A. D'Avella, P. Inzani,D. Menasce, L. Moroni, D. Pedrini, L. Perasso, F. Ragusa, S. Sala, F. Tartarelli
INFN and Physics Department of Milano University, Italy

G. Cesura, D. Hauff, H. Hoernl, J. Kemmer, P. Lechner, G. Lutz, R. H. Richter, H. Seitz
MPI Halbleiterlabor, Munich, Germany

Y. Gao, J. Harton, R. Jared, M. Walsh, S. Wu
University of Wisconsin, Winsonsin, USA

K. H. Becks, K. W. Glitza, J. Heuser, S. Kersten
University of Wuppertal, Germany

[1]Also at University of Wuppertal
[2]On leave of absence from ITEP, Moscow, Russia

Contents

1 Introduction and Layout

1.1 Introduction

This document is intended to provide additional information about the pixel detector system for the ATLAS detector, beyond that contained in the ATLAS Technical Proposal. Additional information, relevant to the pixel system, on silicon detector properties, radiation damage and tracking performance may be found in the Semiconductor Tracker(SCT) backup document [5].

Silicon pixel detectors with high spatial and temporal resolution and high granularity are an excellent match to the challenge of charged particle tracking for LHC detectors. Arrays of pixels formed into barrel layers and disks will provide simultaneous two dimensional track measurements at each layer or disk. Pixel sizes of approximately 50 microns in azimuth and 300 microns parallel to the beam or in radial extent for barrel layers and disks respectively, will provide spatial resolutions of approximately 15 microns in the narrow dimension and 80 microns in the wide dimension, if digital read-out is used. The use of analog read-out can further improve these numbers as shown in section 1.5. Systems envisioned for the ATLAS [1] detector have on the order of 10^8 pixels necessitating a scheme for reading out only those pixels struck on beam crossings of interest.

At the LHC, Beam Cross Overs (BCOs) will occur every 25 ns. At the mean design luminosity of 10^{34} $cm^{-2}s^{-1}$, around 20 pile-up events per BCO will occur in the ATLAS [1] and CMS [2] general purpose collider experiments, from which events of interest must be disentangled. Moreover, in some of these events, one or more tracks must be identified within tightly collimated jets of particles.[3]

Information from the hit detector elements in events from BCOs with a level 1 trigger (10^{-3} - 10^{-4} of the total rate) must be read out in less than the mean time between triggers. During the level 1 latency of ≈ 2 μs, 80 BCOs will occur, and a front end selection of data from up to 1600 overlaid events (each with a multiplicity between 20 and 40 tracks) will be necessary. Additional background from photon conversions and loopers should also be taken into account.

Figure 1 shows a general view of pixel tracking and vertex detector proposed for the ATLAS inner detector. The layout of the pixel system is determined by a number of criteria and constraints including momentum resolution, pattern recognition, and radiation damage. A minimum of two pixel points, along with four points from a combination of the silicon strip, GaAs and MSGC detectors are needed to provide six "precision" points for momentum resolution in the region $\mid \eta \mid < 2.5$. The number of precision points needed for pattern recognition is believed to be at least six and more may be needed. The configuration for full luminosity operation contains ≈ 2.2 m^2 (active area) of silicon pixel vertex detectors arranged in two cylindrical layers and four pairs of disks in the forward direction. The pixel detectors provide critical tracking information for pattern recognition, for vertex measurements and for the measurement of track polar angles. The pixel system has very low occupancy, about

[3] As an example, the mean 1 σ (multiplicity / width) of 7 tracks / 12 mrad in high p_T jets [3] would represent a track density of ≈ 4.5 mm^{-2} at 11.5 cm from the LHC beams. The mean occupancies in crossed microstrip detectors with 50 μm pitch in ϕ and 200 μm in z are 25 % and 100 %, giving a high probability of lost data, and a serious ambiguity problem. In an array of (50 μm $\otimes$ 300 μm) pixels however, the local occupancy would be only 7.5 %.

10^{-4} per pixel, and this can provide nearly unambiguous space points even for tracks within jet-like events. Polar measurements within ATLAS are provided solely, with good precision, by the precision tracking elements. The Z and r measurements from the pixels are critical to obtain good angular resolution. Primary and secondary vertices can be found with the pixel system. Finally, the inherent two-dimensional points from the pixels, with low occupancy are well matched to the need for level 2 triggering in association with calorimeter or muon towers.

A third cylindrical vertexing layer is planned to be installed during the initial low luminosity operation of LHC primarily to enhance B-physics capabilities.. However, such a layer, located at a slightly larger radius to yield a greater longevity, could also be of considerable use in pattern recognition and triggering at higher luminosity. Additional studies of the benefits of a three-layer pixel system for high luminosity operation are being done.

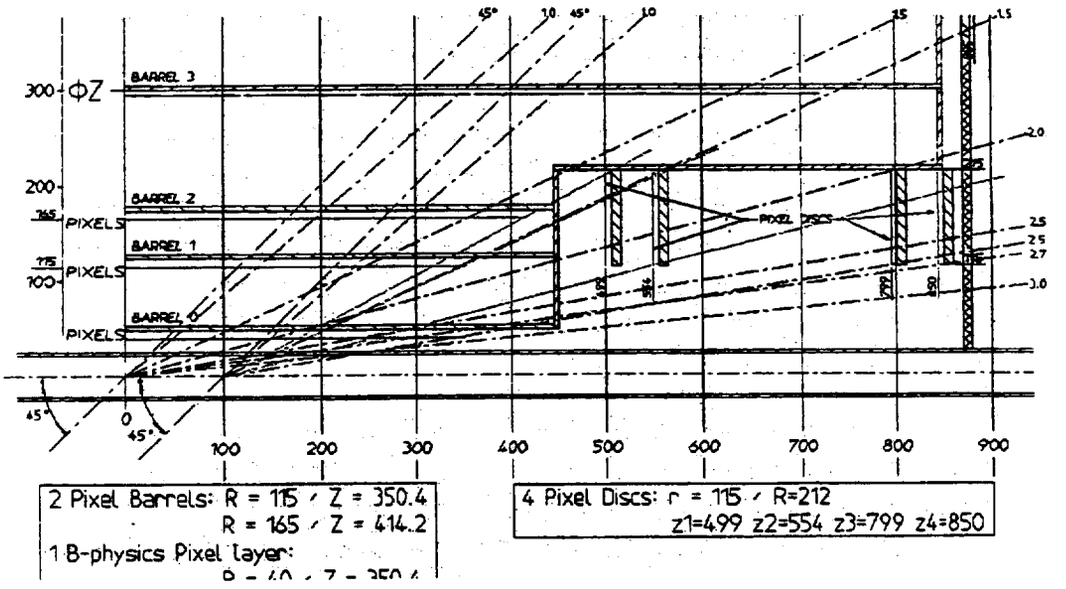

Figure 1: Layout of the pixel tracking and vertex detector proposed for ATLAS.

The inner radius of the barrel and disk layers is determined, to a large extent, by the expected and desired lifetime of the pixel detectors and electronics. The best tracking performance is obtained for the minimum possible radius, but radiation damage to the silicon detectors limits the inner radius to be more than about 10 cm, for about a ten year lifetime at the nominal integrated luminosity.[4] Although it is very likely that the pixel system would be upgraded well before ten years elapse at the LHC, it is understood that designing to a nominal ten year lifetime will provide additional operating margin during the actual lifespan of the system. The B-physics layer at about 5 cm will not survive more than about four years (three years at 10^{33} and one year at 10^{34}) unless it is moved to a larger radius or unless a detection medium other than silicon can be found that will endure greater

[4]for instance the inner pixel permanent layer, located at 11.5 cm radius, is expected [4] to receive radiation damage equivalent to a dose of about 2.5 Mrad (or 8.3 10^{13} 1 MeV neutrons cm^{-2}) per LHC "year" (of 10^7 seconds operation) at the nominal luminosity of 10^{34} $cm^{-2}s^{-1}$.

doses and unless electronics can be made rad-hard to more than 20–30 MRads. Although some candidates exist for new rad-hard detection media (eg. diamond and GaAs), and it may be possible to operate electronics up to the 100 MRad level, we assume in this note that the B-physics layer will be removed or replaced.

The key element of the pixel system is the electronics readout, the $\approx 2m^2$ of integrated circuits, that are bump bonded to the detector elements and which should read-out $\approx 10^8$ channels at a frequency of 40 MHz. At present, several options for the readout architecture are under investigation. But all are based on a column scheme that minimizes signals sent to the periphery of the readout chip. The readout electronics must be built in a radiation hard technology: several promising candidate technologies are discussed in this report.

1.2 The pixel detector layout

The nominal pixel layout for ATLAS is shown in Fig. 2,while details of the geometry are presented in table 1. There are about 1×10^8 and 0.5×10^8 pixels in the barrel and disk regions, respectively. In the barrel region, the radial dimension corresponds to the mean radius of the active detector element, and the half-length represents the distance from the nominal interaction point to the edge of the active region. In the disk region, z is the average for adjacent detector elements staggered in z to give overlap in ϕ. The disk radial dimensions correspond to circles defining the inner and outer edges of the active region. Different readout chip sizes and mechanical designs will yield a layout that differs slightly from that presented here. The layout presented here is presently used in the ATLAS tracking simulator program. Alternatives, and more details, are given in Chapter 3.

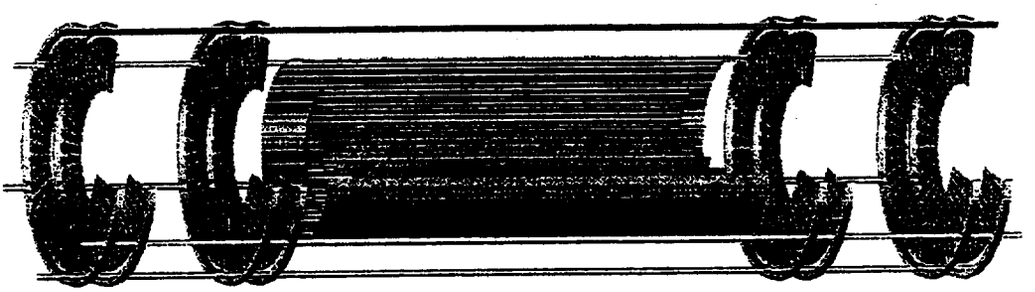

Figure 2: A perspective view of the Atlas pixel system

The inner radius of the pixel detector system is determined by radiation damage, which is discussed in more detail in section 3. The capability to find secondary vertices would be enhanced if the inner radius of the pixel system were reduced, which is the rationale for the B physics layer.

The outer radius of the barrel layer is determined by the desire to extrapolate accurately in dip angle from the pixel system to the silicon strip system. For example, a 5 cm separation between barrel layers yields about a 2.5 mrad angular accuracy, which implies about a

400 micron error in z in the extrapolation to the first layer of the silicon strip tracker or about 675 micron for the second layer. This is comparable to the z resolution of the silicon strip system, which is 600–750 microns, depending on the final spatial resolution chosen for this system. The dip angular accuracy may be useful in the trigger, to calculate invariant masses quickly using the unambiguous ϕ-z (or r) correlations in the pixels. This capability may also be useful in pattern recognition. Track candidates found first in r-ϕ can be associated easily in z using the pixel information.

The length of the pixel barrel sections is determined by the desired rapidity coverage, including the beam size spread in z. Additional studies are required to optimize the barrel coverage and to minimize the material in the system. The location of the forward disks is primarily determined by the requirement to have two pixel points for $\mid \eta \mid < 2.5$.

Figures 3 and 4 show examples of the pixel tile geometries planned for the cylindrical and disk layers respectively. The detector tile structure contains a thin (150 μm) silicon substrate with implanted pixel detector diodes, onto each of which a number of ($\approx$ 1 cm^2) electronic readout chips (thinned to $\approx$ 80 - 150 μm) are bump-bonded using the "flip-chip" technique. Thin detector substrates should offer good radiation hardness and minimal material. A total of about 1 % X0 is expected per layer for normal incidence, including detectors and readout, support, cooling and cabling.

The nominal pixel size for all the layers in the barrel region is 50 μm (ϕ) $\otimes$ 300 μm (z), although other pixel sizes are under consideration. The nominal pixel size in the disk region is also 50 μm (ϕ) and 300 μm (r). The small pixel element size proposed should allow unambiguous space point determination in a high multiplicity environment for tracking, vertexing and pattern recognition. The very low capacitance and leakage current of the elements allow operation at very low noise levels ($\leq$ 200 e$^-$ rms). The intrinsically high signal to noise ratio allows the detectors to be thinner than the usual 300 μm for silicon microstrips, allowing depletion at a lower bias voltage and correspondingly higher radiation resistance, while tracks crossing at large angles will also leave smaller clusters.

Table 1: Nominal Pixel Element Sizes and Positions.

Barrel Region	Nominal Radius (cm)	Active Half length(cm)	Number of Ladders
B-physics layer	4.0	35.04	16
First layer	11.50	35.04	48
Second layer	16.50	41.42	64
Disk Region	Nominal Z (cm)	Active Inner Radius (cm)	Active Outer Radius(cm)
	49.92	11.45	21.25
	55.40	11.45	21.25
	79.90	11.45	21.25
	85.00	11.45	21.25

The ultimate readout resolution is not yet decided, but a realistic goal for the ϕ resolution is 18 μm, including systematics. Pixels of 50 μm (ϕ) $\otimes$ 300 μm (z or r) will give intrinsic ($\sigma = \frac{s}{\sqrt{12}}$) resolutions 14 μm (ϕ) and 87 μm (z or r). The latter can be further improved with

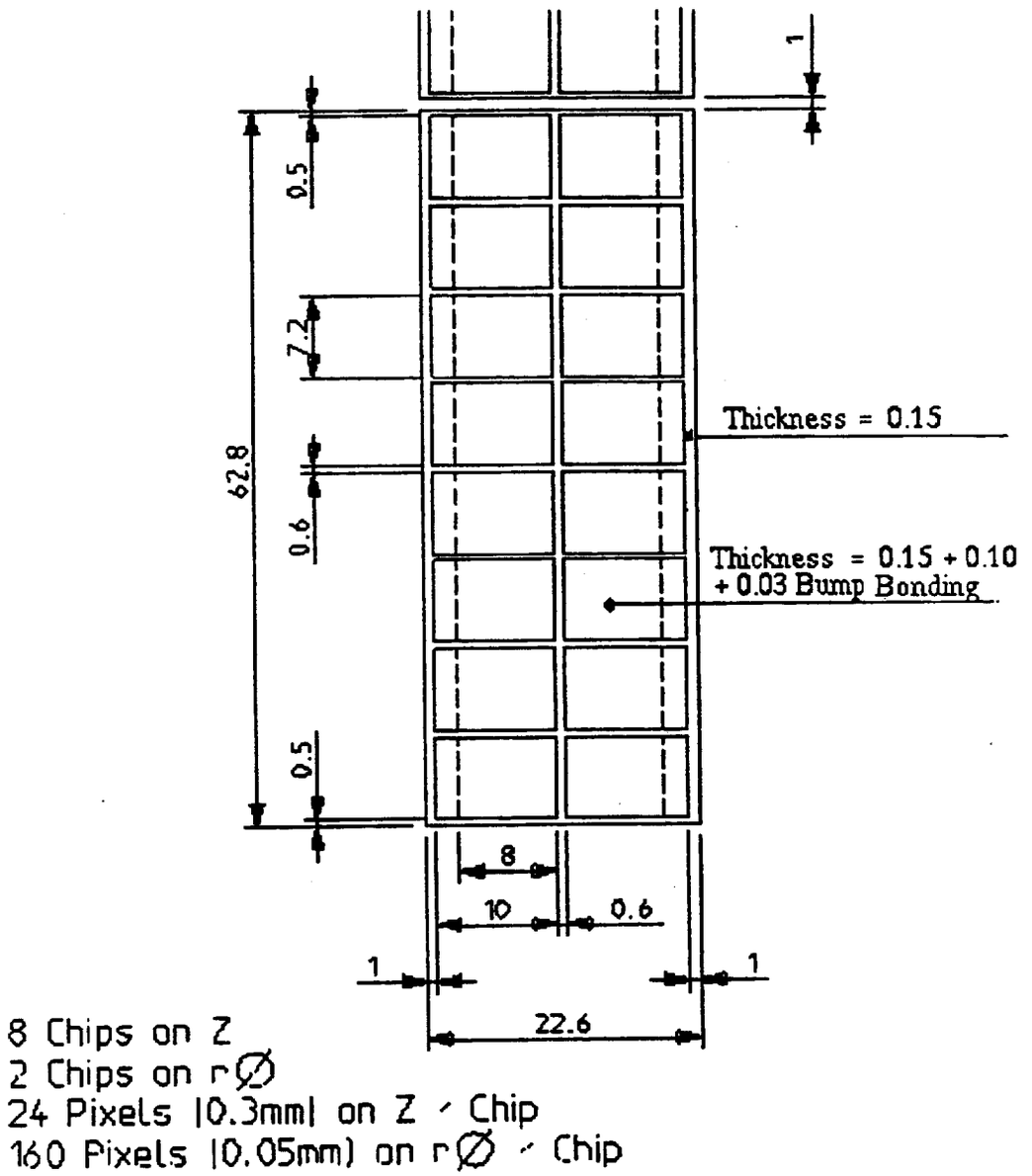

Figure 3: The tile geometry for the cylindrical layers of the ATLAS pixel detector.

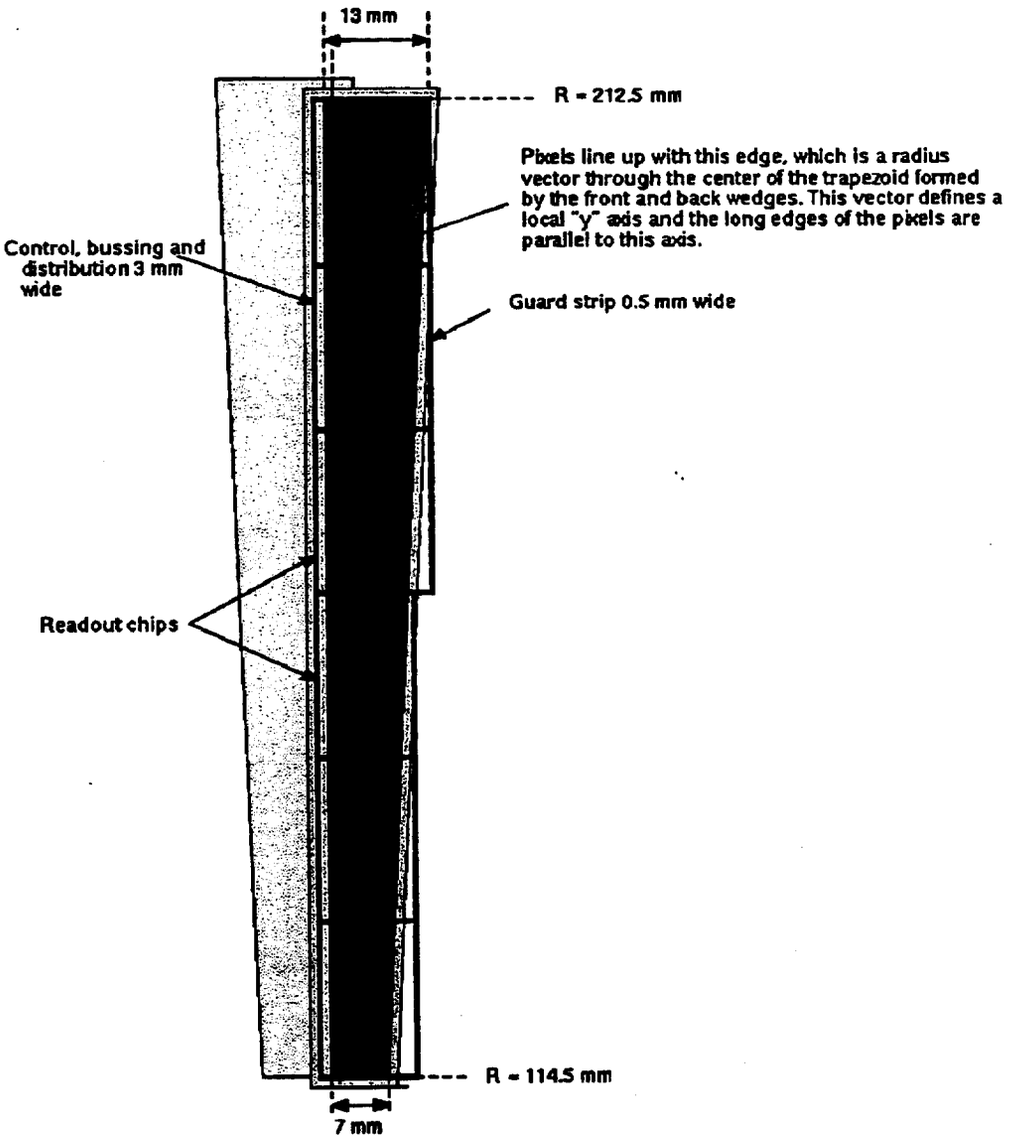

Figure 4: The tile geometry for the disk layers of the ATLAS pixel detector.

a "brick" geometry having adjacent axial rows of pixels offset by half a pixel length in z or r. Further improvement is also possible with a readout architecture incorporating analogue charge interpolation, which is included in one of readout architectures under study.

1.3 Barrel Modules

For the purposes of the simulation only, we use the following dimensions and properties for a barrel module, shown in Fig. 3:

- thickness of detector substrate: 150 μm;
- thickness of bonded electronics: 80 - 150 μm;
- total length (Z): 6.28 cm;
- total width (R-ϕ): 2.16 cm;
- active length (Z): 6.18 cm;
- active width (R-ϕ): 1.66 cm.

Each ladder is an array of modules laid end to end. For easier mounting and modularity, there is no z overlap between modules in a ladder. A gap in z of 1 mm is left between adjacent modules. Allowing an inactive interval of 0.5 mm at the end of each module (taken up by the guard ring structure, and some reserve for detector dicing), the total dead area in z between adjacent modules is 2 mm.

Detector layers are made up of axial ladders arranged in a "barrel stave" assembly. The number of ladders around the circumference of each layer are shown in table 1. With this modularity, the angles between the planes defining the polygon of detector ladders and the layer circumferences are 11.5°, 10.0° and 9.7° for the B physics layer and the layers at 11.5 cm and 16.5 cm respectively, with corresponding angular overlaps in ϕ of 0.52°, 0.13° and 0.14°. The intended minimum active area overlaps in ϕ are about 0.3 mm, or 6 pixel rows.

1.4 Disk Modules

Each disk is a polygon of overlapping pixel disk modules (wedges). The wedge modules overlap and alternate front and back with cooling and support in between them. Other services are located on the outboard edges of the wedges. There are 144 overlapping wedges in one disk; 72 on the front and 72 on the back. The spacing in z between the two overlapping planes of wedges (active silicon to active silicon) is taken to be 0.4 cm. A drawing of a typical module (front and back wedge) is given in fig 4. The pixels within a wedge are arrayed as shown in fig 4. A front and back wedge pair forms one of the 52 trapezoids that form a disk. There is approximately a three pixel overlap at the center of the trapezoid formed by a front and back wedge and also at the edges with an adjacent trapezoid. The long dimension of a pixel is parallel to a radius at the center of a trapezoid but not at its edges since the pixels are arrayed in a rectangular pattern.

1.5 Space Resolution

Since several pixel electronic readout schemes (analog and digital) are still under investigation for the high luminosity LHC application, the ultimate readout resolution is not yet decided, and may be different, for example, in the B physics vertexing layer to the other layers. Table 2 shows the intrinsic resolution achievable with "binary" ($s/\sqrt{12}$) and analog readout. For layers equipped with binary readout, a conservative goal for the ϕ resolution is $\pm$ 18 μm, including alignment and positioning systematics. In the orthogonal direction (z for cylinders, r for disks), a conservative value for the resolution is $(300\mu m/\sqrt{12}) = \pm$ 87 μm.

With analog readout, an intrinsic ϕ resolution of better than $\pm$ 7 μm is achievable [6], [7], which when combined with the alignment and positioning precision of $\pm$ 7 μm, will give an overall spatial resolution in ϕ of $\pm$ 10 μm. The resolution in z,r will depend on the track incidence, and the crossing point along the 300 μm pixel dimension. Previous pixel resolution studies [6], [7] have shown that the end regions along the pixel long dimension have enhanced resolution - through charge sharing - relative to the central regions, whose resolution is "binary". Figure 5 illustrates the regions of high and low z,r resolution. We assume that the end 25 μm of one pixel shares charge with the end 25 μm of the next to give an enhanced resolution of 10 μm over an effective area 50 μm x 50μm. Binary resolution is assumed in the remaining 250 μm x 50 μm central zone. By weighting the relative areas of the zones of high and low resolution in z,r, we find a weighted z,r resolution of 62 μm for the case of analog readout.

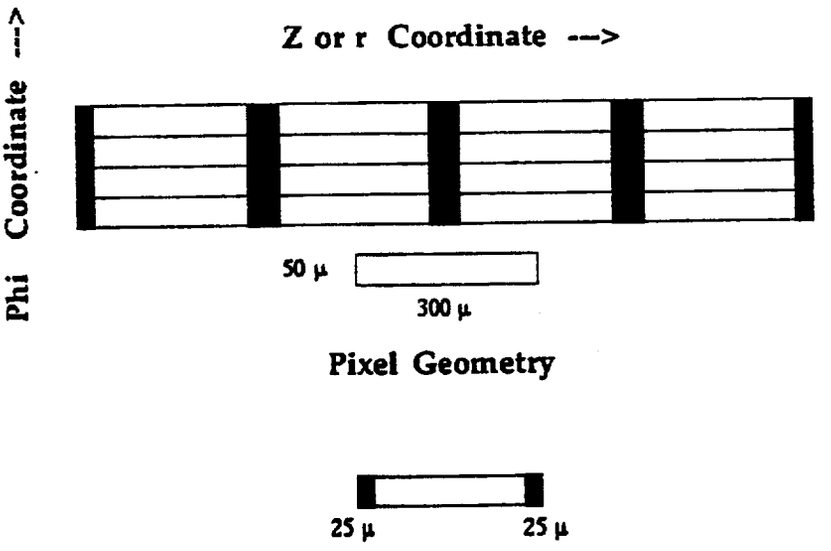

Figure 5: Enhanced resolution in z,r through charge sharing between ends of adjacent pixels

A pixel tiling scheme ["bricking": Figure 6], with adjacent ϕ columns of pixels shifted in z by half a pixel length (150 μm) will exploit lateral (ϕ) charge sharing (perhaps aided by E

x B effects) to further improve the z resolution. An estimate of the z,r resolution is 43 μm, which assuming there is always charge sharing in ϕ, but ignoring any z,r charge sharing. This value is equal to twice the binary z,r precision for the unbricked case. Taking full account of z,r charge sharing with bricking, a second effective 50 μm zone with 10 μm resolution is combined with two 100 μm x 50 μm zones with binary resolution. By weighting the relative areas of the zones of high and low resolution in z,r, we find a weighted z,r resolution of 23 μm [table 2], which probably represents the best z,r resolution achievable.

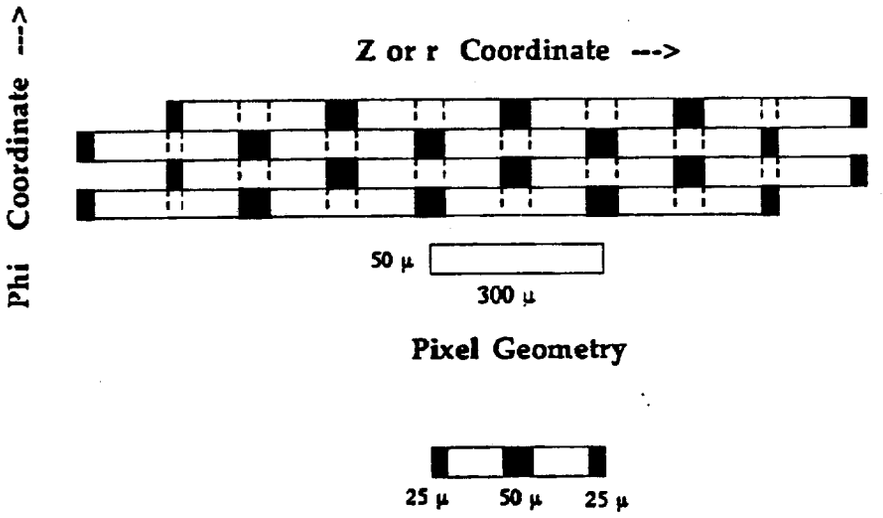

Figure 6: Pixel bricking scheme : alternate ϕ pixel rows are shifted half a pitch in z

Since detailed studies of resolution, including the case of a "bricked" array of pixels in the ATLAS geometry have yet to be made in test beams, we have proposed for the purposes of simulation [8]for the technical proposal pixel intrinsic resolutions of 15 μm (ϕ) and 87 μm (z,r) for the case of binary readout, and 7 μm (ϕ) and 43 μm (z,r), in the case of analog readout with bricking, as indicated in table 2 [5]

Table 2: Intrinsic Resolution of Pixels with Binary and Analog Readout.

	Binary	Analog	Analog + Bricking
$\sigma(\phi)$	$\leq$15μm	7 μm	7 μm
σ(z,r)	$\leq$87 μm	62 μm	43 - 23 μm

[5]Charge sharing can also be exploited in digital read-out schemes. The low threshold (in mips) which can be applied on each pixel will maximise the frequency of pixel clusters and therefore [32] improve the space resolution. We intend to continue tests also along this line, to establish how far beyond the "pitch/$\sqrt{12}$" rule the digital read-out can go.

1.6 B-Physics Possibilities with the ATLAS Pixel Detector

An important programme of B physics is intended for LHC. Three large, specialised B physics detectors have been proposed [9, 10, 11], incorporating sophisticated vertex detectors which include pixels. An important contribution from ATLAS and CMS - including the measurement of CP violation parameters in several exclusive B decay channels, with an accumulated luminosity of a few 10^{40} cm^{-2} is expected during initial low luminosity operation. High resolution, low mass B-physics vertexing layers (removable for later full luminosity operation) are under study for placement within a few cm of the beams.

The achievable impact parameter resolution (in μm) is usually expressed in the form

$$\sigma_{IP} = A \oplus \frac{B}{p_T \sqrt{\sin\theta}} \tag{1}$$

The asymptotic term A depends on the spatial resolution of the innermost detector layer and its distance from the vertex. The scattering term B depends on the layer position and on its multiple scattering contribution (% X/X0), while θ is the angle with respect to the beam line.

Two vertexing layer geometries for B physics have been proposed for ATLAS. The first has a surface of 300 μm thick silicon microstrips at a radius of 6 cm having overall resolution of 10 μm in ϕ and 20 μm in z, with 90° crossing angle [16]. A radiation length of $\leq$ 0.6% X/X0 is proposed by displacing readout and cooling from the sensitive area through the use of long (26 cm) ϕ strips, although this limits the layer coverage to $\eta = \pm$ 2.2 (or $\pm$ 1.7 allowing for a 2 σ variation in the z position of the LHC interaction point), and reduces the strip signal to noise margin. This configuration has a calculated impact parameter resolution of (13 $\oplus$ 62 / P_T $\sqrt{sin\theta}$) [12], and a vertex resolution in z of (39 $\oplus$ 90 / P_T $\sqrt{sin\theta^3}$). The expected lifetime of the layer corresponds to a integated luminosity of 6 10^4 pb^{-1}; principally limited by the rise in depleton voltage due to doping changes under irradiation [13].

The second geometry has an extra layer of pixels to provide unambiguous space points on the measurement surface closest to the secondary vertex. This uses the same pixel geometry as in the layers at R = 11.5 and 16.5 cm (150 μm detector substrate, overall radiation length of 1% X/X0). A detector with a length of 700 mm (see figure 2)for acceptance to $\eta = \pm$ 2.8 ($\pm$ 2.5 with 2 σ beam spot z variation) is under consideration. With "binary" readout, the expected overall resolutions of 18 μm in ϕ (50μm/$\sqrt{12}\oplus$ 10 μm syst.) and 87mm in z (300μm/$\sqrt{12}$) would give a calculated impact parameter resolution of (18 $\oplus$ 61 / P_T $\sqrt{sin\theta}$) [12], and a vertex resolution in z of (84 $\oplus$ 130 / P_T $\sqrt{sin\theta^3}$). With analog readout, giving expected overall resolutions of 10 μm in ϕ (7μm intr. $\oplus$ 7 μm syst.) and a conservative 40 μm in z (around 150μm/$\sqrt{12}$), an impact parameter resolution of (12 $\oplus$ 52 / P_T $\sqrt{sin\theta}$) and z vertex resolution of (52 $\oplus$ 79 / P_T $\sqrt{sin\theta^3}$) have been calculated [12]. In the high luminosity configuration (without a vertexing layer), the corresponding impact parameter and z vertex resolutions are (27 $\oplus$ 220 / P_T $\sqrt{sin\theta}$) and (130 $\oplus$ 240 / P_T $\sqrt{sin\theta^3}$) [12].

Fig. 7 (a) shows the dependence of the A term in the impact parameter resolution upon the position of a pixel layer with overall ϕ resolutions of 10 μm, 15 μm and 18 μm. Fig. 7 (b) shows the dependence of the B term upon the position of a pixel layer with multiple scattering contributions of 1%, 1.2% and 1.5% X/X0 (P_T = 1 GeV tracks at normal incidence). With no length restriction - other than that imposed by cost - greater pseudorapidity acceptance

for B physics [17] becomes available with a pixel layer, allowing for example, the more rapid accumulation of statistics for a higher sensitivity to the B_s mixing parameter x_s. A detector with a length of 700 mm (see figure 2)for acceptance to $\eta = \pm$ 2.8 ($\pm$ 2.5 with 2 σ beam spot z variation) is under study.

Detailed studies of the B-physics performance of different ATLAS vertexing configurations in ATLAS are required. One example of particular interest is the decay time resolution, using three dimensional measurement of the vertex in the decay $B_s^0 \rightarrow D_s^- \pi^+$, upon which x_s reach principally depends [14]. Preliminary estimates, based on studies of several vertexing options [14], suggest a resolution of $\leq$ 0.07 ps ($<$ 5%) should be achievable with a pixel vertexing layer having spatial resolution of around 10 μm in ϕ and 20-40 μm in z. An x_s reach up to about 40 appears achievable with an an event sample of around 16000 $B_s^0 \rightarrow D_s^- \pi^+$ events [14], corresponding to an integrated luminosity of 6 10^4 pb^{-1}. This integrated luminosity roughly corresponds to the lifetime limit for a silicon detector with 300 μm substrate placed at a radius of 6 cm [16], but should be well within the lifetime of a 150 μm substrate pixel vertex detector with a correspondingly much shallower rise in depletion voltage with radiation dose. Since standard model predictions for rare decays such as $B_s^0 \rightarrow \mu^- \mu^+$ can only be tested to a precision of about three standard deviations with this integrated luminosity, there is a clear advantage to a vertex detector able to withstand the highest possible radiation dose.

The precision of secondary vertex finding is also important in controlling combinatorial background [15] in the CP violation measurement channel $B_d^0 \rightarrow \pi^- \pi^+$. Preliminary estimates suggest that a transverse decay length resolution of around 50 μm in the P_T range 3-6 GeV/c is possible with the pixel vertex detector. A statistical precision of 0.043 in the measurement of $\sin 2\alpha$, via a time - dependent decay asymmetry analysis based on an integrated luminosity of 10^4 pb^{-1}, is expected [15], assuming a resolution of 57 μm in the radial positon of the secondary vertex. A measurement of $\sin 2\beta$ to a statistical precision of 0.018 (time dependent analysis) in the clean measurement channel $B_d^0 \rightarrow J/\psi K_s^0$, is considered possible with comparable statistics and J/ψ decay vertex resolution. Fuller details of the B physics possibilities using the ATLAS detector are given in ref. [14].

1.7 The barrel sector prototype

The focus provided by beam testing a "Barrel Sector Prototype" (BSP) will aid in all aspects of pixel detector implementation. After having installed silicon pixel tiles on ladders and disk segments and aligned these in a prototype mechanical support structure, the pixel detectors will be integrated into the wedge -shaped prototype, which will contain other central tracking elements The BSP is planned for construction in 1996 for beam testing in 1997, and will address many of the system performance, mechanical alignment and cooling issues. A prototype mechanical structure to support several ladders of pixel detector tiles at layer radii 4.0, 11.5 and 16.5 cm and partial disk at their nominal z positions is planned. Realistic readout electronics, incorporating sparsified readout of pixels sharing a time stamp in common with that of a simulated level 1 trigger will be implemented.

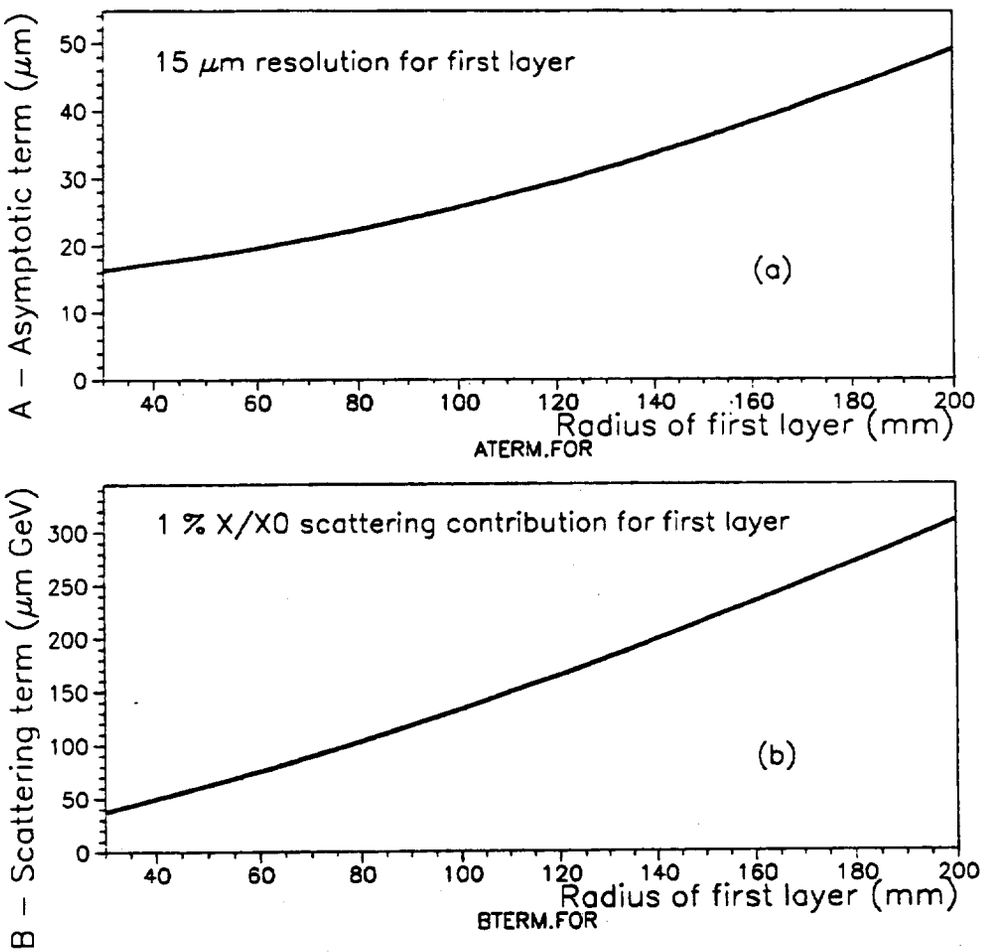

Figure 7: The effects on impact parameter measurement precision for B physics from
(a) precision of the first layer and its distance from interaction point
(b) multiple scattering in the first layer and its distance from interaction point
(parametrisations follow those of ref [16]).

2 Status of Pixel Development around the world

2.1 Review of RD19 and CERN-based developments

2.1.1 Introduction

In particle physics experiments, after 1-dimensional silicon microstrip detector arrays, a thousandfold increased segmentation with true 2-dimensional geometry could be envisaged without prohibitive cable volumes and excessive power dissipation [18],[19]. Along these lines, the pixel (or micropattern) detector has been designed as a new type of semiconductor device for particle tracking and pattern recognition. This detector should be able to cope in robust way with high multiplicity events at high rates, while allowing for a longer detector lifetime under irradiation and a thinner sensitive depletion region. At CERN the development was initiated in 1988 in the framework of the LAA detector R&D project [20].

In a collaborative effort between an increased number of particle physics groups and microelectronics industry we continued in 1991 in RD19 [21] the work on this true 2-dimensional semiconductor detector in view of high luminosity applications in LHC and the most recent status report has been presented in January 1994 [22]. In the meantime, insertion of prototype detectors in the WA97 heavy ion experiment and in the DELPHI Very Forward Tracker provide encouragement and practical experience with these complex devices.
The objectives of the detector and electronics development in RD19 are:

- design and implementation of redout chips for pixel matrices with cell dimension between 30 μm and 500 μm and 1000 to 4000 cells in the matrix on a single chip; emphasis is placed on binary signal processing but also analog readout is pursued;

- readout architecture design which should allow the transmission off-chip of the coordinates of the particle hits only; due to the true 2-dimensional nature of the detector, no further processing is required, and track finding and reconstruction can proceed immediately; the characteristics of the architecture should ultimately correspond to the requirements in a high luminosity p-p experiment at the LHC, close to the beam pipe;

- hybrid assembly of the readout chips with the detector matrices using "flip-chip" technology, e.g. solder or indium bump bonding; the monolithic combination of sensor and readout functions is being studied as a more sophisticated alternative to the hybrid implementation;

- introduction of Multi-Chip-Modules (MCM) which should allow the building of arrays with appropriate size for LHC experiment ($\approx$2 m^2); a stepwise increase of module size with a hierarchical structure is envisaged;

- development of thin, low mass assemblies in order to reduce the multiple scattering, which is particularly important for B-physics applications; thin readout chips can be produced and detector thickness between 100 μm to 200 μm is feasible but reduction of the mass of support and cooling structures may be more effective than reduction of the detector mass;

- study of the optimal operating temperature;
- demostration of successive stages of prototype detector systems in real experiments;
- transfer of technology to industrial manufacturing facilities in order to ensure reliable production of the detectors in a short time frame, at lower cost, as well as to stimulate spin-off;
- some additional, more specific radiation hardness issues may have to be investigated, partly because the pixel detectors are designated for the most severe radiation environments in the collider experiments.

2.1.2 Results

2.1.2.1 Design and performance of the readout cells Basics considerations for pixel readout cells have been studied [23]. Low noise can be achieved at relatively low power dissipation ($\approx$20 μW per cell) because of the segmentation of the detector capacitance. The price to be paid is the complexity of the chip and the overhead in digital electronics.

The first pixel cell for particle detection with latched binary readout has been designed in 1988 in collaboration with Vittoz and Krummenacher [24],[25]. This provided the proof of concept and circuit was measured to have a noise of < 500 e^- r.m.s. in connection with wire-bonded detector cells of ≈ 0.5 pF capacitance [20]. An 8x12 matrix was made and the cells in the electrical test row were found to have a threshold distribution with $\sigma = 2000$ e^- around an average value of 9000 e^-.

Figure 8: Layout of a single pixel cell of 75 μm x 500 μm (0.037 mm^2). The bump pad is seen on the left. The digital delay and strobed multipexer take the right half of the cell.

The second front-end circuit design (fig. 8) used a continuously sensitive comparator and it has been succesfully incorporated in the OmegaD and Omega2 readout matrices, each having 64 rows and 16 columns, with cell size 75 μm x 500 μm (fig. 9). The Equivalent Noise Charge ENC of the cell without detector connection is $\approx$ 80 e^- r.m.s. and for the complete, bump-bonded assembly the absolute value of the noise has been determined to be 170 e^- r.m.s. $\pm$30 e^- or 1.4 keV FWHM using a ^{190}Cd radioactive source, as shown in fig. 10. This isotope emits photons at 22 and 25 keV which could be well separated in a differential threshold scan for single pixels. The threshold is adjustable with lowest practical value $\approx$ 5000 e^- and has signifi antly improved threshold non-uniformity of 750 e^- r.m.s.. A careful threshold calibration has been performed using the electrical test row and this relative scale has been expressed in equivalent absolute electrons using the photon-emitting sources ^{190}Cd, ^{241}Am and ^{57}Co. We should achieve in a future readout circuit a threshold of

2.3 Review of Delphi and CPPM - based developments

The developments are based on the RD19 analogue cell, with the aim to install 330 $\times$ 330 μm^2 pixels in the forward upgrade of the DELPHI microvertex detector for LEP200 [37].

The new electronic cell includes a charge preamplifier, a shaping filter, a discriminator with threshold control, a gate, a latch and some switches for sparse readout. A block diagram and a schematic are shown in figures 21 and 22.

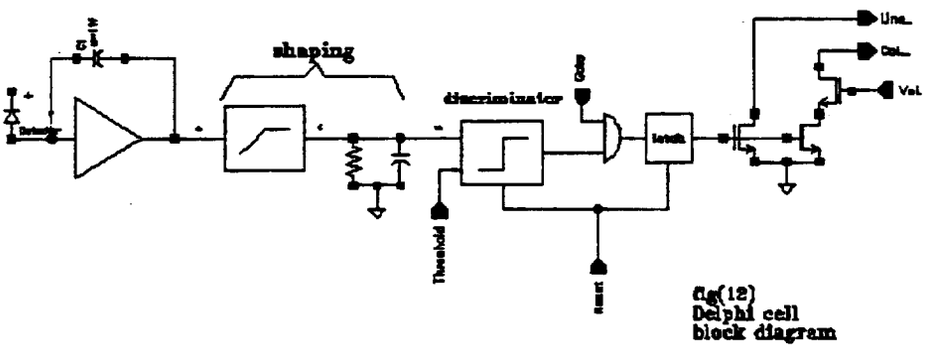

Figure 21: DELPHI pixel unit cell: electronic block diagram.

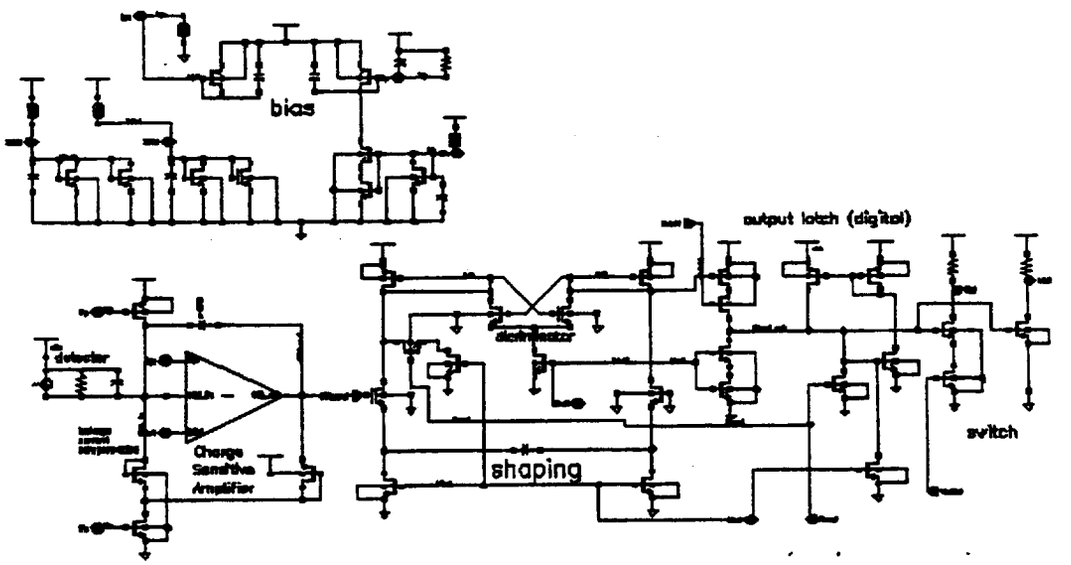

Figure 22: DELPHI pixel unit cell: schematic diagram from electronics.

The sparse system reads out [38] only hit pixels (zero suppression) by addressing synchronously row and column. Pixels are wired-ored by row and column (fig. 23) such the row

signals are activated only in the hit pixels. After data acquisition, a daisy-chain through digital gates between rows scans the rows. The daisy-chain stops when an active row is found, projecting out the coded row address to peripheral logic. At this time, and only for this row, the columns are activated by a validation signal; in the same manner a daisy-chain between columns scans the column signals and stops when an activated column is found. The peripheral logic projects out the coded column address; at the next synchronous clock, the daisy-chain finds the next activated column, etc. At the end of the column scanning, the sparse readout continues to scan rows. This readout logic implements a true sparse scan in 2 dimensions and can operate safely up to 8 MHz.

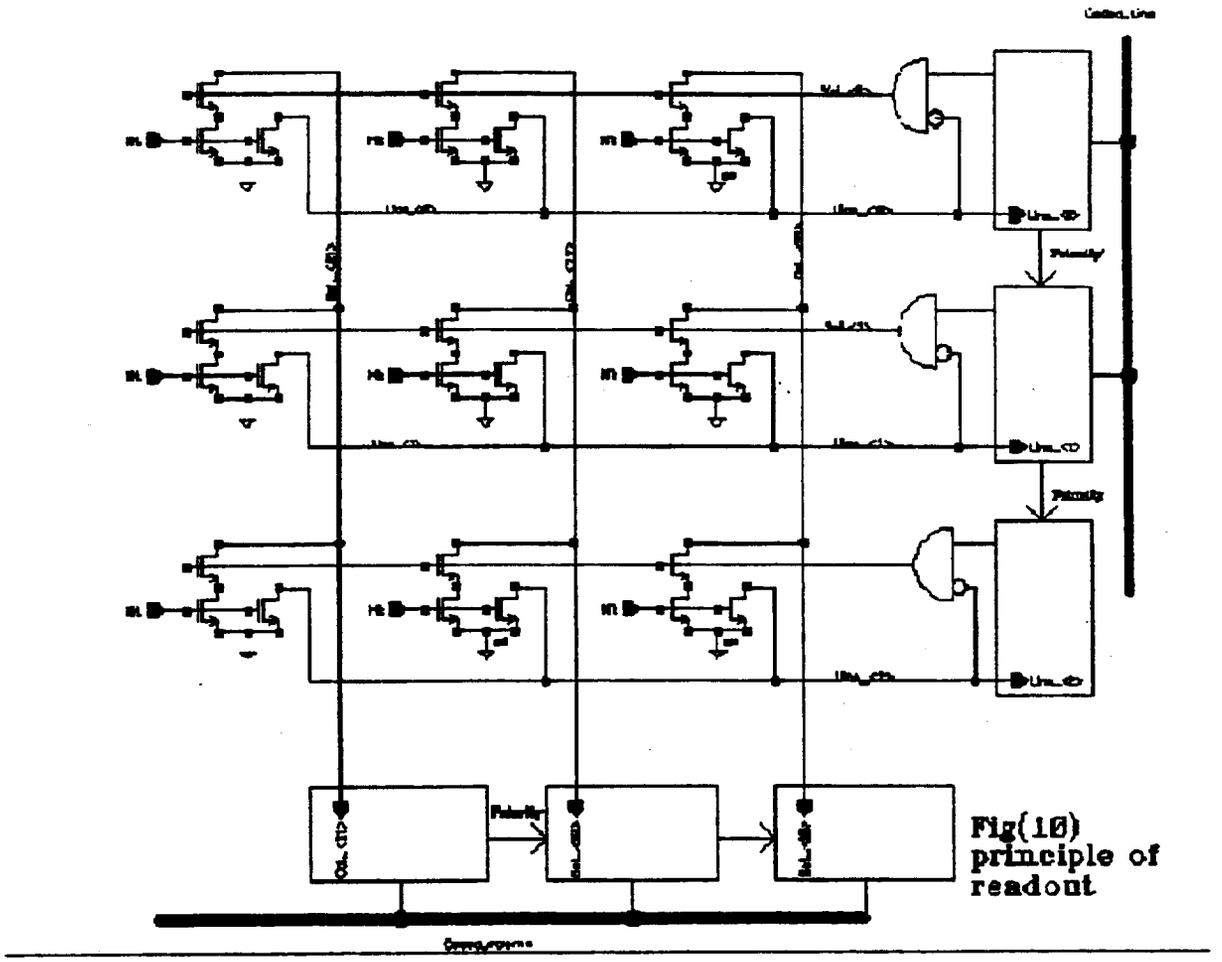

Figure 23: Principle of sparse readout of the DELPHI pixel array.

The analogue part is polarised by column with bias cells located at the bottom of each column. The leakage current, measured by a dummy pixel connected to the bias cell is subtracted from the input current signal. In order to considerably reduce the price of the electronic-to-detector bonding, we have implemented a large pad of 150 $\times$ 150 μm^2 (fig 24), which is about nine times larger than for the RD19 detector. The total input capacitance becomes 1.4 pF, instead of 160 fF. The layout was modified to cope with this larger capacitance. In order to do that, we increased the transconductance of the input device and the feedback capacitance C_f. The diminution of gain ($1/C_f$) is compensated by increasing the

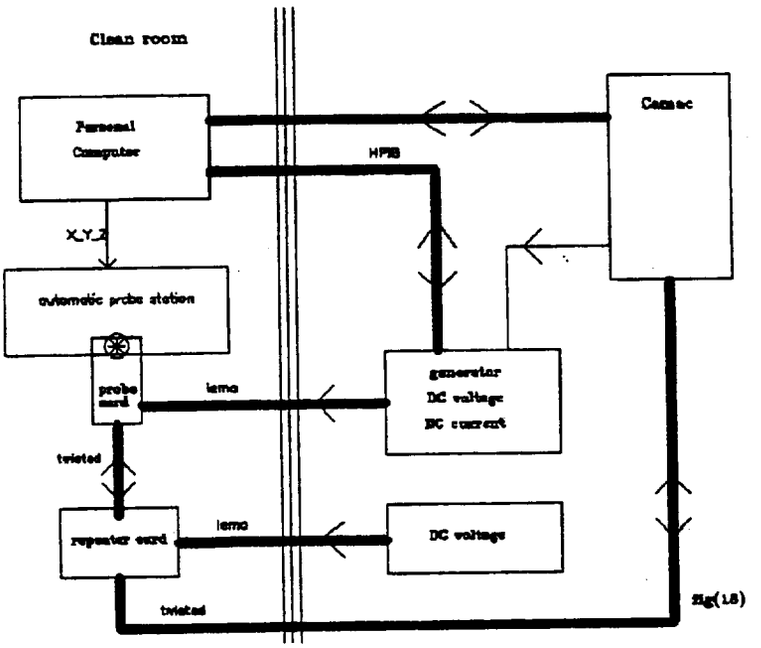

Figure 26: Block diagram of the hybrid tile characterisation station for the DELPHI pixel detector.

- ENC noise: 240 e^-.

Because chips have to be tested prior to bonding (Known Good Die principle) and sorted according to threshold, we installed an automated test system, based on a wafer inspection and probe station (fig. 25 and 26).

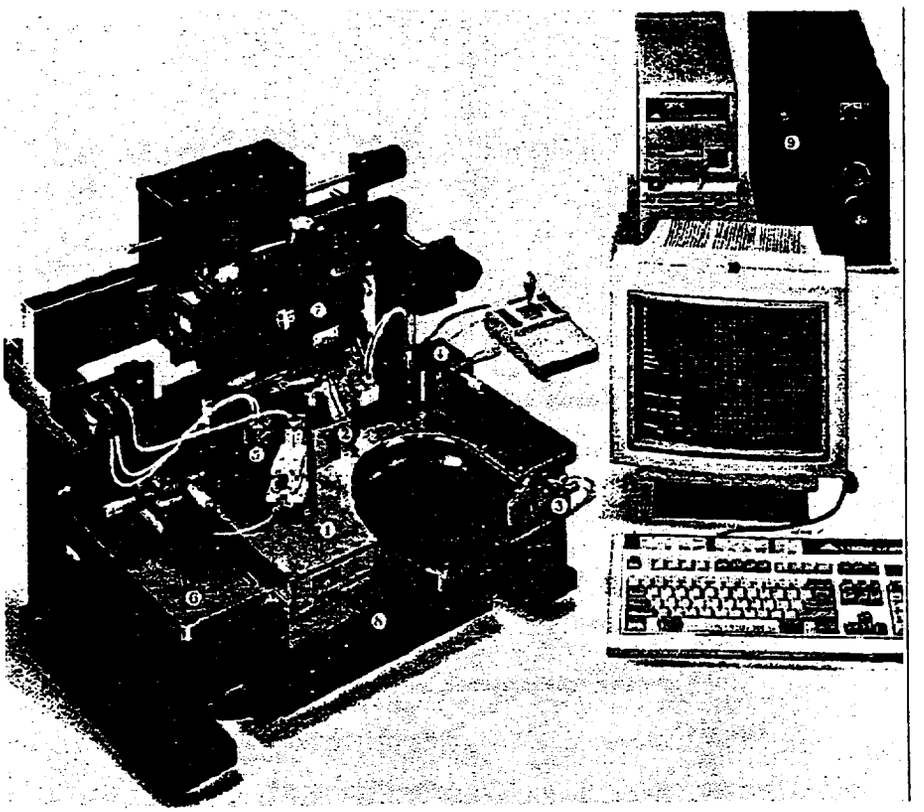

Figure 25: Automated test system for detector hybrid tile characterisation for the DELPHI pixel detector.

The test procedure checks for good chips by their power consumption, the number of noisy pixels, threshold dispersion and a sparse readout logic test in various configurations.

To reduce dead area between chips, all the lines inside the electronic chip are routed to a single edge along which connection pads are implemented (fig. 27).

The DELPHI module shown in fig. 28 and 29 is in many ways a prototype for the ATLAS module geometry. Chips are bonded in two rows on 2 $\times$ 7 cm^2 detector substrates to make hybrid tiles (fig. 28). The substrate contains the pixel diodes, the control and most of the power lines, the signal buses for the readout chips, and their external connections to kapton ribbon cables.

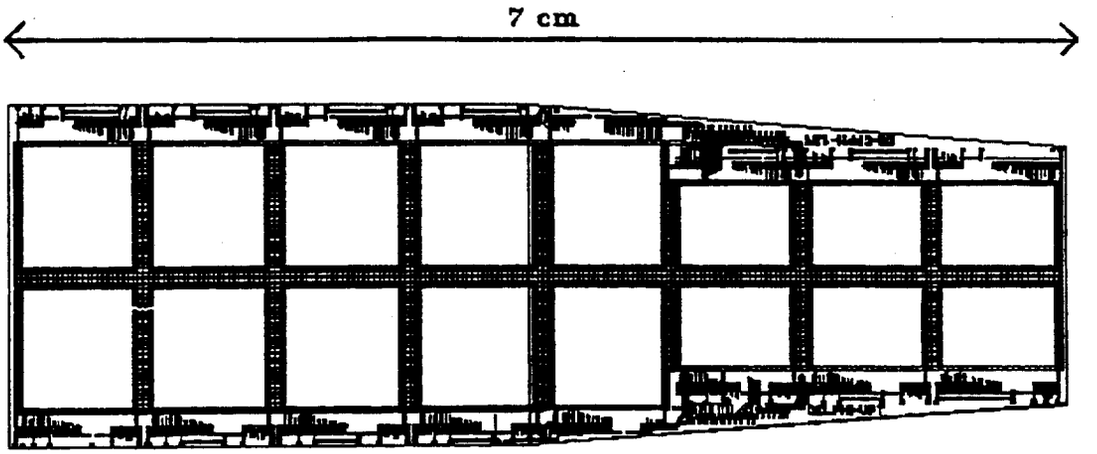

Figure 28: The hybrid pixel detector tile for the upgraded DELPHI microvertex detector.

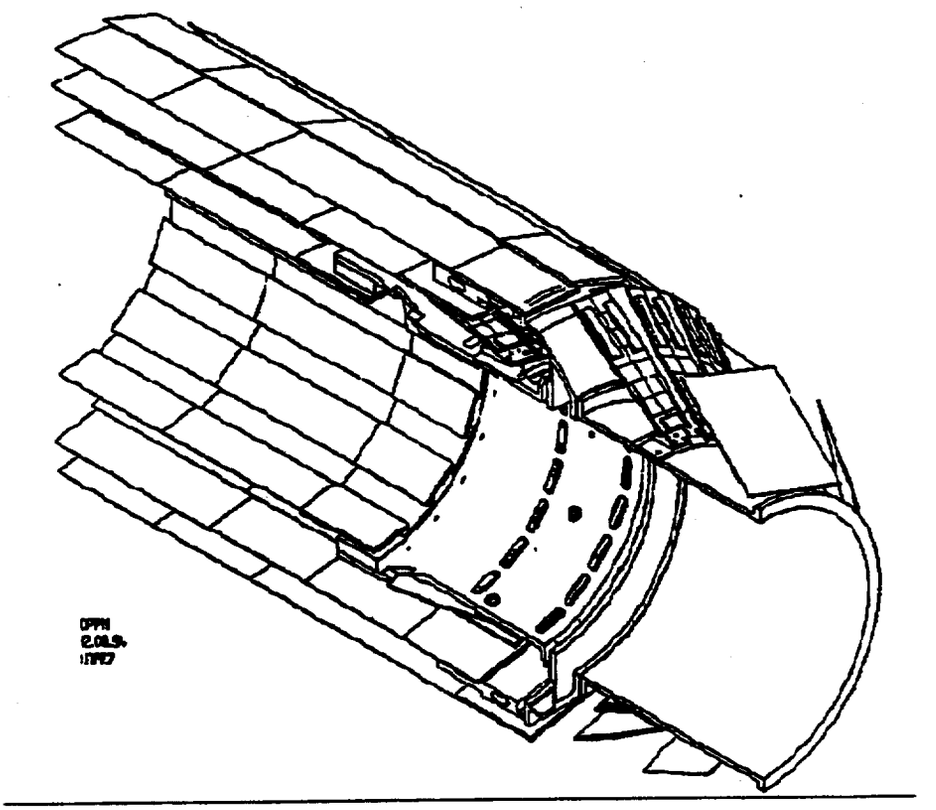

Figure 29: Mounting geometry for pixel detector tiles in the upgraded DELPHI microvertex detector.

1500 e^- with σ = 300 e^- r.m.s. which would come closer to the intrinsic noise value of 170 e^- r.m.s.. Detector signals from $\approx$ 100 μm thick Si detectors ($\approx$ 7000 e^-) could then easily be processed in binary mode.

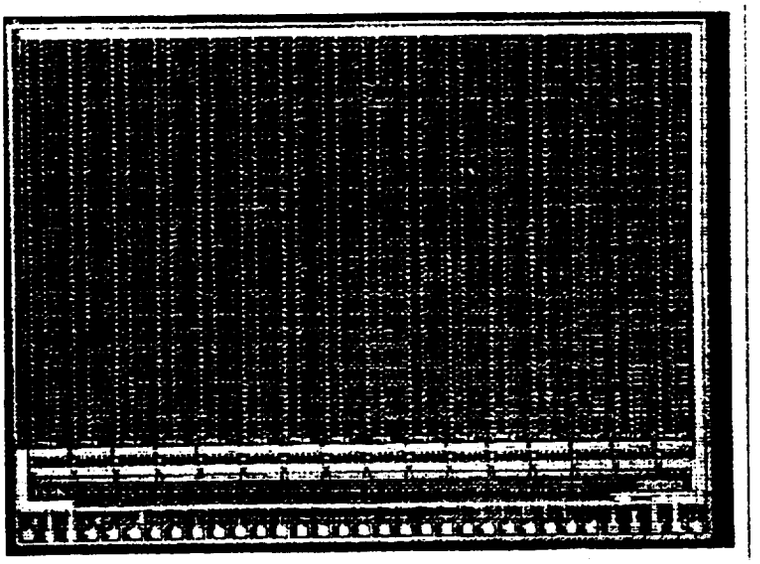

Figure 9: The Omega2 pixel readout matrix of 16 columns and 64 rows. It includes a test at the top. The die size is 6.3 mm x 8.4 mm.

Detection efficiency measurements in a particle beam have been made as a function of the threshold setting with various detectors bonded to a readout chip. The results are shown in fig. 11 for a 300 μm and a 150 μm thick Si detector as well as for a 200 μm GaAs matrix. The silicon results compare well with the expected values based on the Landau distribution indicated by the dotted lines. Inefficiency in the charge collection in the GaAs detector explains the different behaviour, but it should be noted that the detection efficiency achieved is already better than that of the thin Si.

The same type of readout chip has been bonded to a special matrix detector with a thin, transparent window in order to study the sensitivity of this silicon matrix to low energy electrons and light for scintillating fiber detector readout.

The electronics circuit uses only a few μm of Si in the top layer of the readout chip and we have produced 80 μm back-thinned chips which were bonded to the detector matrix. In yet another beam test we verified that their behaviour is identical to that of 'normal' assemblies using 300 μm thick chips, which, actually, already have been thinned from the standard 525 μm thickness.

A third front-end (Anapix) has been designed for analog readout and it incorporates a peak detector. This cell has implemented in an 8-cell linear array which does not yet allow bump-bonding. The noise without detector is 100 e^- r.m.s. and connected with wire-bonded detector cells it is measured to be 200 e^- r.m.s [26].

2.1.2.2 Detector diodes and readout matrix The detector is a matrix of ion-implanted, rectifying diodes, separated by silicon dioxide barriers, as illustrated in fig. 12. For very small sensor elements the capacitance sensed by the front-end amplifier is dominated by the

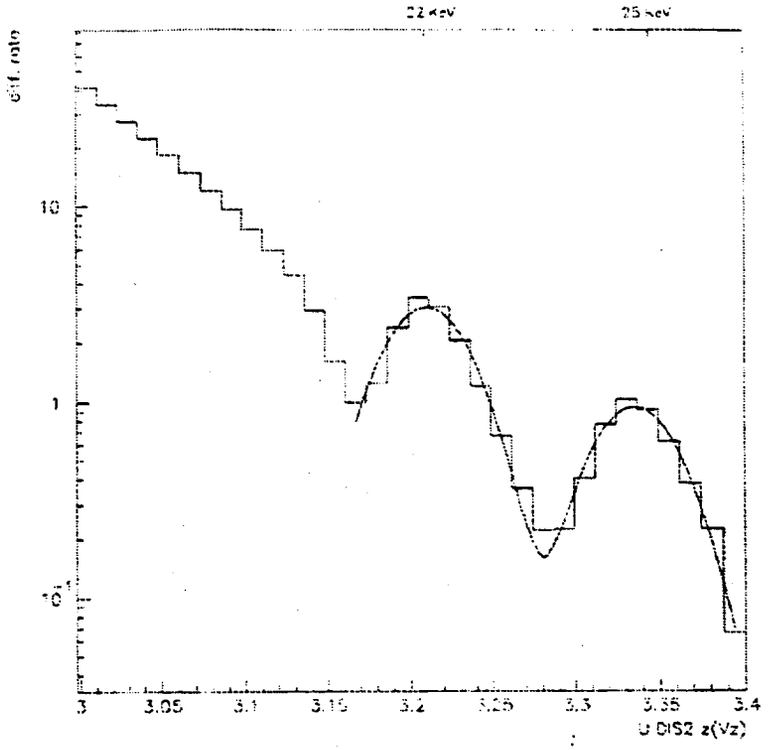

Figure 10: Differential number of counts in an incremental threshold scan for a single pixel irradiated by a ^{190}Cd radioactive source. The 22 keV and 25 keV lines are clearly separated, and this indicates a noise of 170 e^- r.m.s. or 1.4 keV FWHM.

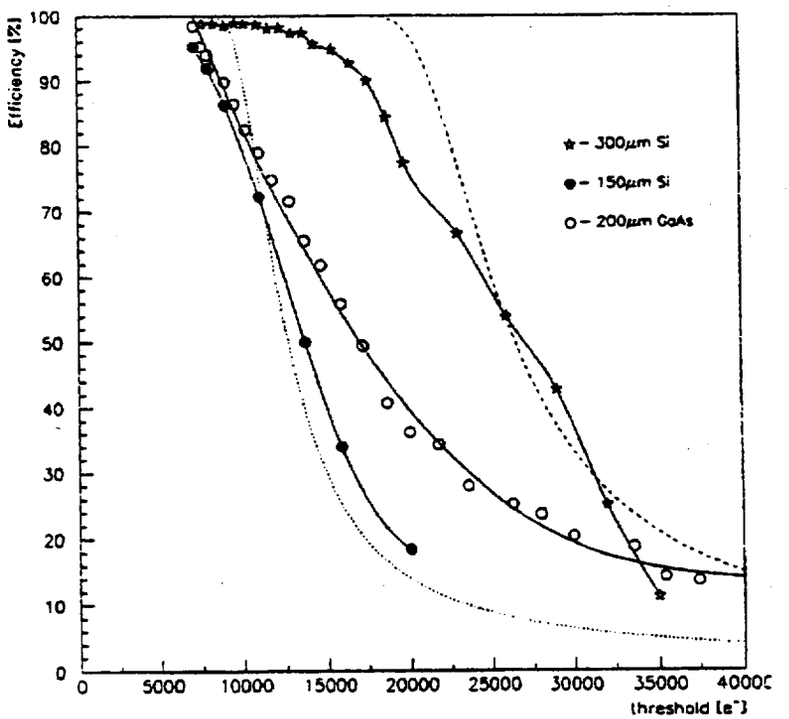

Figure 11: Detection efficiency as a function of threshold setting in e^- for different detector assemblies.

interpixel capacitance [27], which can be reduced by a large diode-to-diode separation. The trade-off is a distortion in the electrical field affecting the speed of charge collection. The external dimensions of a detector chip are imposed by the avilable wafer size (usually ⌀ 100 mm) and manufacturing yield/cost. Detector modules of 6 to 8 cm long currently seem to be the best compromise.

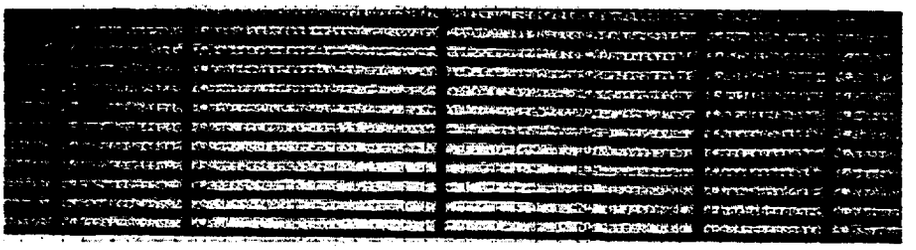

Figure 12: A close up of the detector matrix showing in the middle the region between two readout chips. The height of the cell is 75 μm. Normal cells, left and right, are 500 μm in the horizontal direction, but the 2 cells in the middle are to be connected to the edge columns of the readout chips and they are twice as long: 1000 μm, in order to provide the 'stiching' of the sensitive detector area. The 38 μm diameter bonding contacts can just be seen, and the many small circles are vias between the implant and the metal layer.

The readout chips are limited in size to $\approx$ 1 cm^2 by the lithography limitations and yield. In order to make buttable arrays the pixel cells on these electronics chips must fit exactly on the detector matrix, at least along 3 of the sides. The current cell size of 75 μm x 500 μm is determined by the area of the processing electronics and the bus/supply lines in the matrix. In the 3 μm SACMOS technology ad equivalent 1 μm density has been achieved because of the absence of clearance around the via-contacts (self-aligned contacts). In the future submicron technology even higher densities will be possible, although some of the gains may be lost due to conservative design rules for radiation hardness. A new cell, now under design, will have size 50 μm x 500 μm and the readout chip covers an active area of 0.51 cm^2 with 2048 pixels in 16 columns and 128 rows. Ultimately, we are aiming at sensor with size 50 μm x 300 μm. An equivalent area with different, e.g. square, aspect ratio could be made as well, although the rectangular shape has advantages for the supplies distribution and the columnar organization of the readout. The peripheral electronics on one of the sides of the readout chip may occupy several mm^2 and it contains buffers, logic and slow control.

2.1.2.3 Bump bonding The solder bump-bonding technology has been developed around 1970 by IBM for general application in computer modules, as more reliable alternative to wire-bonding, with a standard bond-size $\approx$ 100 μm. Wire-bonding has been generally used outside IBM due to the lower cost and quite acceptable performance. Fine pitch bonding using indium bumps has been applied since $\approx$ 1980 for Infra-Red imagers, often bonded to CCD readout chips. For the micropattern detector we have chosen a fine-pitch solder bump technology developed by GEC-Marconi Ltd [28].

We found that it is difficult to make a bump-bonded assembly with too small a readout matrix (8 x 12 cells), which moreover had been manufactured on a Multi Project Wafer. The irregular structure of such a wafer is another complication for controlled deposition of

bump connections. Part of a bumped pixel readout chip is shown in fig. 13. In the course of the past 3 years we have processed $\approx$ 100 detector and readout wafers with over 5 million bumps. Careful visual inspection is made before bonding of the components. A very small fraction of the failures after assembly are due to the bump bonding. A study of enhanced automation is being made and this should lead eventually to a significant cost reduction in the bump-bonding.

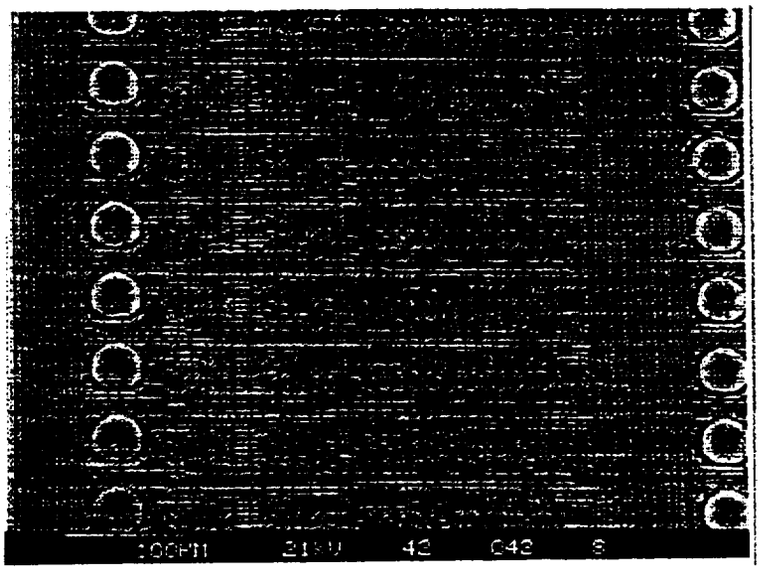

Figure 13: View with a scanning electron microscope of part of a pixel readout chip with $\oslash$ 38 μm solder bumps.

2.1.2.4 Construction and testing arrays Since 1990 we have progressed step by step in the construction and evaluation of pixel detector arrays. In 1991 we tested a telescope of 3 single chip "Omega-Ion" assemblies in the Omega WA94 experiment [29]. Several million triggers were collected, and a typical event is shown in fig. 14. Track reconstruction indicated a precision of $\approx$ 25 μm and the efficiency was 99.2% [30].

In the subsequent "Omega2" chip several weaknesses were improved, e.g. the left-right asymmetry in the duration of the internal delay in each pixel. The spread on the delay in the pixels of one chip has a standard deviation of $<$ 20 ns. A tri-state driver has been added in order to allow sequential data transmission fraom several chips via the same bus [31]. Several readout chips can be bonded onto one detector ladder, as is shown in fig. 15. The stiching area in the middle between readout chips needs to have slightly longer detector diodes, as indicated in fig. 12. The ladder will be the basic building block for the array. In the present array, 6 ladders with 6 chips each are positioned on a common ceramic substrate, as in fig. 16. Two staggered arrays with 175 μm overlap from ladder to ladder are needed to cover a 53 mm x 55 mm sensitive area hermetically with a total of 72576 pixels.

In 1993 we have demonstrated in a test with reference wire-chambers as well as in the Omega WA97 experiment the first 29 cm^2 hybrid pixel array with 72576 contiguous sensor elements [32]. The tracking precision was now $\approx$ 20 μm and the noise hits $<<$ 10^{-6}. The

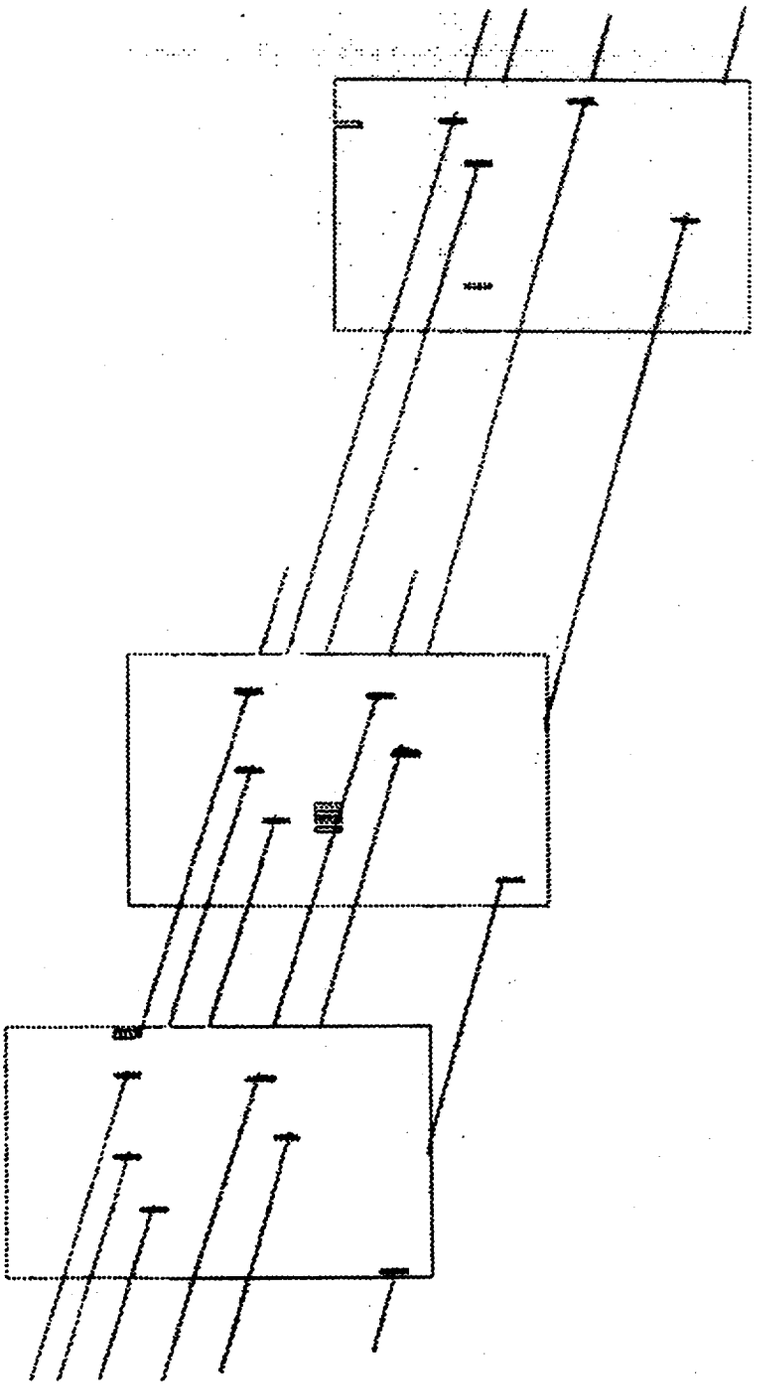

Figure 14: Tracks from a typical event in the Omega WA94 sulphur experiment, seen in the 3-plane pixel telescope.

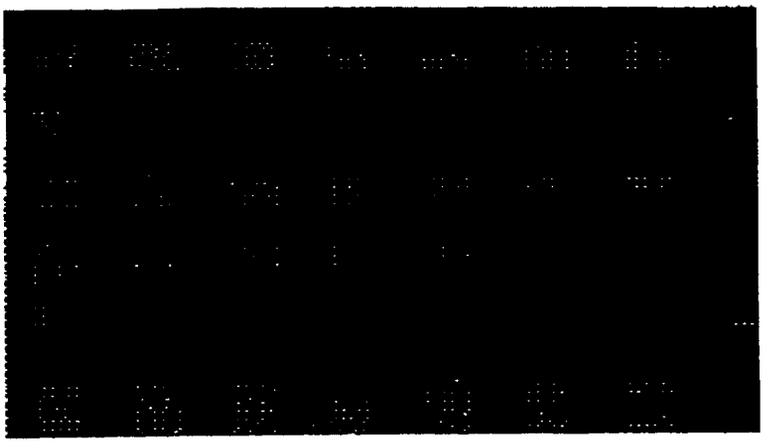

Figure 15: Photograph of 2 ladders, with the detector substrate upwards (top) and with the 6 attached readout chips upwards. Each ladder contains 6048 sensitive sensor with associated electronics.

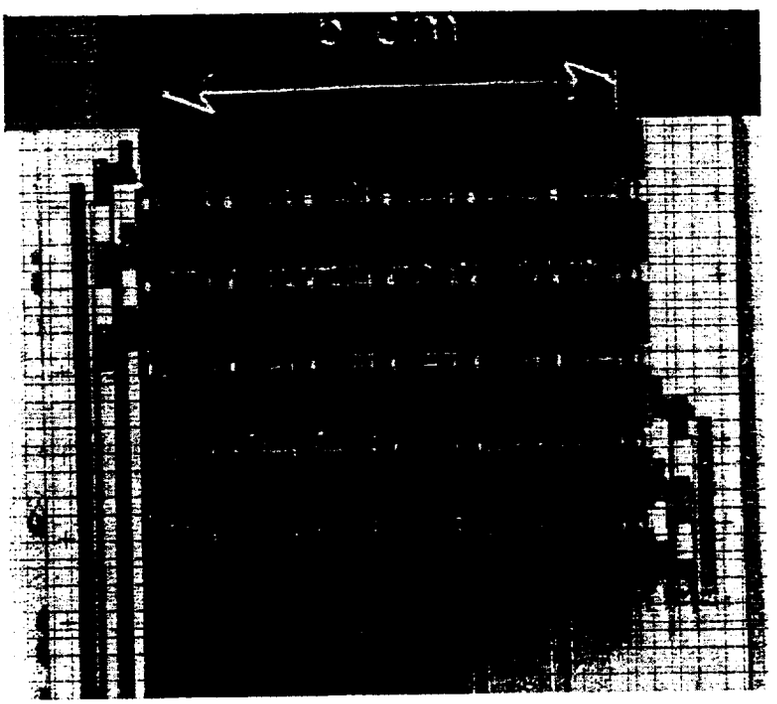

Figure 16: Photograph of a complete array of 6 ladders. This array has 32288 detecting elements and a second, identical array, staggered over the open "slots" completes a full detector plane. One can see the dark back side of the detector chips and the bias filter capacitors beside each ladder.

dead area on the first array was 2%, on the second, however, only $\approx$ 80% of the area was active.

Following a considerable effort in evaluation and component testing we have constructed in the course of 1994 four complete planes which are being used in WA97 in the first Pb run at the SPS. The total number of pixels is now close to 300,000 and the dead area on all planes together is $< 3\%$. Fig. 17 shows plots of hits in 3 planes, totalling 216 chips on 36 ladders. Several additional planes are being prepared, and besides being useful for the lead physics program, this work teaches us how to improve testability and reliability of the pixel detector arrays in the future versions.

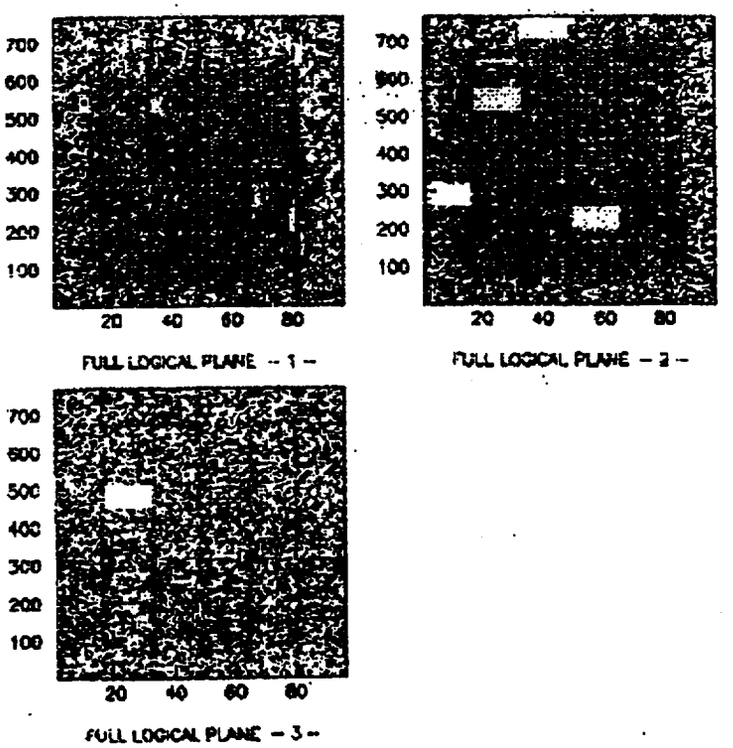

Figure 17: Tracks from a typical event in the Omega WA94 sulphur experiment, seen in the 3-plane pixel telescope.

2.2 Review of LBL-based developments

In the late 1980's, a collaboration between Hughes Aircraft Co., Berkeley Space Science Laboratory and SLAC began development of hybrid pixel detectors for particle physics applications. Figure 18 (after [33]) shows a generic hybrid pixel array, with detector and electronic components bonded together with the Hughes 15 μm indium bumping process.

Between 1989 and 1991, two readout chip geometries were studied: a (10 column $\otimes$ 64 row) array of 120 μm square pixels and a (256 $\otimes$ 256) array of 30 μm square pixels. Each cell contained a charge storage element: readout of the (10 $\otimes$ 64) array proceeded via 10 parallel, columnar analogue shift registers while the (256 $\otimes$ 256) array used two orthogonal 256 element analogue shift registers. There was no sparse scan or time stamping.

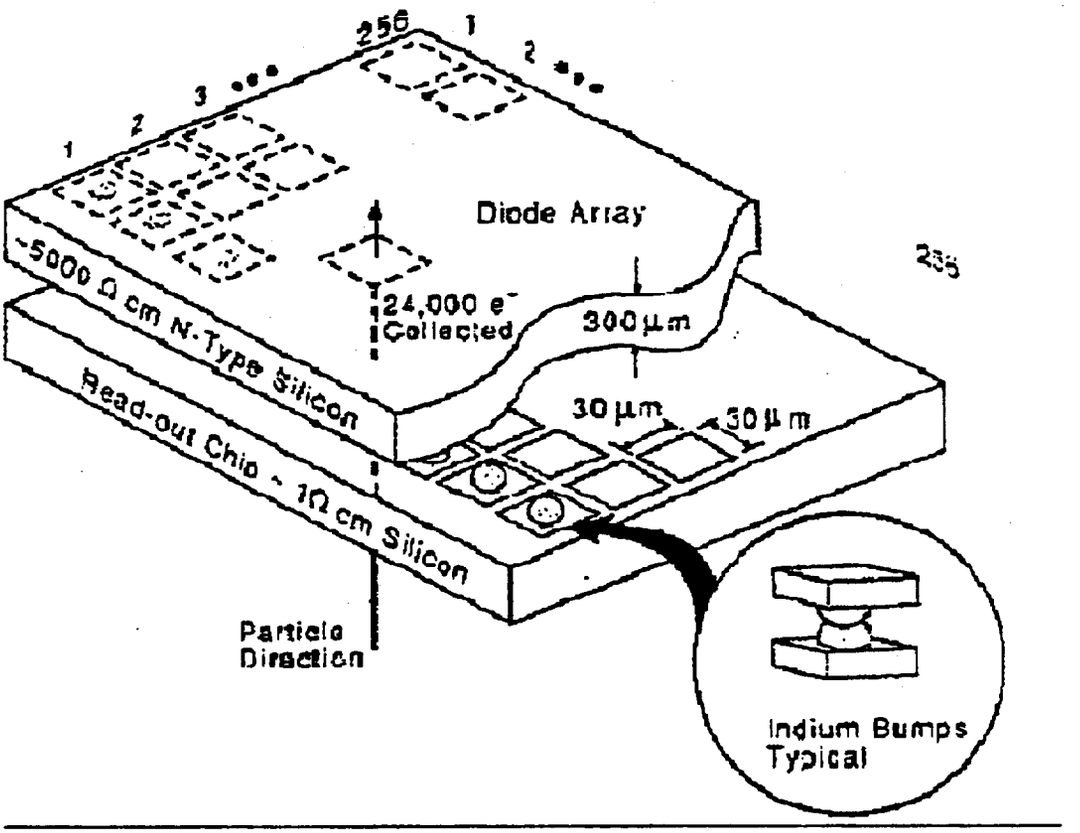

Figure 18: Schematic of a hybrid pixel detector, showing the attachment of the detector and readout electronics: in this case by Hughes 15 μm indium bump bonding process.

Off chip charge measurement and interpolation gave typical noise $\leq$ 300 e^-, and signal to noise ratio in the range 50-100:1 (300 μm detector). Beam tests of the 30 μm square pixel arrays with analogue charge interpolation between neighbouring pixels [6] demonstrated an outstanding spatial resolution of $\sigma \leq \pm$ 3 μm (fig. 19). In 1991, back-thinning of readout electronics from 300 μm to 50 μm (following indium bump bonding to a detector wafer) was successfully demonstrated by Hughes, leading to the prospect of hybrid pixel detectors with overall thickness less than that of silicon microstrip detectors.

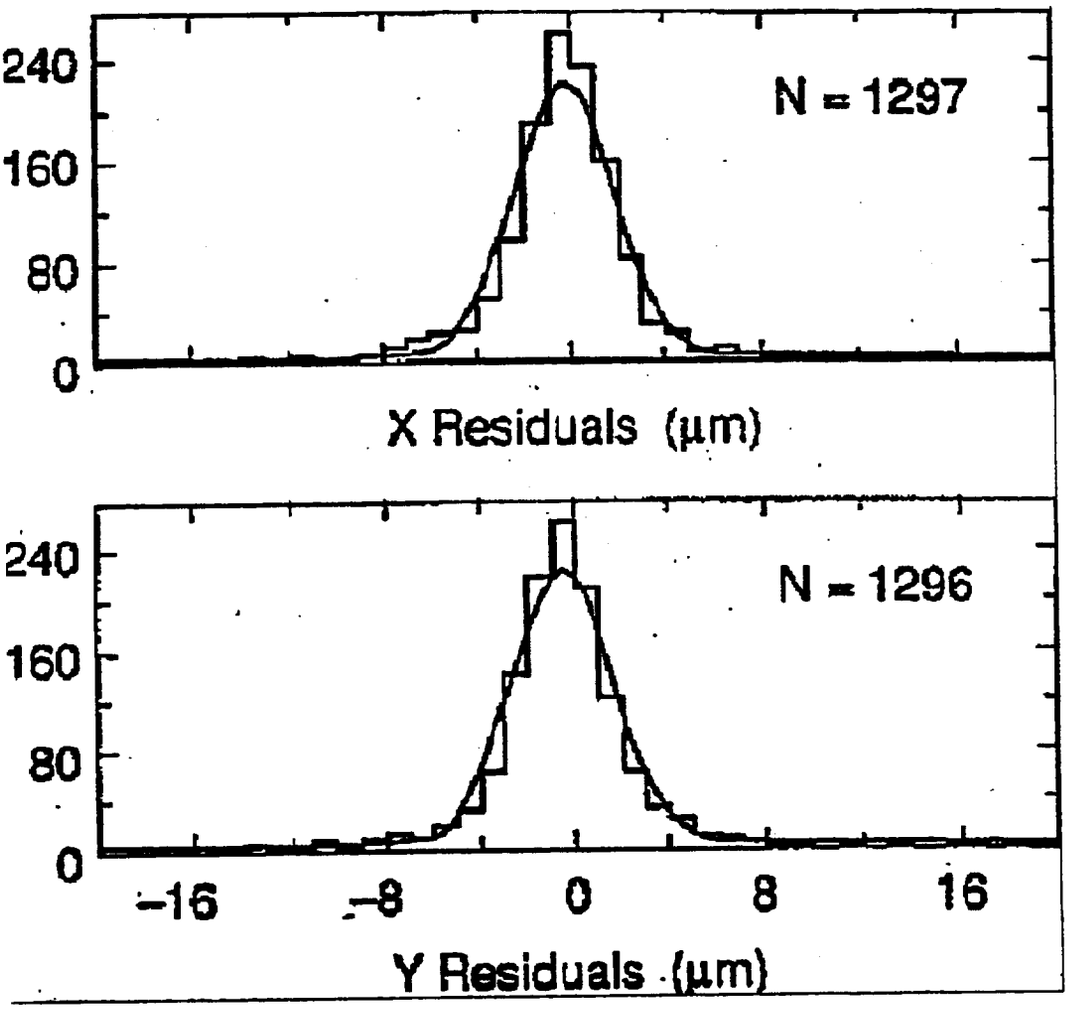

Figure 19: Special resolution of $\sigma = \pm$ 3 μm demonstrated in beam tests of arrays of (30 μm $\otimes$ 30 μm) pixels with Hughes readout and analogue charge interpolation [33, 34]

The SSC Pixel Detector Development Collaboration, established in 1990, set design goals for pixel detectors for high luminosity at SSC [34], which included:

- Peripheral architecture to selectively read out the 2D coordinates and analogue charge (with a dynamic range of 500) stored in pixels with charge above threshold, with additional neighbour tagging logic to allow high spatial resolution through charge interpolation;

- Ability to self-test and disconnect bad pixels;
- Time stamping to 16 ns resolution;
- A maximum noise per pixel 200 electrons rms;

In 1991, a developmental readout chip (Hughes "4": a (64 $\otimes$ 32) array of (50 μm $\otimes$ 150 μm) cells) was fabricated to realise as many as possible of the above design goals. The unit cell architecture - shown in fig 20 (after [34]) - contains a charge storage element, amplifier, a comparator to signal pixels with charges above threshold to row and column shift registers, and peripheral row and column addressing to read out their analogue charge. Though meeting many of the SSC goals, the architecture exhibited an unacceptably large comparator time walk, while the digital signaling of hit pixels to periphery caused significant interpixel crosstalk. Despite further improvements, increases in the projected SSC luminosity and trigger level 1 latency caused concern that an architecture with access relying on shift registers along both orthogonal dimensions would be pushed very close to its operational limits.

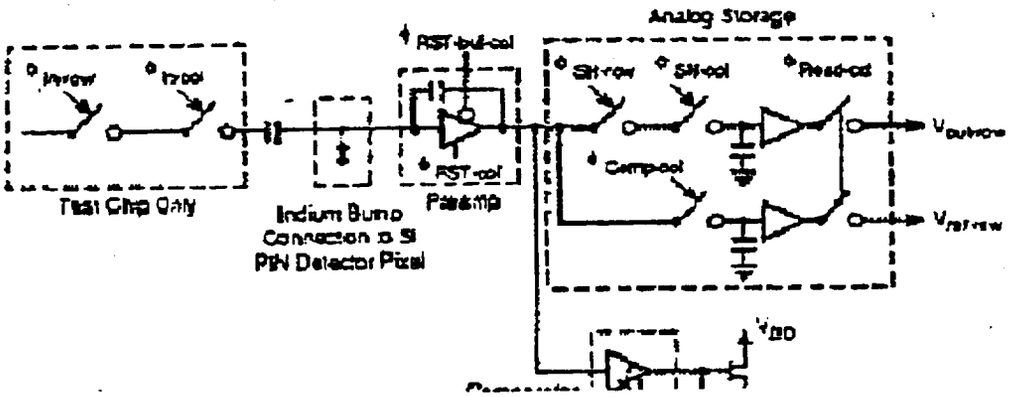

Figure 20: Generic pixel unit cell architecture (SLAC-Hughes-BSS collaboration), with charge storage element, comparator to announce a pixel with charge above threshold to row and column shift registers, and row and column addressing to read out the analogue charge.

At LBL, a columnar "data - driven" pixel readout architecture has been investigated in a series of custom chips (LBL 1-4) [35] requiring no clocks or resets to establish the sensitive state. Columns of pixels communicate in one dimension, using currents to reduce crosstalk, with peripheral storage FIFOs. These store only the BCOs and associated pointers for corresponding pixel hits in the column, and have a depth of 4 or 8 steps (depending on eventual trigger latency). "Smart" pixels have a 2 or 3 bit memory to store their BCO pointers. BCO pointer comparison will be destructive, resetting the pixels. Charge and 2-D

data from pixels with a BCO pointer other than that of a level 1 trigger are not read out, and they reset themselves after a time slightly longer than the trigger 1 latency.

The history of the three design cycles for the LBL Pixel Unit Cell (PUC) are given in the table 3:

Table 3: LBL Pixel Unit Cell Design History

	LBL-1	LBL-2	LBL-3	GOAL
Noise (e^-)	50	200	120	$\leq$200
Time-walk (ns)	19	8	10	$\leq$14
Q range (fC)	2 - 8	1 - 8	1 - 8	1 - 8
Q Linearity$\pm$%	20	1	3	$\leq$10
dQ/dt (fC/μs)	—	$\sim$0.5	3.3	6.0
Q_T Threshold (e^-)	—	1000	1000	1000
Δ Q_T (e^-)	3000	41	150	$\leq$200
Gain (V/fC)	0.2	2.0	2.0	2.0
Max I_{Input} (nA)	—	$\sim$1	26	$\approx$30
Power (μw)	60	144	15	$\leq$30
Pixel Area (μm^2)	—	50 x 150	50 x 536	50 x 300
Crosstalk, IC	—	$\leq$0.5 Q_T	—	$\leq$0.5 Q_T

Values for LBL–3 are simulations, whereas indicated values for LBL–1 and LBL–2 are measurements. Measurements for LBL–2 have shown:

- Successful implementation and measurement of a 600 aF integrator feedback capacitor;
- 30 GHz integrator gain-bandwidth product;
- One part in 140 channel-to-channel cross-talk with no false triggering of neighbors by a 12 fC hit;
- A 3 fC/μs charge-to-time-over-threshold conversion rate with 3% standard deviation in output pulse width from channel-to-channel;

To make a 2D array(LBL–4), the PUC LBL–3 was incorporated with end-of-column logic that provides time-stamping and readout capability. Also, new circuits were added to LBL–3 such as:

- A PUC selection and calibration circuit to enable electrical test of every PUC in an array before hybridization;
- An interface between the PUC and EOC arrays;
- A replica PUC to simplify chip bias in new operating modes such as open-loop detector leakage cancellation;
- Current-to-binary PUC location address converters;
- Analog store read out amplifier.

LBL-4 and its application to ATLAS are described in Chapter 3.

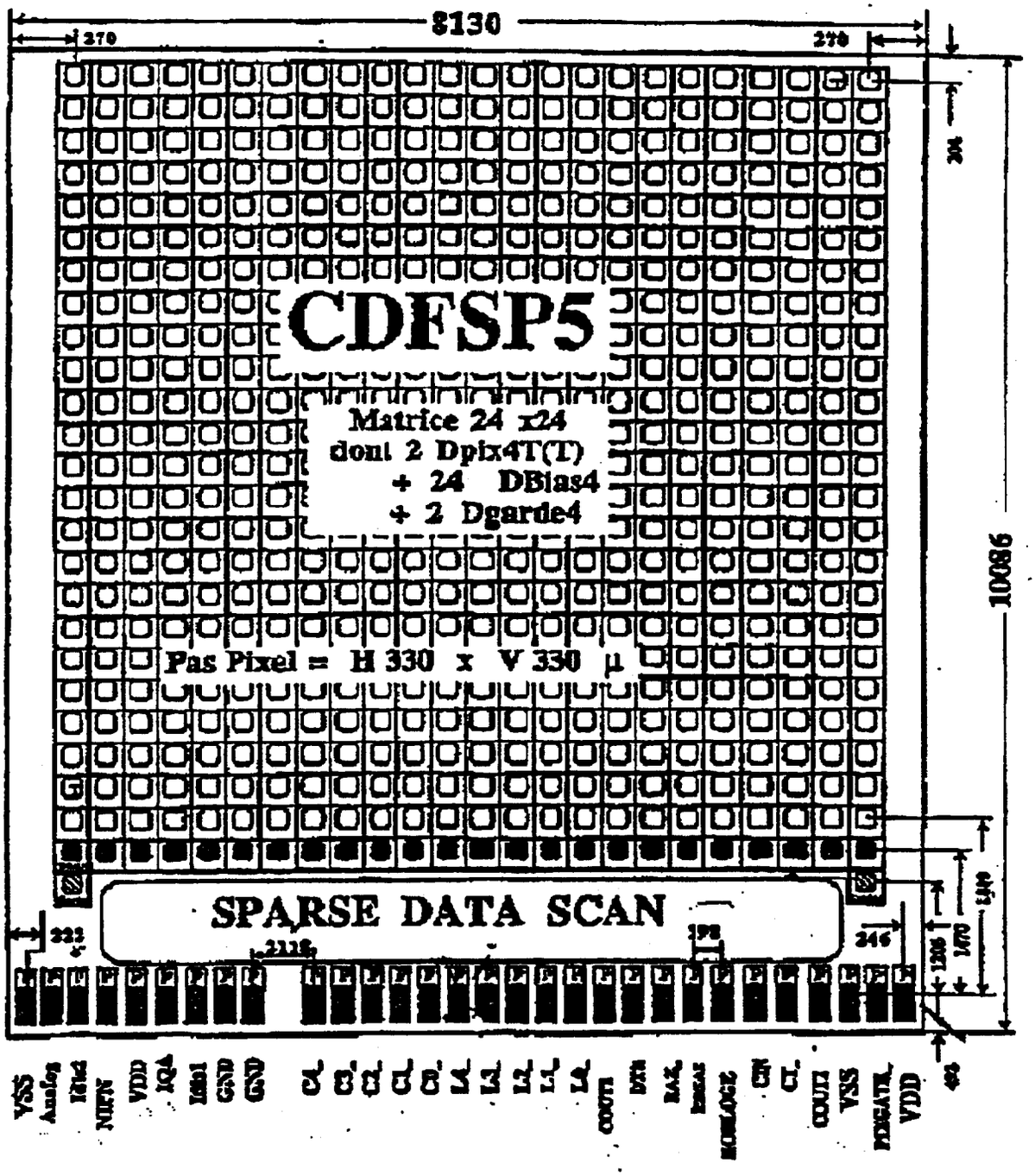

Figure 27: Organisation of the sparse readout chip for the DELPHI pixel detector: the chip I/O connectors are gathered along one edge.

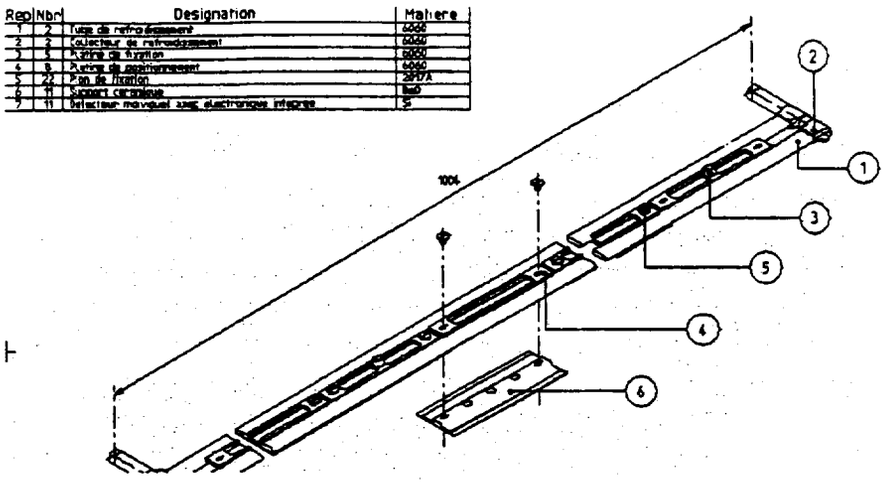

Figure 30: Ladder support showing the two cooling channels and the mounting points for pixel detector modules.

4. low cost (relative to an all - beryllium structure) through the use of thin extruded aluminium cooling channels. A brazed aluminium-beryllium overall assembly is envisioned.

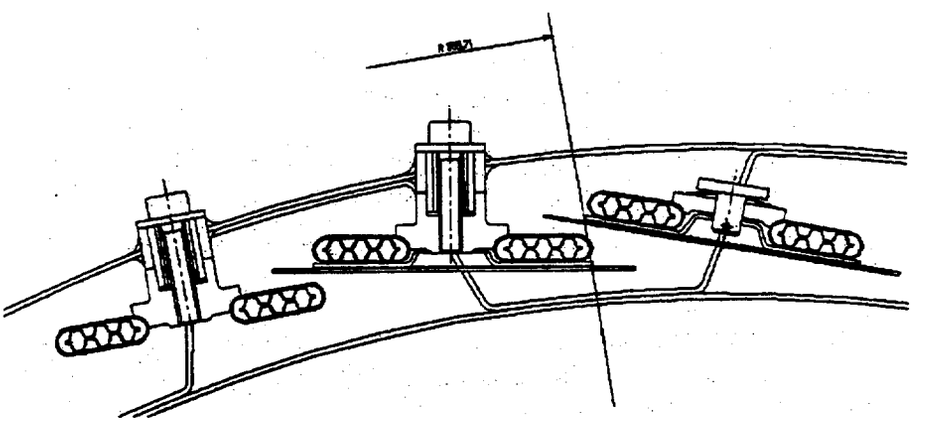

Figure 31: Cross sectional view of the detector support cylinder, showing the mounting of detector ladders.

3.1.1.1 Radiation Lengths The material (X/X0) breakdowns for the B physics (4 cm radius) and high luminosity (11.5 and 16.5 cm) barrel and the disk pixel tile modules, assuming normal incidence, are shown in table 4. The effects of electronics, cooling, cabling and support are averaged over the whole tile area (example: 62.8 mm $\times$ 22.6 mm for barrel pixel tiles) but do not include factors to take account of the overlap in azimuth between adjacent tiles.

3 The ATLAS Pixel Project

3.1 Mechanics and Alignment/stability

The mechanical structure for the cylindrical and disk pixel surfaces has the dual purpose of delivering cooling fluid to the pixel surfaces and of supporting the detectors with a maintained dimensional stability of the order of 10-20 μm, at constant temperature [39]. Position changes may be caused (mainly) by temperature fluctuations, but also by the effects of moisture absorption by composite structures and by creep effects, which could be radiation damage dependent. It has been proposed [40] that the relative positions of pixels should be known and stable in time to an accuracy of (10 μm (ϕ) $\otimes$ 25 μm (z)) (cylinders) and (10 μm (ϕ) $\otimes$ 25 μm (r)) (disks). An assembly precision (before surveying) of (100 μm (ϕ) $\otimes$ 500 μm (r) $\otimes$ 1000 μm (z)) has been proposed for the semiconductor tracking elements the ATLAS inner detector [41]. This correspondingly requires a relative position monitoring precision at least an order of magnitude better, though absolute pixel positions will eventually be deduced from track data. Studies of the effects of detector misalignment (through placement imprecision) on mass resolution in certain B physics channels have been made [42]. The B_d mass resolution in the decay channels $B_d \rightarrow J/\psi\ K_s$ and $B_d \rightarrow \pi^+\ \pi^-$ was degraded by a factor of about two with (in-plane) placement imprecision of 250 μm: it should however be possible to monitor and maintain pixels to a significantly higher precision than this. In the sections below we present two different concepts for the mechanical and cooling systems.

3.1.1 Barrel Mechanical System (CPPM design)

The proposed barrel pixel mechanical support structure (under study at CPPM) is shown in cross section in fig 31. It has several components:

- layer support cylinders consisting of a single 0.4 mm beryllium skin over most of their lengths - reinforced at each end with two more 0.4 mm beryllium braces, and divided axially into two demicocques for access to the detector modules - carrying aluminium inserts for the attachment of detector ladder supports;
- axial detector ladder supports (aligned parallel to the LHC beam), consisting of pairs of thin aluminium cooling channels (0.15 mm wall), carrying spring clip attachments for individual silicon detector tiles (fig 30);
- a cooling fluid recirculation system under development.

Such a structure has several advantages:

1. a very high rigidity to mass ratio through the use of cylinders in beryllium (Young's modulus = 340000 Nm m^{-2}, density = 1.85 g cm^{-3});
2. a high degree of modularity with both the axial support / cooling ladders and the silicon detector modules individually demountable (fig 31);
3. lightness, through combination of support and cooling functions in the same structure, minimising the multiple scattering of particles crossing the detector (table 4);

Table 6: Total radiation lengths* (% X/X0 at normal incidence) for each cylinder and disk element of the pixel system. The B-physics layer components are listed separately. (*)For simulations which calculate module overlap automatically from module geometry. (**) Optional at this stage; engineering studies to see if it will be necessary.

Radius (cm)	Z-start (cm)	Z-end (cm)	Total Percent X/X0	Element	Active/Dead Material
4.00	0.00	35.04	0.79	B pixel layer	A+D
5.00	0.00	45.00	0.11	B layer Be Support shell	D
5.05	35.04	45.00	0.17+0.30	B layer cooling, cabling	D
5.05	35.04	45.00	0.24	Be Cyl: Be end Reinforc. ring	D
11.5	0.00	35.04	0.86	11.5 cm pixel layer	A+D
12.5	0.00	45.00	0.11	11.5 cm layer Be Support shell	D
12.55	35.04	45.00	0.24+0.30	11.5 cm layer cooling, cabling	D
12.55	35.04	45.00	0.24	Be Cyl: Be end Reinforc. ring	D
16.5	0.00	41.42	0.86	16.5 cm pixel layer	A+D
17.5	0.00	45.00	0.11	16.5 cm layer Support shell	D
17.55	35.04	45.00	0.24+0.30	16.5 cm layer cooling, cabling	D
17.55	35.04	45.00	0.24	Be Cyl: Be end Reinforc. ring	D
22.5	0.00	45.00	0.30	Overall cylind. stiffener (in active volume**)	D
22.5	45.00	86.00	0.36	Outboard cylin. support structure	D
22.5	45.00	86.00	0.07+0.07	B layer Outboard Cooling , cabling	D
22.5	45.00	86.00	0.39+0.37	Outboard cooling cabling (11.5 and 16.5 cm layers only)	D
22.5	49.92	55.40	0.11	cooling and cabling for 1st disk	D
22.5	55.40	79.90	0.22	cooling and cabling disks 1 and 2	D
22.5	79.90	85.00	0.33	cooling and cabling Disks 1, 2 and 3	D
22.5	85.00	86.00	0.44	cooling and cabling Disks 1, 2, 3 and 4	D

Table 4: Radiation length (% X/X0) contribution from pixel module components (no overlap; see text).

Component	Barrel Pixel Modules (4 cm B physics layer)	Barrel Pixel Modules (11.5 & 16.5 cm layers)
Silicon detectors	0.16	0.16
Electronics + bump bonding	0.14	0.14
Cooling tube	Incl. in "Cooling"	Incl. in "Cooling"
Support	0.11 (contr. of external support shell in Be)	0.11 (contr. of external support shell in Be)
Coolant (average)	0.17 (liquid film + tube in Be)	0.24 (liquid film + tube in Al)
Cabling (average)	0.14	0.14
Module attachments (average)	0.18	0.18
TOTAL	0.90	0.97
TOTAL Ecl. Indiv. Be Support Shells	0.79	0.86

Table 5 summarises the effective total radiation lengths for the 4, 11.5 and 16.5 cm layers, when the effects of azimuthal overlaps between adjacent detectors tiles are also taken into account.

Table 5: Radiation lengths of barrel pixel layers, including overlap.

Layer radius (cm)	Base X/X0 (No overlap) (%)	Overlap addition (%)	Total (inc. 0.11% X/X0 Be support shell)
4.0	0.79	0.095	1.00
11.5	0.86	0.097	1.07
16.5	0.86	0.105	1.08

For the forward pixel disks 3.1.2.2, X/X0 increases from 0.94% to 1.21%, taking overlap into account.

A plot of radiation lengths vs rapidity is given in fig 32(a,b) for the system without [with] the B-physics layer. The forward pixel disks are added. Module overlap is taken into account.

The design of the pixel mechanical structure, the cooling and the electrical services is at an early stage.

To facilitate simulations in which module overlap is calculated automatically from a give module geometry, tables 6 and 7 (based on [8]) summarize the present estimate of total radiation lengths for various cylindrical and disk elements of the pixel system. Components of th B-physics layer are listed separately. Radiation lengths are ϕ averaged and (r, z) dimensions of elements are shown.

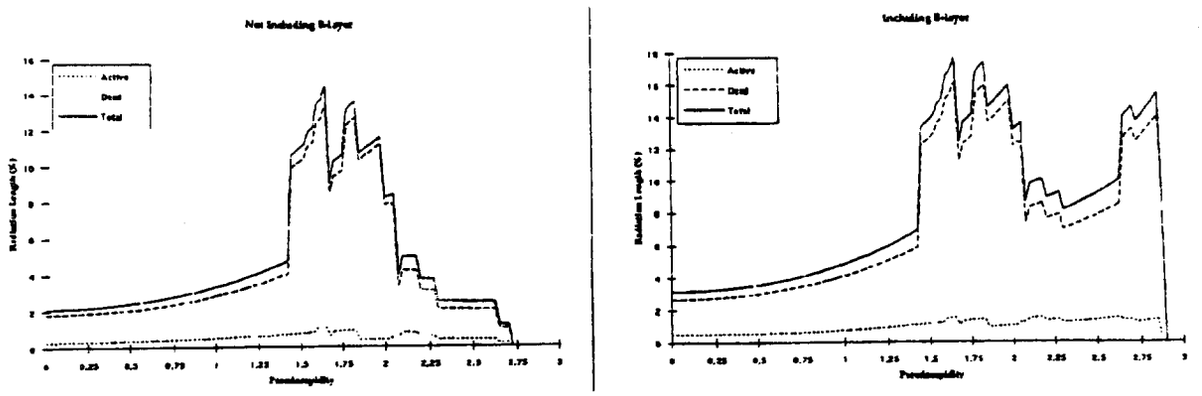

Figure 32: Material distribution as a function of η.

The pixel services must be routed through the gap between the silicon tracker and the first TRT disk. The approximate radiation length of these services is (25 cm/R) $\otimes$ 0.89 without the B-physics layer and (25 cm/R) $\otimes$ 0.94 with the B-physics layer. At the outermost radius these must be added to other services.

3.1.2 Mechanical System (LBL design)

The nominal layout of the pixel detector system has been given in Chapter 2. However figures in this chapter may have dimensions that do not agree with dimensions given in Chapter 2 as some simulations and calculations were done on earlier system layouts. In addition, there are differencies in chip sizes and modules between the CPPM-based and the LBL-based design.

3.1.2.1 Barrel mechanical system The basic detector unit for the barrel, shown in Fig. 33, is a module 29.80 mm in azmuthal dimension and 59.95 mm in z dimension. In our present conceptual design modules are afixed to structural members to form staves that parallel the beam or z axis. Staves are then arranged in overlapping fashion to form a cylinder or barrel layer. Table 8 gives the average radiation length thickness for such a barrel layer.

Table 8: Average radiation length over azimuth for a barrel layer of the carrier design option.

Silicon detector including 55% overlap	0.41%
Silicon electronics including 34% overlap	0.14%
Bump bonds	0.01%
Carbon-carbon carrier	0.34%
Berylium tube 3 mm OD	0.06%
Coolant	0.05%
Cabling	0.10%
Total	**1.11%**

An overview of three barrel layers is shown in Fig. 34. Figure 35 gives an end view of three

Table 7: The total radiation lengths in each disk element of the pixel system with the B-physics layer and the dimensions (r,z) of those elements. All dimensions are in centimeters. Radiation lengths are averaged over ϕ and are for normal incidence.

Z (cm)	r-Inner (cm)	r-Outer (cm)	Total Percent X/X0	Element	Active/Dead Material
49.92	11.4	21.3	0.94	1st Disk Layer	A+D
49.92	21.25	22.5	0.18	1st Disk Support + services	D
54.40	11.4	21.3	0.94	2nd Disk Layer	A+D
54.40	21.25	22.5	0.18	1st Disk Support + services	D
79.90	11.4	21.3	0.94	1st Disk Layer	A+D
79.90	21.25	22.5	0.18	1st Disk Support + services	D
85.00	11.4	21.3	0.94	1st Disk Layer	A+D
85.00	21.25	22.5	0.18	1st Disk Support + services	D
45.00	5.0	12.5	015+0.14	B layer B cooling , cabling	D
45.00	12.5	17.5	0.09+0.08	B layer B cooling , cabling	D
45.00	17.5	22.5	0.07+0.06	B layer B cooling , cabling	D
45.00	12.5	17.5	0.22+0.23	11.5 cm and B layer cooling, cabling	D
45.00	17.5	22.5	0.545+0.43	16.5, 11.5 cm and B layer cooling, cabling	D
45.00	5.00	22.5	0.36	Beryllium Spacer for cylinders	D
86.00	22.50	30.00	0.05	Spacer supporting pixel system from strip support at r = 30 cm.	D

layers at radii of approximately 5 cm, 11 cm, and 16 cm. The tilting of each stave allows for active area overlap in the azimuthal direction and some optimization of Lorentz-angle effects.

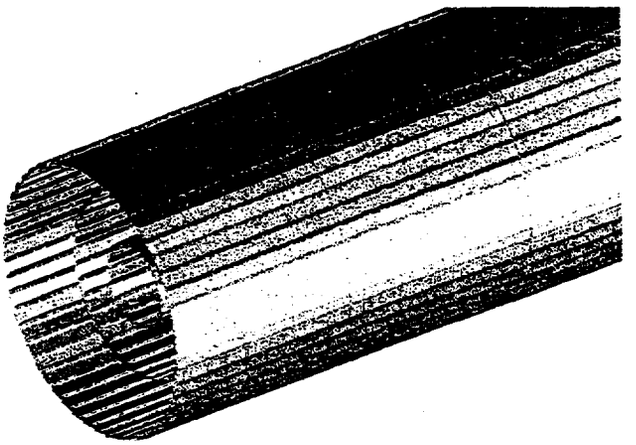

Figure 34: Overview of three barrel layers

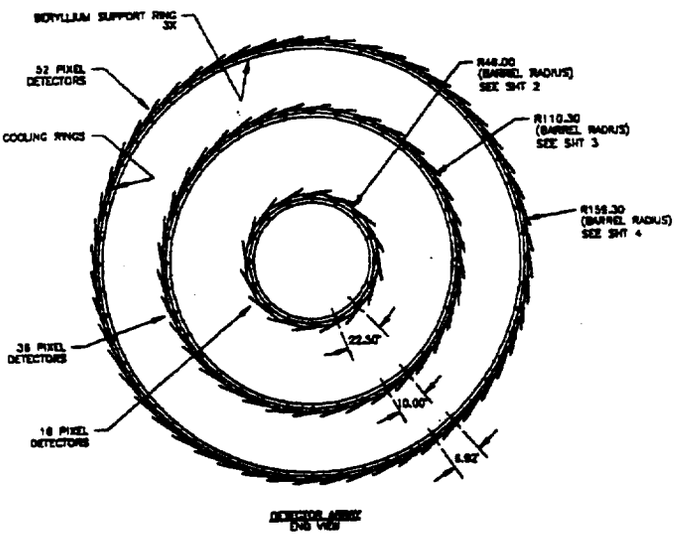

Figure 35: End view of three layers at radii of about 5, 11 and 16 cm

At present modules are not overlapped in z leaving an inactive region of approximately 1 mm between modules on a stave. The stave support also provides coolant to the pixel modules. The size of the stave structure is then determined by strength and coolant flow. Staves are attached to a support and coolant supply or return ring at each end to form a layer. Layers are then supported by an end fixture to form the barrel system. A layer of support and coolant tubes with coolant supply rings and intermediate supports is shown in figure 36.

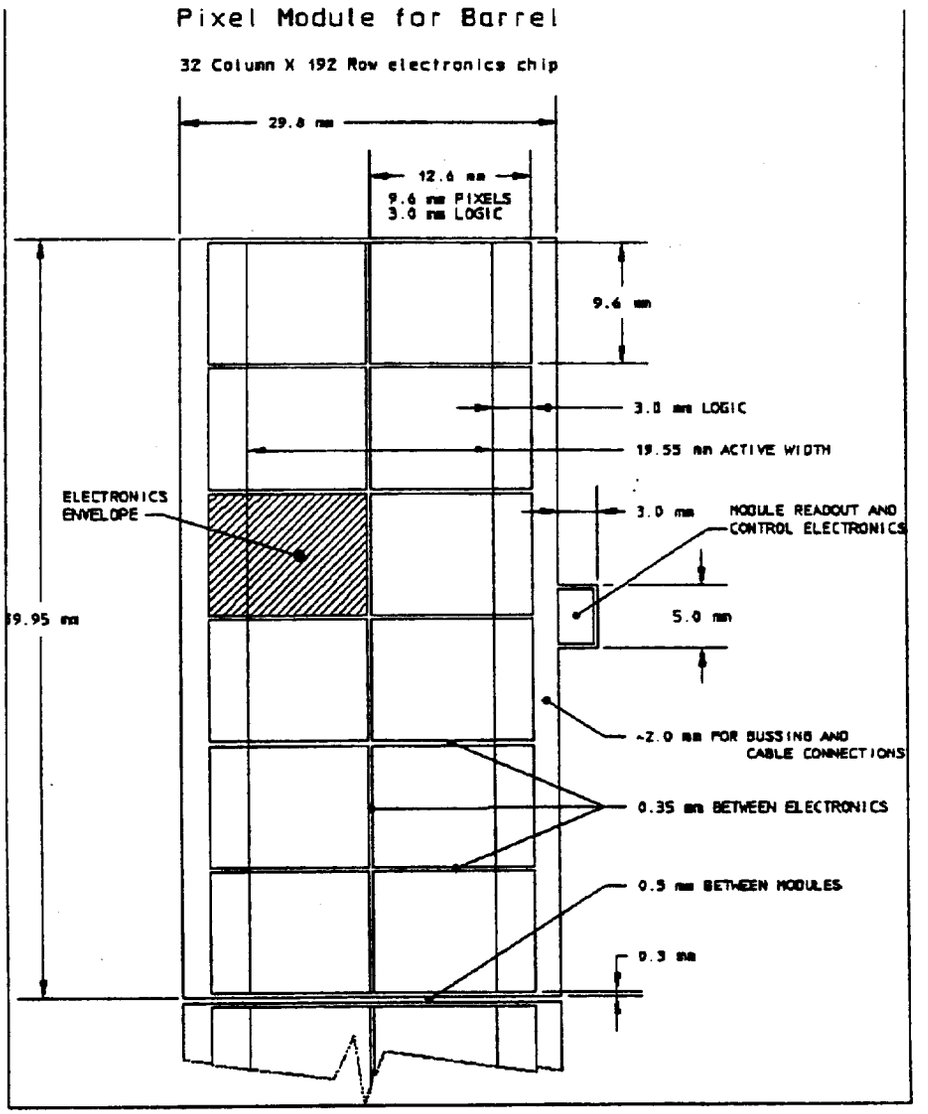

Figure 33: The basic detector unit for the barrel design

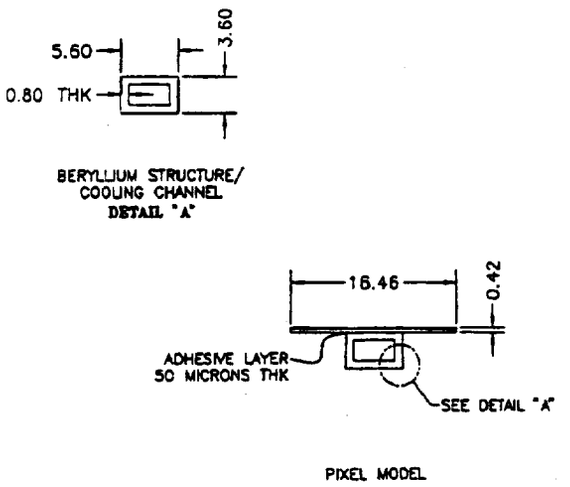

Figure 37: Beryllium structure to support the silicon modules

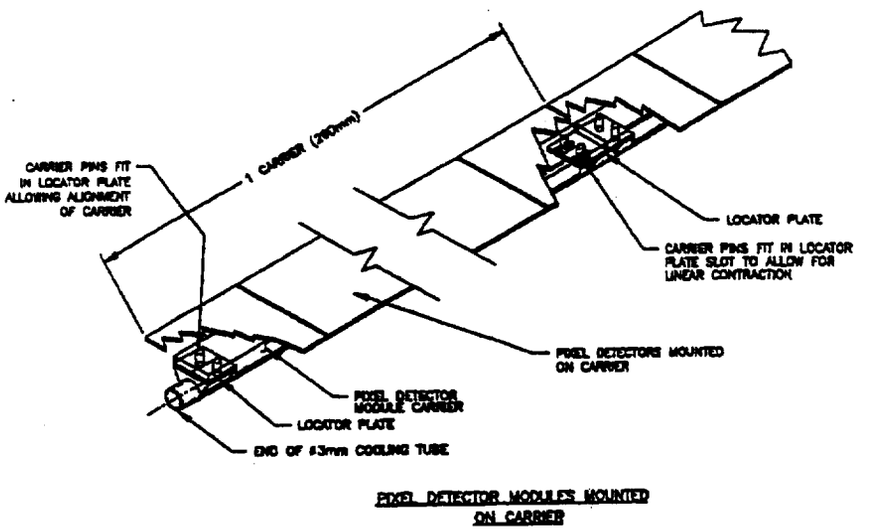

Figure 38: A design in which the silicon is separated from the beryllium cooling channel

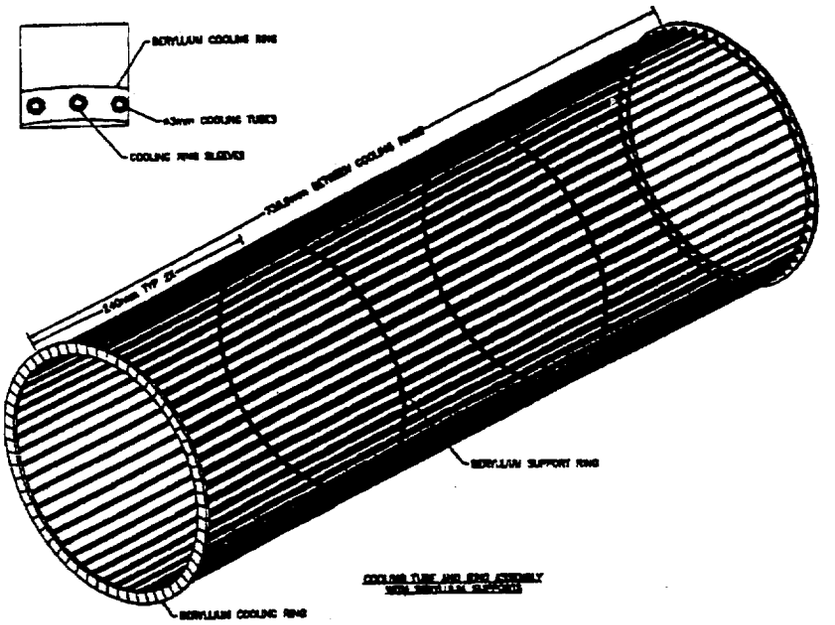

Figure 36: Coolant tubes with coolant supply rings for the barrel pixels

The most vexing problem for stave design is how to handle coefficient of thermal expansion (CTE) differences between silicon and and the stave structural member. Beryllium at present seems to be the best structural material due to its 35 cm radiation length and its high strength, modulus, and good thermal conductivity. However, its CTE is 4.5 times that of silicon. This means there will be bowing of a stave during cool down if the silicon modules are attached directly to a beryllium box support as shown in Fig. 37.

This bowing has been investigated for a stave of 65 cm length with the silicon afixed to the beryllium with a noncompliant adhesive. For fixed stave ends and the dimensions of the beryllium given in Fig. 37, the bowing was 17 microns. If the beryllium wall thickness is reduced from 0.8 mm to 0.5 mm the bowing increases to 29 microns. These deflection are not great; however the condition of fixed ends is difficult to obtain especially when minimal structural material is mandated. If the ends of the stave are free to rotate then the deflection increases to a significant 1.36 mm. Twists of the stave during bowing will be of concern as they are hard to define. Calculations with a compliant epoxy attachment of silicon and beryllium remain to done. A design that separates the silicon from a beryllium cooling channel is shown in Fig. 38.

In this design the silicon is afixed to a carrier of a composite material that more closely matches the CTE of silicon. A carrier subassembly has four or five pixel modules mounted and positioned on it before attachment to a round beryllium cooling tube that is part of a previously fabricated cylindrical structure as shown in Fig. 36. Several carriers are attached to the beryllium tube at locator plates as shown in Fig. 38. The carrier is fixed at one end and can slip longitudinally at the other thus allowing for CTE mismatch. This design has the advantage of separating the pixel module placement from the cooling structure fabrication

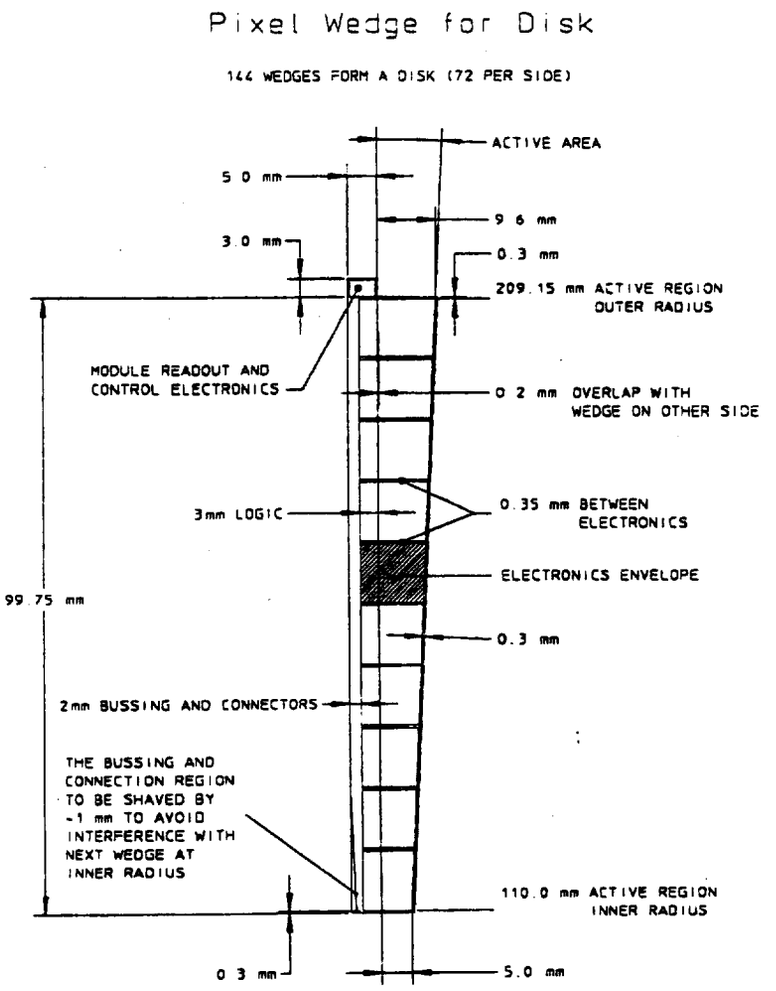

Figure 39: Basic detector unit (wedge) for the disk design

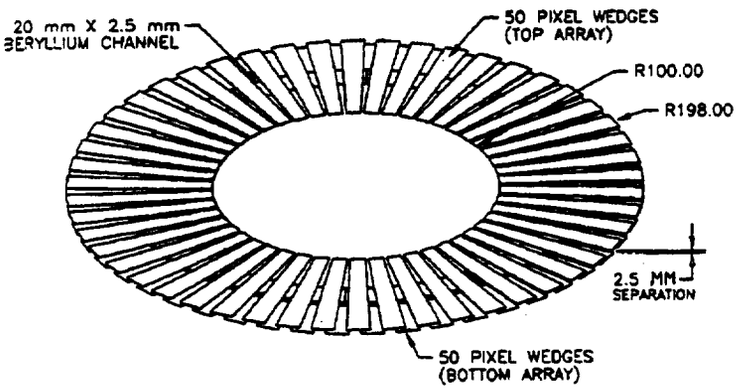

Figure 40: Design concept for a pixel disk

and thus there is no coolant connection to be made when placing the stave in a layer. In the first design either a coolant connection is made when the stave is attached in a layer, which could cause distortions, or the modules must be attached on a completed layer in postage stamp fashion. In the second design, the thermal connection between the silicon and the coolant tube is the critical point to be investigated as heat must traverse a composite carrier and a thermal conductive grease between the coolant tube and the composite carrier. In addtion, the coolant tube and carrier must mate reasonably well. We have at present chosen to pursue the second design with separate mounting of modules on a composite structure.

Finite element analysis (FEA) has been done on stave cross sections to investigate temperature differences, strain, and stress induced by heat removal from the pixel module surface and also due to CTE mismatch upon cool down from room temperature to operating temperature.

The temperature difference between coolant and edge of module is approximately 0.5°C. From module center to module edge the temperature difference is 0.3°C. This 0.3°C temperature difference should also be approximately correct for the carrier stave design; however the temperature difference between coolant and silicon in the carrier design will be greater than in the direct attachment design. For the present greater module width the 0.3°C rise will be slightly greater. This FEA models the bump-bond layer as a continuous layer. An FEA model that uses individual bumps was constucted and gives similar results however it is to complicated to be used for large problems. The deviation of the module edge from flatness relative to center is 1.1 microns due to transverse thermally induced bowing. The maximum Von Mises stresses due to the cool down and operation has been calculated to be 1.1 Kg/mm^2.

This deviation and stress should be less in the case of the carrier design. Thermal, strain, and stress simulations for the carrier design are presently underway.

3.1.2.2 Disk Mechanical System The basic detector unit for the disks is shown in Fig. 39.

Wedges are arranged in overlapping fashion on both sides of a support and cooling structure to form a disk. Table 9 gives the average radiation length thickness of a disk.

Table 9: Average radiation length for a disk layer

Silicon detector including 83% overlap	0.49%
Silicon electronics including 47% overlap	0.16%
Bump bonds	0.01%
Diamond heat spreaders	0.39%
Beryllium channel	0.06%
Coolant	0.05%
Cabling	0.05%
Total	**1.21%**

Figure 40 shows a concept for a pixel disk.

A beryllium coolant and support ring is midway between inner and outer disk radii.

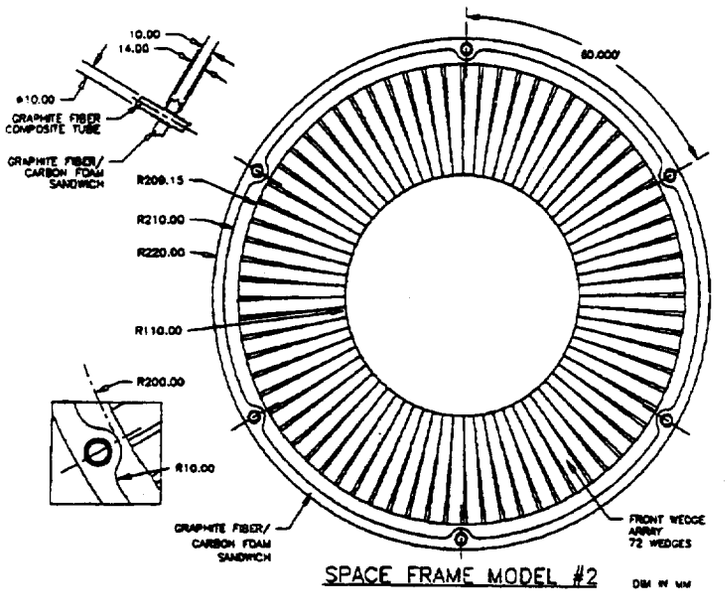

Figure 42: Disk with supporting frame

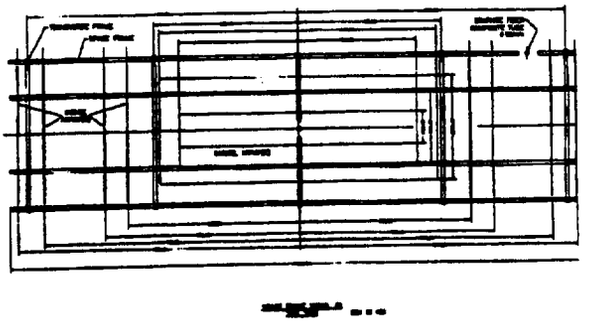

Figure 43: Sketch of a space frame to support the pixel system