A Specification of the Silicon Strip Detectors for ATLAS SCT

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Abstract

Considerations on the silicon strip detectors to be used in the ATLAS semiconductor tracker are presented. Critical radiation damages on the silicon bulk and on the surface oxide are reviewed and preferred choices of technology are listed. Practical parameters, such as size of the detectors, are discussed. The results are summarized in the tables, which items and values are to be taken as a specification of the final detector.

1. Introduction

Based on our knowledge and technologies established for the radiation-hard silicon strip detector, we would like to propose a specification of the silicon strip detector for the ATLAS Semiconductor Tracker (SCT). In the following, we will discuss the radiation environment and the considerations on the detector in general in the section 2, the major detector parameters in the section 3, and, finally, the dimensions of the detectors in the section 4.

2. General remarks

2.1 Radiation level

At a radius of 30 cm, over 3 years of operation with a luminosity of 1×10^{33} cm^{-2}s^{-1} and 7 years with 1×10^{34} cm^{-2}s^{-1} afterward, a charged particle fluence of $1.0\text{x}10^{14}$ particles/cm^2 in total is expected (corresponding to 27 kGy of absorbed dose in Si) [1]. This fluence is counted by the 1 MeV neutron equivalent flux using the non-ionizing energy loss hypothesis (NIEL). Several hundred MeV protons have about 40% higher damage than the 1 MeV neutron: 1.43 (1 MeV n/cm^2) = 1 (500 MeV p/cm^2) [2]. This difference requires some care in comparing a particular result of the proton damage to a prediction.

2.2 Depletion voltage

With the fluence of $1.0\text{x}10^{14}$ particles/cm^2, the resistivity of the silicon will decrease according to the generation of effective acceptor states by traversing particles, and thus, the reverse-bias voltage to deplete the full thickness of the silicon bulk will increase. A part of the initial effective acceptor states will disappear in time (i.e., annealing); a part of

the initial effective acceptors is permanently stable; and, there is a component in the effective acceptor states which increases in time (i.e., anti- or reverse-annealing) [3, 4].

The time constants of the annealing and the anti-annealing are found to be very temperature dependent. When the detector is operated and kept at 0 °C, the detector is predicted to require a full depletion voltage of 146 V (H. Ziock et al.) or 156 V (E. Fretwurst et al.) for a 300 μm silicon thickness. We have irradiated four detectors with 500 MeV protons at a fluence of $0.56\text{x}10^{14}$ /cm^2 and kept them at 0 °C. We have tracked the full depletion voltage and measured it to be around 70 V at one year after irradiation [5]. When extrapolated linearly with the fluence, it may give a depletion voltage of 130V or less at $1.0\text{x}10^{14}$ particles/cm^2. Although the coincidence of the three numbers is plausibly well, confirmation must be required for the depletion voltage of the real detector (to be used in the ATLAS SCT) at the fluence.

Although the time constants of the annealing and the anti-annealing are temperature dependent, because of the competition of the two processes, there is a temperature minimum at -7 °C in the operation temperature (Fig. 1). The valley of the temperature minimum is rather shallow as seen in the figure. The implication of the shallow valley is the wide tolerance on the detector temperature; ΔT~ 10 °C (i.e., -12 ~ -2 °C) can be allowed practically for a depletion voltage variation of 10 V.

2.3 p-n junction breakdown with reversed bias voltage

SDC prototype double-sided silicon strip detectors [6] can hold the bias voltage up to 300 V without introducing an excess leakage current. The leakage currents were measured up to 200 V for samples before irradiation (Fig. 2) and, up to 300 V for a type-inverted sample after an irradiation of about 1×10^{14} protons/cm^2 (Fig. 3). The detector guard structure is the standard of Hamamatsu Photonics (single guard ring (see the section 3.6.2)).

2.4 Single-sided vs. Double-sided

Using a double-sided detector provides advantages of: reducing material (0.3% $X_o \times$ 4 layers = 1.2% X_o); built-in alignment of axial and stereo sides (within 5 μm being established at Hamamatsu). Disadvantages are: requirement for full depletion of the bulk to make the ohmic side work; potentially higher cost.

Using a single-sided detector reverses the advantages and the disadvantages of the double-sided detector. However, the cost for alignment of the axial and the stereo detectors should be properly evaluated and included. In the case of back-to-back gluing, one must also include the cost of careful handling of the detectors in the gluing process. Also, one needs to evaluate the stress to the detector being caused by hardening of the glue by irradiation and to find a method to provide a potential to the middle plane.

Considering the expected bias potential of below 200 V, even including over-depletion, there is no fundamental limitation to use either type of detectors.

2.5 AC coupling vs. DC coupling

The AC coupling detector avoids the large leakage current flowing into the amplifier (estimated to be 2μA/strip at maximum), easing the design of the amplifier, and at the end, giving a better amplifier performance in noise, a better material budget, etc. DC coupling forces to use a single-sided detector or a double-side detector with amplifier floating. The AC coupling design has obvious advantages.

Concern of the AC coupling is the breakdown and/or the reliability of the (integrated) AC coupling capacitors. The fatal breakdown voltage of the double layer of SiO_2 (2000 A) and Si_3N_4 (500 A) is measured to be more than 200 V (Fig. 4). Yield of the AC coupling is being improved. DELPHI double-sided detectors (double layer of SiO_2 and Si_3N_4) are achieving less than 1% loss in production [7].

Even though the loss is less than 1%, there would be a shorted coupling capacitor. The shorts can be detected in the initial burn-in phase and can be detached from the amplifier (by mechanically de-bonding or by burning out a trace by laser).

2.6 Interface fixed oxide charge

Silicon strip detectors are processed to have a so-called passivation layer of SiO_2 to protect the surface. In case of an AC coupling detector, the coupling layer over the implant strip is also made of SiO_2 (sometimes together with other material such as Si_3N_4). It is known that the ionization radiation creates a positively ionized oxide layer at the interface between these SiO_2 layers and the bulk of silicon (which is called as the interface fixed oxide charge). The charge density of the interface starts to saturate at a value of about 2×10^{12} e/cm^2 around a dose of 2 kGy (corresponding to the fluence of 0.7×10^{13} p/cm^2)[8].

2.7 Micro discharge at strip edge

Micro-discharge at the strip edge is caused when the electric field along the strip edge is stronger than that of the avalanche breakdown of the silicon (about 30V/μm). The strong field is generated by three factors: (1) the reverse-bias voltage applied to deplete the silicon bulk (potentially severer at the p-n junction side), (2) the voltage difference between implant strip and the readout electrode in the case of AC coupling, and (3) the electric field generated by the accumulated interface positive oxide charge.

In the factor (2), one has a choice to have a full (or faction) of bias voltage difference on the AC coupling by grounding the AC electrode (with grounded amplifiers) or null difference by floating the amplifiers. In the case of having a voltage difference, the field concentration can be mitigated by designing the AC electrode narrower than the implant strip. The SDC DSSD is designed to have a width of 12 μm of the implant and a width of 6 μm of the AC electrode [9]; it has achieved the discharge starting voltage of more than 150 V (Fig. 4 (a) p-side, (b) n-side). This is before irradiation.

The effect of the interface oxide charge is being vigorously investigated by irradiating γ's in Japan. After accumulating radiation, the factor (3) is found to have a large effect [10]. A preliminary result is that the effect of the trapped oxide charge dominates over the effect of the potential difference on the AC coupling. Grounding or floating the amplifier may make no difference. This might be true for the DC coupling detector, too, because it also has a SiO_2 passivation over the surface. To ease the micro discharge even in the oxide charge accumulation, one needs to improve the implant-strip edge itself not to make the electric field concentrate. We are making an attempt to have the doping level of the implant denser and the depth of the implant deeper, etc.

3. Detector Parameters

We will discuss specific parameters of the detector in the following. The parameters are summarized in Table I and III as a spec in addition to miscellaneous columns. Table II gives the SDC DSSD spec for a reference.

3.1 Initial leakage current

To assure the quality of a detector, one can use the (initial) leakage current as an indicator of the fabrication process. The leakage current is less than 10 nA/cm^2 for a good sample (with a 300 μm thickness) in experience. Tolerance would be 1 μA/cm^2 and 40 μA/detector in case of a 6 cm × 6cm detector.

For a strip detector, it would be also better to specify the (initial) leakage current per strip to assure the strip quality. From the 1 μA/cm^2 tolerance, one would specify, e.g., 60 nA/strip for 100 μm pitch of 6 cm detector.

3.2 Bias resistor

3.2.1 Resistance value

Unlike the previous experiments, e.g., in LEP, the ATLAS silicon strip detectors will experience a large bulk damage in silicon, which leads to a large leakage current through the bulk and the maximum is set about 2μA/strip (at 200 V bias) at the fluence of 10^{14} p/cm^2. This leakage current induces a voltage drop in the bias feeding resistance. It would be better to have a smaller voltage drop in the resistor (e.g., extra heat generation). To limit the voltage drop within a reasonable value, e.g., 2 V, the bias resistance should be less than 1 MΩ.

The bias resistance generates an equivalent-noise-charge of the preamplifier of

$$ENC \propto \sqrt{4kT\tau_m / R_b}\,. \qquad (1)$$

The ENC is 250 electron for R_b=1 MΩ and τ_m=100 ns, which is reasonable compared with the input transistor noise of the amplifier of more than 1,000 electron. A faster shaping provides a room to reduce the resistance for the equal amount of the noise, e.g. R_b=250 kΩ for τ_m=25 ns.

3.2.2 Type of the bias resistor

We have studied two different types of bias feeding method [11]: (1) punch-through gap on a junction side and an accumulation layer resistance on an ohmic contact side; (2) Polycrystalline silicon resistors on both sides. Before irradiation both types worked well as characterized to have stable depletion voltage. As the radiation dose of 65 MeV protons accumulated, the voltage drop over the punch-thru/accumulation layer resistance increased, by more than 10 V (at a bias potential of 80 V) at 40 kGy, possibly due to the effect of the oxide charge. The polysilicon resistance was stable and the increase of the voltage drop was about 50 mV.

FOXFET (-"reach-through") scheme is a variation of the punch-through method [12]. The scheme needs to prove the radiation hardness against the oxide charge accumulation. Because of the stability of the resistance and simplicity in operation, we would prefer the polysilicon resistor.

3.3 Single-sided Silicon Strip Detector

3.3.1 Type of bulk and type of implant strip

Due to the creation of effective acceptor states in the bulk by radiation, the n-type bulk will transmute into p-type around a fluence of 2×10^{13} p/cm^2. This type inversion means that the p-n junction will move from one side to the other. The n-bulk detector requires a fabrication process so that the p-n junction in the other side works reliably after type-inversion.

The n-bulk/p-implant detector requires a care on the backside so that it can be the p-n junction after type-inversion, and also requires full depletion to isolate the p-implant strips in the (type-inverted) p-bulk. The p-bulk/n-implant detector will not invert and does not require full depletion to isolate the n-strips. The n-bulk/n-implant detector will become the p-type/n-implant detector. However, this n-bulk/n-implant detector requires the p-n junction in the backside in the initial fabrication which is essentially a double-sided processing; the cost of this detector is high. A pair of this single-sided detector is more costlier than one double-sided detector [4]. We would prefer the p-type bulk for the single-sided detector. Since the p-type bulk is not the industry standard, it might be costlier than the n-type detector.

The bulk resistivity is naturally high due to the slower mobility of the majority carrier. The initial resistivity would be required to be more than 14 kΩ-cm to give a full depletion voltage of less than 70 V. Little knowledge is gained for the bulk damage of the p-bulk. If the removal of the initial acceptor level will not occur, then the created effective acceptor level would pile up over the initial acceptor linearly, and the full depletion voltage may become more than 200 V. We need to confirm the full depletion voltage to the expected fluence of 10^{14} particles/cm^2.

3.3.2 Implant type of the silicon strip

We would prefer n-type.

3.3.3 Isolation of p-n junction side

Accumulation of the (interface) positive oxide charges in the SiO_2 AC coupling/passivation layer will help to deplete the region between the n-strips by expelling the majority carrier of holes in the p-bulk. However, the same fixed oxide charges may create a thin accumulation layer of electrons very near the surface, making a thin layer of effective n-type bulk and, thus, decreasing the isolation of the n-strips. To avoid this thin accumulation layer, a dense implantation of p material near the surface of the silicon is required, e.g., implanting a p^+ blocking line or spraying p^+.

3.4 Double-sided Silicon Strip Detector

3.4.1 Type of the silicon wafer

An n-type bulk is preferred. Since a double-side detector will require the double-side processing, there is no fundamental requirement on the type of the bulk. Since the n-bulk silicon wafer is the industry standard, it would be less costly.

3.4.2 Isolation of p-n junction side

The initial p-n junction will become a p-p ohmic contact after the type inversion of the bulk. Meanwhile, there is the accumulation of the (interface) fixed oxide charge in the SiO_2 AC coupling/passivation layer This fixed oxide charge will help to deplete the region between the p-strips, and, since the implanted strip is p-type, the possible thin electron-accumulation layer of effective n-bulk will form a p-n junction and will not degrade the isolation. No special structure is required in this side.

3.4.3 Isolation of n-side (Ohmic-contact side)

To isolate the n-strips (in the n-bulk) a structure is required between the n-strips. An MOS-type electrode works to deplete the surface region. As the radiation accumulates, the potential to the MOS-type electrode increases steeply, up to 20V for a dose of 10 kGy to compensate the effect of the accumulated oxide charge [13]. A variation of this method is having the AC electrode wider than the implant so that the potential of the AC electrode works as the MOS electrode. This wider electrode will generate a noise by the micro-discharge at the strip edge, if the potential difference is put on the AC coupling, or even if no potential difference but with the accumulated fixed oxide charges.

Another way to isolate the n-strips is to implant a p-type layer between them, implanting a p^+ blocking line (or spraying p^+). The required implantation density is obtained experimentally. Since the charge density of the interface oxide charge is large, although saturating around 2×10^{12} e/cm^2, the density of p^+ implantation is required to be as large as 1×10^{14} borons/cm^2; otherwise the possible electron-accumulation layer by the oxide charge degrades the n-strip isolation [14]. This p^+-blocking-line and the density are still required after the type-inversion since the effective acceptor density after the fluence of 10^{14} particle/cm^2 is still order of 10^9 e/cm^2 (1 μm thickness of the volume density of 10^{13} e/cm^2), which is much smaller than the oxide charge density of 10^{12} e/cm^2.

The p^+ method is simple, straight-forward, and care-free over the MOS method. The effect of p^+ spraying of this density over the implant strip is unknown (at least for the authors). We would prefer the p^+ blocking line for the isolation of the n-strips.

3.5. Silicon Wafer thickness

The full depletion voltage of the silicon detector is proportional to the square of the depletion thickness. A 250 μm thickness detector still gives enough electron-hole pairs [15], and is clearly preferable. However, the 300 μm thickness is the industry standard for the 4-inch wafer. Also, a concern on cracking the 250 μm wafer during the semiconductor processing is expressed by a manufacturer. We would require a pre-production of enough quantity to learn the yield of the 250 μm thick detector.

3.6. Distance from the active region to the dicing line center

3.6.1 Dicing width

Industry standard (for IC chip production) is not the full-thickness cutting: sawing half-depth and cracking. This introduces large chip on the rim. Hamamatsu rule (of the silicon detector) is the full-cutting. The product is proved to have a very clean cutting surface and very small chip on the rim. The cutout width is 60 μm. The edge of the real detector is 30 μm narrower than the dicing line center.

We have measured 20 cut-samples (6 cm×3.4 cm) and the error of the size is <3 μm (one standard deviation). Thus, a (achievable) tolerance would be 4~5 sigma's, i.e., ±12~15 μm.

3.6.2 Width of edge inactive region

Hamamatsu detector has an inactive region around the edge (Fig. 5). The region is made of the bias ring, the guard ring (20 μm width underneath the bias ring), clear space (150 μm width), and a metal band (350 μm width). The edge of the implant strip is 100 μm away from the outer edge of the bias ring. In total, a width of 600 μm of the edge inactive region is surrounding the active strip area. With this design the SDC DSSD holds a bias potential of more than 300 V.

4. Overall dimension of a detector

4.1 Maximum area

The most cost effective way of using a silicon wafer is to use the maximum area out of a wafer. There is a "stay-clear" region around the edge of the wafer where the process quality is getting worse. The general rule is to have a 5 mm of stay-clear in the 4-inch (10.0 cm diameter) wafer. The usable diameter is, then, D=90 mm. The relation between the length (L) and the width (W) of a rectangular detector is

$$W = \sqrt{D^2 - L^2} \quad (2)$$

The maximum usage is to have a square (W=L=63.6 mm) or nearly square shape (e.g., L=60 mm, W=67 mm) (Fig. 6).

4.2 Length

For a small-stereo angle detector, when two detectors are bonded in length wise to form a longer detector, the length of the single detector is quantized. The imposed assumptions are:

(1) A stereo strip of one detector is a geometrical continuation of the stereo strip of the other detector (when electrically bonded). Since two detectors are identical, the two strips are repetition (n times) of the stereo strips (Fig. 7).

(2) The pitch of the bonding pads (to readout chips) is set identical for the axial strips and the stereo strips. The justification for this assumption is to use the identical hybrid and the identical bonding method for both axial and stereo detectors. With this assumption, the pitch of the stereo strips (p_s; measured normal to the strip) becomes slightly smaller than that of the axial strips (p_a) by cosΨ, where Ψ is the stereo angle, i.e., $p_s = p_a \cos\Psi$.

With these two assumptions, the relation on the pitch p (of the axial strip, i.e., p_a) and the length L is

$$np = L \sin \Psi, \quad (3)$$

then,

$$L = \frac{np}{\sin \Psi}. \quad (4)$$

For a stereo angle of 40 mrad and an (axial strip) pitch of 50 μm, the length L is quantized to 5n (mm), i.e., 55, 60, 65 mm. For a pitch of 75 μm, the length is 3.75n (mm), i.e., 56.25, 60, 63.75 mm. Although quantized, there is infinite number of choices for the length, e.g., slightly different choice of the stereo angle gives slightly different length. Among the infinite choices, a length of 60 mm looks very reasonable for the numbers such as the pitch of 50 or 75 μm and the stereo angle of 40 mrad.

The length L is of the ideal detector with ideal strips. With the requirement for a space for dicing and edge structures, the (ideal) detector length should be kept at L; the actual detector is smaller by the dicing cutout (60 µm) and actual strip length is shortened by the space required for the edge structures. When two detectors are butt-glued, the ideal detectors (length L) are to be glued with no gap. In the real life, the dicing cut-out (60 µm) is just perfect for filling the glue (Fig. 8).

4.3 Width

4.3.1 Width of the axial strip detector

Width of the detector is primarily determined by the number of readout strips. A readout chip may have a 128 readout channels, and the total readout region is a multiple of 128 channels. Besides the readout region, the detector needs to include the field shaping regions and the edge inactive region. Hamamatsu rule is to have a 300 µm for the field shaping and a 600 µm for the edge inactive region, in total of 900 µm per side. With a strip pitch (p) and a multiple of 128 ch chips (n), the total width of the detector (W) is

$$W = 128np + 1.8 \text{ (mm)} \qquad (5)$$

For a 50 (100) µm pitch and with n=10(5) chips, the readout region is 64.0 mm and the total width is W=65.8 mm. For a 75 µm pitch and n=6 (7), the readout area is 57.6 (67.2) mm and the total width is 59.4 (69) mm. The 7-chip 75 µm-pitch design is out of the maximum available width of 67 mm.

4.3.2. Concepts for the stereo strip detector

There are two ways to make the stereo strips: skew the whole axial detector by the stereo angle (=rotating solution); skew the stereo strip pattern by the stereo angle in a rectangular detector (=stereo detector solution). In the case of double-sided detectors, the latter choice is the only available one. For the back-to-back gluing of two single-sided detectors, those two choices are available. After the consideration discussed below, with the readout electronics placed in the center of the 12 cm detector (2 x 6 cm), the rotating solution gives the same dead area as the stereo detector solution for the ϕ and z overlapping. Considering the awkwardness of the edge pattern of the rotating solution, we would prefer the stereo detector solution. The incremental cost for making another set of mask for the stereo pattern would be negligibly small for the production of 18 m^2 of silicon detectors.

4.3.3 Width of the stereo strip detector

Case (1): Electronics at the end of the 12 cm detector - Because of the stereo angle, the stereo strip side requires an offset of $L\tan\Psi$. For a 12 cm detector and a stereo angle of Ψ=40 mrad, the offset is 4.8 mm (Fig. 9). The triangular regions, which has no readout connection, still works as the field shaping. Thus, no field shaping region is required. Adding the offset of W_{off}=4.8 mm and the edge inactive region of W_{edge}=1.2 mm, the stereo side requires an extra width of 6.0 mm. Adding the extra width to the readout

region, the width becomes 70.0 (63.6) mm for the 50 (75) µm pitch. The 50 µm pitch detector exceeds the maximum available width of 67 mm by 3.0 mm. One can limit the width to 67 mm by reducing the (full-length) readout region to 61.0 mm.

Case (2): Electronics at the center of the 12 cm detector - In this case, the offset is reduced to that of 6 cm detector and is W_{off}=2.4 mm (Fig. 10). However, since the readout region is reaching the side-edge, we don't need to add the extra region corresponding to the offset of 2.4 mm, but we do need the field shaping region of 300 µm. Thus, W_{edge}=1.8 mm. The total width is equal to that of the axial side: 65.8 (59.4) mm for the 50 (75) µm pitch.

Case (3): Extra fan-in connection - In case we have an extra fan-in connection, we can map the strips even in the triangular region to the electronics (Fig. 11). Full stereo detector strips are read out, i.e., W_{off}=0 mm. Since we need to read out the extra region, we have options either putting more readout electronics or reduce the number of strips, i.e., widening the strip pitch. Widening the strip pitch might be a practical choice, but we will loose the advantage of using the same readout hybrid on the axial and the stereo sides; we need full-width fan-in connection. Also, we need to re-define the detector length and/or the stereo angle. The extra width is for field shaping and for the inactive region. Thus, W_{edge}=1.8 mm, and the total width is the same as the axial side.

4.3.4 Overlapping the detectors in ϕ and z

Stereo-detector-solution - To have a continuous coverage in ϕ direction (and in z direction), adjacent detectors are to be overlapped. Since the stereo detector is the wider one, we will discuss the overlap of this detector. We require to overlap the width of the triangular region (W_{off}) and the edge inactive space (W_{edge}). In addition, we require to overlap 2.5 strips per one side. Then, the total overlap width becomes

$$W_{\phi}=W_{off}+W_{edge}+5\times p. \tag{6}$$

The widths for each case of the section 4.3.2 is listed in Table III. The overlap width is 7.0 (7.9)% to the readout region for the readout pitch of 50 (75) µm for the case (2): electronics at center.

In the z direction, since the edge of the detector is rectangle, the required overlap is the sum of the edge inactive region and the similar sensitive space corresponding to the 2.5 strips:

$$W_{z}=W_{inactive}+5\times p = 1.2\text{ mm} + 5\times p. \tag{7}$$

Rotating-solution - When making the stereo side by rotating the axial detector, the offset is null in the ϕ direction, and thus, the ϕ overlap can be minimum (Fig. 12). However, when we look at the z direction, there is an offset of $W_{off}=W\tan\Psi$, which is typically 2.4 mm (assuming a typical width of W=60 mm). Since the detectors are aligned in ϕ, we need the similar overlap quantity as in the eq. (6) to overlap the corners. The overlap width is

$$W_{z}=W_{off}+W_{edge}+5\times p. \tag{8}$$

The rotating solution will help in the ϕ direction but require the overlap in the z direction more; No improvement over the case (2).

4.3.5 Double-metal design of the stereo strips

If the disappearing strips out of a side can be folded to the appearing strips in the other side, there is no requirement for the extra width (Fig. 13). The stereo-side width can be as same as that of the axial-side. Although a fraction of stereo strips covers two regions geometrically, they will not give two-dimensional confusion (for the stereo angle of 40 mrad and a detector length of 12 cm) because no axial strip crosses the folded stereo strip in two points. This folding can be done by external connection, e.g., double-metal layer which is the least labor intensive for the connection (although the process intensive).

Incremental capacitance of the folded stereo strips - The double-metal layer usually increases the total detector capacitance due to the extra interstrip capacitance of the extra traces, along with the cross-over capacitance. Since the extra connecting traces are placed very sparsely (d=pitch/tanΨ: 1.25 mm for a pitch of 50 µm), the incremental interstrip

capacitance is expected to be small. The interstrip capacitance (per unit length) is approximately given by

$$C=\frac{\pi\varepsilon}{\log(d/a)} \tag{9}$$

and the incremental capacitance (for a width of the trace of a=10 µm) is

$$C^{'}/C=\frac{\log(p/a)}{\log(d/a)}=33\ \%. \tag{10}$$

Using a typical 1 pF/cm capacitance (dominated by the interstrip capacitance), the 12 cm strip has a total capacitance of 12 pF, and the incremental capacitance would be 4 pF.

The additional cross-over capacitance (n=600~1300 cross-overs, insulator thickness of g=5 µm, $\varepsilon=4\varepsilon_o$ (SiO_2)) is estimated as

$$C\approx 4n\frac{\varepsilon a^2}{g}=1.7\text{~}3.7\text{ pF}. \tag{11}$$

Total incremental is 6~8 pF, i.e., 48~67 % increase; the total strip capacitance would be 18~20 pF.

4.4 Tilt angle of the detectors

There are two ways to overlap the adjacent detectors in r-ϕ direction: (1) No tilting and changing the radius of the detectors; (2) tilting the detectors and keeping the median of the detector radius constant. There is a good point in tilting the detectors besides making overlap, i.e., improving the spatial resolution by creating the charge sharing region.

The maximum charge sharing is achieved by making the charge carriers spread over between two strips. Without a magnetic field, the swath of the carrier (Δ_o) at a tilt angle (χ) is

$$\Delta_o=d\tan\chi \tag{12}$$

where d is the thickness of the detector (d=300 µm). Equating the swath to the strip pitch (p) gives the tilt angle of 9.5° (p=50 µm), or 14.0° (p=75 µm). A magnetic field deflects the carrier and change the relation.

In the case of single-sided detector, only one type of bulk, i.e., one type of charge carrier, can be chosen. We take p-bulk and electrons. The deflection distance of the furthest carrier is

$$\Delta^{-}=\mu_B{}^e Bd. \tag{13}$$

Since the Hall mobility of electrons is large, μ_B^e=1391 cm^{2}V^{-1}s^{-1}[16], the deflection is also large, 83.5 μm, at B=2 Tesla. A tilt angle is required to compensate the deflection so that the corrected swath to become the pitch as

$$p=\Delta=\Delta^{-}-\Delta_o \quad (14)$$

and,

$$\chi=\tan^{-1}((\mu_B^e Bd - p)/d). \quad (15)$$

The tilt angle is 6.4° (p=50 μm) or 1.6° (p=75 μm).

In the case of double-sided detector, there are two types of charge carrier, i.e., electrons and holes. Instead of making the swath to equal the pitch, we need to choose the swath of electrons and the swath of holes to be equal to balance the both resolutions, i.e.,

$$\Delta^{+}+\Delta_o = \Delta^{-}-\Delta_o\ . \quad (16)$$

From the relation, the tilt angle becomes

$$\chi=\tan^{-1}((\mu_B^e-\mu_B^h)B/2) \quad (17)$$

which is 6.1° using the Hall mobility of holes, μ_B^h=325 cm^{2}V^{-1}s^{-1}[14]. The swath is about 50 μm.

Table I. A specification of the ATLAS silicon strip detector

	Single-sided Comment/Requirement	Double-sided	
Dimension			
Length	60 mm	60 mm	Dicing line center
Width	Table III	Table III	<67 mm
Edge space	0.6 mm	0.6 mm	V_{bias} >300V, Hamamatsu rule
Bulk			
Type	p-type	n-type	at BOL
Resistivity	>14 kΩ-cm	4~8 kΩ-cm	at BOL, V_{dep} <70 V
variance	≤10%	≤10%	
Thickness	250~300 μm	250~300 μm	
variance	<3%	<3%	
Implant strip			
Type	n-type	p-type, n-type	
Density	MD	MD	
	$V_{discharge}$ >80V at EOL		
Depth	MD	MD	
	$V_{discharge}$ >80V at EOL		
Axial pitch (p_a)	Table III	Table III	
Stereo pitch (p_s)	$p_a\cos\Psi$	$p_a\cos\Psi$	Ψ: Stereo angle
Strip width	TBD	TBD	
Isolation of n-strips	p+ blocking line	p+ blocking line	
Resistance	>>R_b	>>R_b	at EOL

Table I cont'd...

Bias resistor			
Resistance (R_b)	250k~1MΩ	250k~1MΩ	for τ_m=25~100ns, at EOL
variance	≤20%	≤20%	
method	Polysilicon	Polysilicon	V_{drop} <2V at EOL
AC coupling & electrode			
Material	$SiO_2+Si_3N_4$	$SiO_2+Si_3N_4$	
$V_{breakdown}$ >150V			
Loss	<1%/detector	<1%/detector	
Capacitance	>10×C_{det}	>10×C_{det}	Charge collection
Electrode	Aluminum	Aluminum	
width	TBD	TBD	Strip-edge discharge
resistance	<30Ω/cm	<30Ω/cm	Signal dispersion
Bonding pad			
Size	50×150 μm^2	50×150 μm^2	
Reinforcement	Required	Required	No breakage with Al-wire bonding
Passivation	SiO_2	SiO_2	Entire detector except the bonding pads
Leakage current			Room temp. at BOL
	<60nA/strip V_{bias}=100V	<60nA/strip	
	<40μA/detector V_{bias}=300V	<40μA/detector	

Note:

The range of value means that a final value will be chosen within the range.
BOL=Beginning of Life (i.e., before irradiated)
EOL=End of life (i.e., 1.0×10^{14} particles/cm^2 and/or 27 kGy of γ's)
MD=Manufacturer dependent, TBD=To be determined

Table II. Example: SDC Double-sided silicon strip detector, a reference

	Double-sided	Comment
Dimension		
Length	60 mm	Dicing line center
Width	34.1 mm	Two from one 10 cm wafer
Edge space	0.6 mm	V_{bias} >300V
Bulk		
Type	n-type	
Resistivity	4~8 kΩ-cm	
variance	≤10%	
Thickness	300 μm	
variance	<3%	
Implant strip		
Type	p-, n-type	
Density	MD	$V_{discharge}$ >80V at EOL
Depth	MD	$V_{discharge}$ >80V at EOL
Axial pitch (p_a)	50 μm	
Stereo pitch (p_s)	$p_a \cos\Psi$	Ψ: 10 mrad
Strip width	12 μm	
Isolation of n-strips	P+ blocking line	1×10^{14} borons/cm^2, 26 μm wide, ~1μm deep
Resistance	>>R_b	at EOL

Table II cont'd ...

Bias resistor		
Resistance (R_b)	250kΩ	for τ_m=20ns
variance	≤20%	
method	Polysilicon	stable till EOL
AC coupling & electrode		
Material	$SiO_2+Si_3N_4$	$V_{breakdown}$ >150V
Loss	<1%/detector	
Capacitance	20 pF/cm	
Electrode	Aluminum	Aluminum
width	6 μm	Grounded amplifier, $V_{discharge}$ >80V
resistance	50Ω/cm	
Bonding pad		
Size	50×150 μm^2	
Reinforcement	Polysilicon	No breakage with Al-wire bonding
Passivation	SiO_2	Entire detector except the bonding pads
Leakage current		
	<100nA/strip	V_{bias}=100V at BOL
	<1μA/detector	V_{bias}=100V at BOL

Note: Expected EOL accumulated radiation level is 1~2×10^{14} charged particles/cm^2.

Table III. Detector dimensions and operation contidions

Pitch(*)	50(100) μm	75 μm	Comment/Requirement
Length	60 mm	60 mm	Dicing line center
Width			<67 mm
Axial	65.8 mm	59.4 mm	
pitch (p_a)	50(100) μm	75 μm	
readout strips	1280(640)	768	Full 12 cm
readout width	64.0 mm	57.6 mm	
field shaping	2×0.3 mm	2×0.3 mm	
edge space	2×0.6 mm	2×0.6 mm	
Stereo	65.8/67/65.8 mm	59.4/63.6/59.4 mm	Elec: Center/End/Fan-out
pitch (p_s)	$p_a\cos\Psi$	$p_a\cos\Psi$	Ψ: Stereo angle = 40 mrad
readout strips	1280(640)	768	
readout width (W_R)	64/61/64 mm	57.6/57.6/57.6 mm	
offset (W_{off})	2.4/4.8/0 mm	2.4/4.8/0 mm	
edge space (W_{edge})	1.8/1.2/1.8 mm	1.8/1.2/1.8 mm	
Overlap fraction (φ) $(W_{off}+W_{edge}+5\times p)/W_R$	7.0/10.3/3.2 %	7.9/11.1/3.8 %	
Best tilt angle			
p-bulk single-sided	6.4°	1.6°	Best resolution for 300μm, B=2Tesla
double-sided	6.1°	6.1°	
Best operation temp.	-12~ -2 °C	-12~ -2 °C	10 V depletion-voltage variation at EOL

(*) 50/100 μm: 50 μm-pitch full readout, or, 50 μm implant and 100 μm charge-divition readout
75 μm: 75 μm-pitch full readout

Figure Captions

Fig. 1 Depletion voltage variation as a function of the operating temperature at an accumulated fluence of 1.0×10^{14} p/cm^2 in 7 years predicted by H. Ziock et al.. A voltage band of 124 to 134 V is overlaid in the figure.

Fig. 2 Leakage current measurement of the two 2nd SDC double-sided prototype detectors. Leakage currents are measured at three temperatures: 0, 10, and 23 °C. The bias voltage was given up to 200 V which was the maximum output of the power supply.

Fig. 3 Leakage current measurement of one of the first SDC double-sided prototype detector which has been irradiated to the protons at a fluence of about 1×10^{14} p/cm^2 and kept at room temp. Leakage current measurement at two temperatures: 0 and 23 °C.

Fig. 4 Noise measurement of the 2nd SDC DSSD prototype detectors: (a) p-n junction side, (b) n ohmic side. The noise increase in the junction side over the bias voltage of 160 V is caused by the micro discharge (see text) and not by the breakdown of the AC coupling capacitor. The AC coupling capacitor holds the voltage difference (in the horizontal axis) up to 200 V.

Fig. 5 Layout of the SDC double-sided detector (axial side)

Fig. 6 Maximum rectangular detector out of a 4-inch wafer.

Fig. 7 Concept for making a larger stereo-strip detector from two identical detectors

Fig. 8 A 12 cm long silicon strip detector made from butt-glued two 6 cm detectors. The detector dimensions, such as the length L, is calculated from the center of dicing line; the real detector is narrower by the width of saw, e.g., 60 µm, which is perfect for filling the glue.

Fig. 9 A 12 cm long stereo detector with a readout electronics at the end of the detector. The right-most readout strip will have an offset of 4.8 mm when reached at the other end. Adjacent detector needs to overlap this offset, in addition to the inactive edge space, to make a continuous coverage (in ϕ).

Fig. 10 A 12 cm long stereo detector with a readout electronics placed at the center of the detector. The right-most strip will have an offset of 2.4 mm. Adjacent detector will overlap this offset, in addition to the inactive edge region, to make a continuous coverage (in ϕ).

Fig. 11 A 12 cm long stereo detector with a readout electronics at side and a fan-in connection. The full area can be covered with a design of the fan-in by reading out the short strips at the corners.

Fig. 12 A 12 cm long stereo detector made by rotating the axial detector. The ϕ overlapping can be minimum, but a large overlapping in z is required.

Fig. 13 A 12 cm long stereo detector - a concept for making a dead-space-less design by connecting the short strips in one side to the short strips in the other side. The connection can be made by either double-metal layer technique or an extra trace on a separate plane, e.g., glass.

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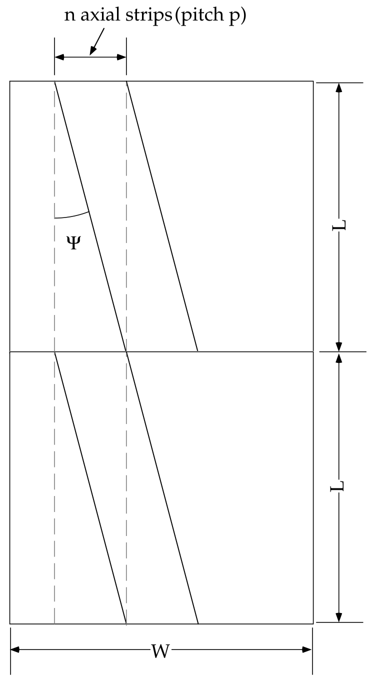
Fig. 2 to Fig. 6 are not available in an electrical form.

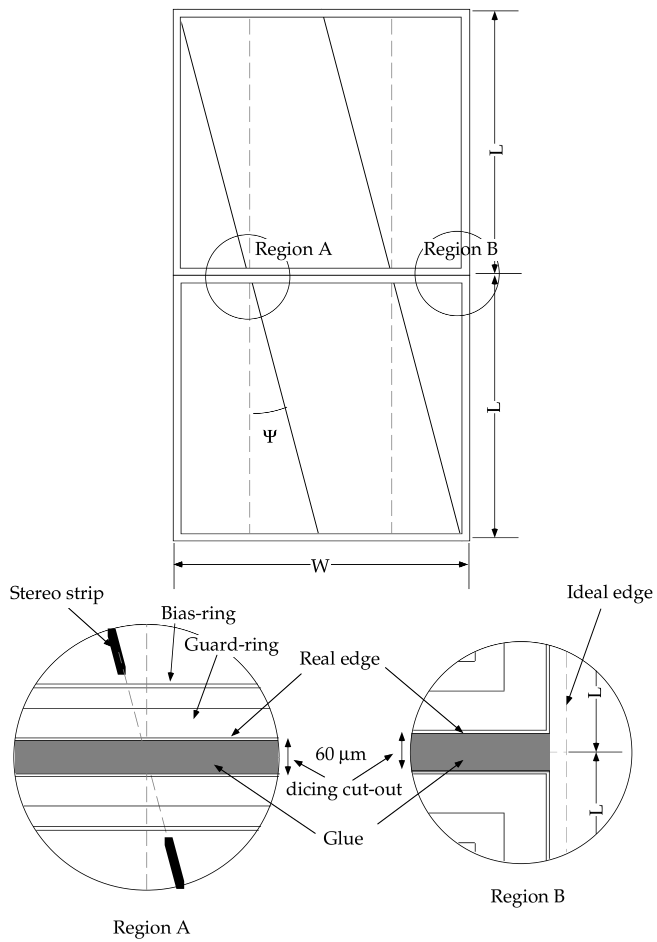


L: Detector length
W: Detector width
Ψ: Stereo angle

$$L = \frac{np}{\sin \Psi}$$

Concept for making a larger stereo-strip detector
from two identical detectors

Fig. 7 Concept for making a larger stereo-strip detector from two identical detectors



A 12 cm long Silicon Strip Detector
made from butt-glued two 6cm detectors

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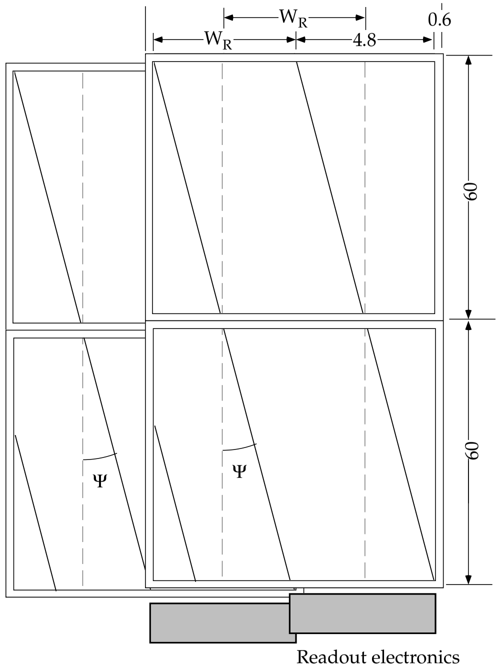

Stereo angle Ψ: 40 mrad

A 12 cm long Silicon Strip Detector
made from butt-glued two 6cm detectors

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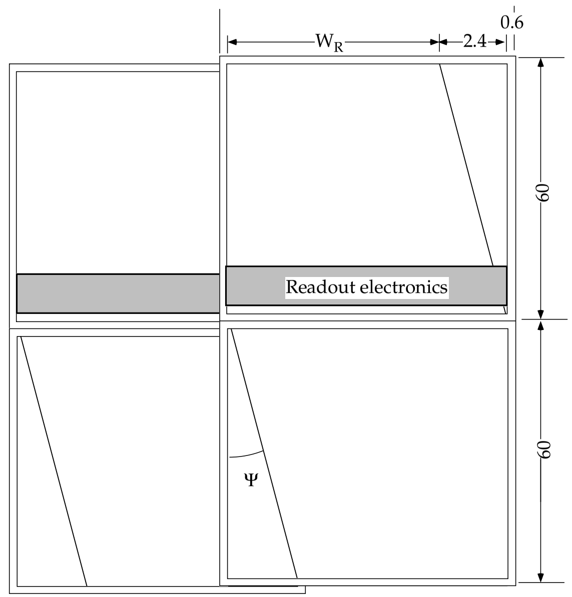

Stereo angle Ψ: 40 mrad

A 12 cm long Silicon Strip Detector
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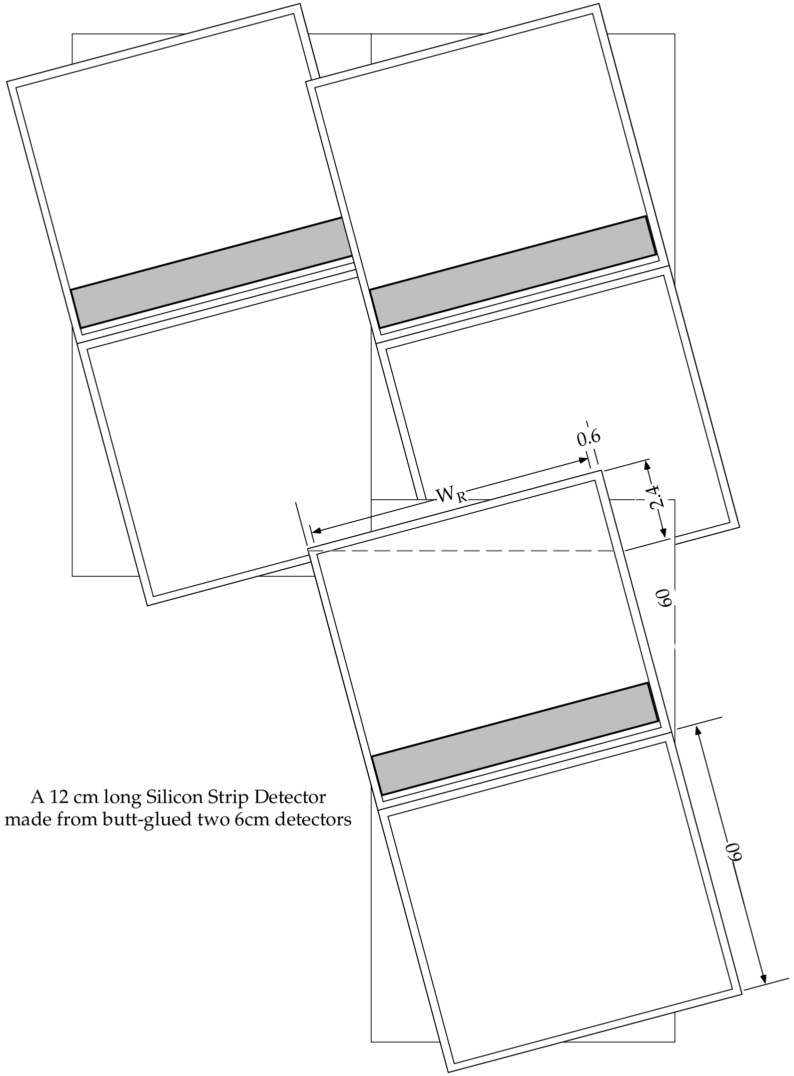

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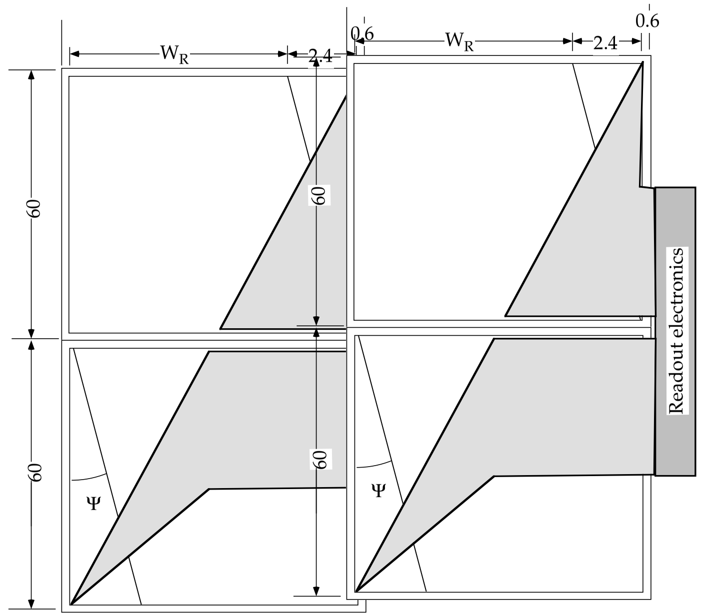

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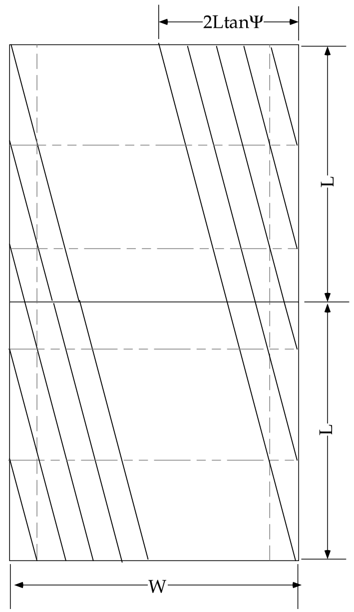

Ψ: stereo angle

Concept for making a dead-space-less stereo-strip detector
by folding the imcoplete stereo strips at edge to the strips in the other side

Fig. 13 A 12 cm long stereo detector - a concept for making a dead-space-less design by connecting the short strips in one side to the short strips in the other side. The connection can be made by either double-metal layer technique or an extra trace on a separate plane, e.g., glass.

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