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The ATLAS Silicon Inner Tracker and Vertex Detector: Design Considerations and Related Technologies

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This report describes the status of the Silicon Inner Tracker and Vertex Detector of the October 1 1992 ATLAS letter of intent. In this report, we review the detector and related technologies.

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1 Introduction.

ATLAS is intended to be a general purpose pp experiment which would be operational at the startup of LHC in order to exploit its full discovery potential. The detector will be optimised for the study of a wide variety of physics studies, including the origin of mass at the electroweak scale, top quark decays, supersymmetry searches and sensitivity to large compositeness scales. Many of the interesting questions at LHC require the full luminosity of 1.7 10^{34} cm^{-2} s^{-1}, but emphasis is also put on the performance necessary for physics accessible during the initial lower luminosity running, including more complex signatures including tau detection and heavy flavour tags.

2 The Required Physics Performance of the ATLAS SITV Detector.

A discussion of the extensive studies made of the physics performance and detector requirements is included in the ATLAS letter of intent [1]. In addition to these studies, a vigorous programme of simulation studies for the SITV has been undertaken, combining the simulation of some benchmark physics processes with several different SITV inner configurations, together with studies of the performance (for example in impact parameter resolution and momentum resolution) of the SITV in combination with other tracking elements including the silicon inner tracker (SIT), and the forward and central TRD's and MSGC's. The effects of pattern recognition on performance for these benchmark processes (for example via fake track rejection at the full LHC luminosity) are also under investigation. For comparison, we review the tracking requirements of the SDC tracker in section 4.

2.1 Impact Parameter and Momentum Resolution

In this section we consider the SITV geometry that will provide optimum momentum resolution and impact parameter resolution for full luminosity LHC operation. Obvious restrictions on the latter come from the position of the innermost layer, due to the expected radiation levels, which are discussed in section 2.1.2 and also later in this report.

2.1.1 Momentum Resolution: Positions of the SITV Tracking and Vertexing Layers.

A radial space of about 110 cm radius is available for tracking inside the ATLAS electromagnetic calorimeter and solenoidal magnet. The ATLAS inner tracker (SITV + larger radius elements at about 1 metre: fig 1) should provide a precise curvature measurement of charged particles in order to:

- distinguish the sign of the charge of electrons up to the highest produced momenta (their energy will be more precisely measured by calorimetry);
- identify electrons from the correspondence between the momentum measured in the tracker and the energy deposited in the calorimeter and from the matching of a track with the centroid of the electromagnetic cluster;

- complement the toroid measurement of muon momentum.

These requirements are essentially satisfied provided a ($\Delta p_T/p_T$) somewhat better than 50% at 1 TeV/c can be achieved, for a sagitta of about 90 μm. References [2, 3] show that with a realistic outer tracking detector at a radius of about 1 metre (with between 40 and 60 μm precision - including alignment errors), and under the assumption of a 20 μm radial uncertainty in beam position, that $\Delta p_T/p_T$ is about 40% for 1 TeV/c tracks when a sagitta-measuring plane with an accuracy of 15 μm (50 μm strips for example) is placed at a radius of between 20 and 50 cm from the beams. Positioning such a detector at 30 cm was considered as a balance between detector positioning errors and minimising the number of channels. It also leads to the attractive possibility of combining vertex and sagitta measurements in the same detector, by extending the track vector inward to r $\leq$ 20 cm. This would enable a precise determination of the beam spot and give an impact parameter tag for heavy flavour physics. In a practical detector, the need for redundancy would dictate double layers of detectors at about 30 cm and 20 cm, which together with the inner vertexing layer, would provide a degree of stand-alone pattern recognition, and self-alignment capability based on track samples. For impact parameter measurement, space point information from the innermost plane would be combined with that from the outer planes for track vector measurement.

In the forward regions of SITV two paired planes of gallium arsenide (GaAs) detectors cover the range ($\eta \geq \pm$ 1.8). These detectors will be in the form of wheels with inner and outer radii of 15 and 25 cm respectively, positioned at z values of 57-70 and 96-109 cm from the interaction point. The z positions of these detector wheels are chosen to provide extra measurement points on forward going tracks that intersect the forward MSGC's at the limits of their forward coverage (r = 40 cm at z = 100 cm and 340 cm respectively). The z positions and radial dimensions of the GaAs detectors are also intended to provide some overlap in rapidity coverage with the forward disks of the SITV detector (fig 2) for alignment purposes.

2.1.2 Impact Parameter Resolution: Position of the Innermost Tracking and Vertexing Layers.

In this section we consider the SITV geometry that will provide adequate impact parameter resolution for full luminosity LHC operation. Obvious restrictions on the position of the innermost layer come from the expected radiation levels, which are discussed in [1, 4, 5], and also later in this report.

In the proposed SITV geometry, discussed in section 5 (fig 2), we have adopted the conservative principle of placing silicon microstrips no closer than at a radius of 20 cm of the beams, where the radiation dose at full luminosity, including the effects of gamma conversions and looping tracks in the 2T magnetic field will be no more than 18 kGy/year (1.8 MRad/year). The layers closer to the beam line will be made of more radiation-hard technology; either silicon pixel detectors or GaAs microstrips. Fig 3 shows the results of simulations of radiation dose and impact parameter resolution (run with Pythia 5.6, Jetset 7.3 and Geant 3.15) for a layer at varying distances from the interaction point. The simulation assumes a beam pipe of 5 cm radius with a thickness of 1.8 mm beryllium (0.5 % X_0) and a vertexing superlayer (two planes) of 2 % X_0: including cooling and mechanical support. At a radius

of about 12 cm the radiation dose would be about 3.5 MRad/year, for an impact parameter resolution of 20-25 μm. For comparison with the typical b impact parameter is 155 μm.

Preliminary results from other studies [6, 7, 8, 9, 12] of impact parameter resolution and momentum resolution with both a stand-alone and combined tracker also indicate that an impact parameter resolution of 25 μm will be achievable.

2.1.3 Simulation of b Jet Tagging for Top Mass Measurement

Top quark mass measurements will form an important part of the standard model physics programme at LHC, and it is anticipated that the mass of the top quark, even if already discovered at FNAL prior to the start-up of LHC, will not be known initially to much better than $\pm$ 10 GeV/c^2 before LHC physics begins.

Reference [7] is a study of b-jet tagging for top mass measurement in hadronic top quark decays: the only channel for which a complete reconstruction of m_t can be performed. Events of the type

$$t\bar{t} \rightarrow W^+W^-b\bar{b} \rightarrow l\nu q\bar{q}b\bar{b} \qquad (l = e \; or \; \mu)$$

were generated for m_t = 130 and 200 GeV/c^2.

It was assumed that t $\rightarrow$ Wb was the dominant process, and that within a $t\bar{t}$ event, one of the W's may decay into a high P_T ($\geq$ 40 GeV/c) lepton and a neutrino - giving a clear signature of an event. At least three reconstructed jets with $P_{T_1} \geq$ 50 GeV/c and $P_{T_{2,3}} \geq$ 40 GeV/c in the hemisphere opposite the lepton were also required, where two of the jets should have an invariant mass close to that the W mass.

It was assumed that the t quark mass could be measured by reconstructing the 3 jet invariant mass in the hemisphere opposite the high p_T lepton, while the combinatorial background could be further reduced by requiring the third jet to be a b jet.

The analysis used a detector geometry similar to ATLAS option "A", consisting of a SITV, combined with an outer (radius 70 to 90 cm) and forward tracker. The SITV had an assumed resolution of 20 μm in (r-ϕ), with detector surfaces at about 10, 20 and 30 cm from the beam, and a total radiation length of about 5% X_o, including the beam pipe. The impact parameter resolution improved from about 200 μm at about 1 GeV/c to a fairly constant value of about 27 μm for track momenta above 10 GeV/c. A jet was tagged as a b jet if it contained at least one associated charged track with $p_T \geq$ 2 GeV/c and an impact parameter greater than 200 μm. This b jet tagging algorithm gave an increase of a factor of 4 - 5 in the signal to background ratio at the top invariant mass peak.

It is expected, that these measurements will be done during initial low luminosity running, in the absence of minimum bias pileup. The results were obtained without taking track finding problems into account. Some preliminary pattern recognition studies done later for these $t\bar{t}$ results are described in section 2.3.3.

2.2 Pseudorapidity Coverage

The rapidity acceptance ($\eta = \pm$ 1.5) of the proposed SITV detector geometry is a compromise between the requirement for maximum physics reach, and the technical difficulty and expense of making a detector with acceptance out to very high rapidities.

In general, the requirement that the microstrip detectors be located in regions of tolerable radiation dose dictates radii $\geq$ 20 cm, and result in a geometry with a long cylindrical part, which can lead to an expensive, large area detector. Also, the increased multiple scattering in the detector layers at higher rapidities degrades the momentum resolution and impact parameter resolution relative to those attainable at lower rapidities [1]. Figure 4 shows the required area of an outer (r = 30 cm) SITV detector as a function of rapidity. It can be seen that the area/rapidity relation is approximately linear at lower rapidities, and that η = $\pm$1.5 is a reasonable cut-off point for the cylindrical part of a SITV geometry. Coverage at higher rapidities are best provided by disk or cone segments.

2.3 Pattern Recognition

2.3.1 General

The studies discussed in this report are for the "Concept A" tracker [1], in which an SITV detector with some stand-alone pattern recognition capability is assumed necessary. In the "concept B" inner tracker with the multiple straw tubes of the TRD, stand-alone pattern recognition capability for the SITV could be less important. Initial pattern recognition studies done until now concern three different physics cases discussed below.

2.3.2 Simulation of Isolated Leptons with Pile-up at High Luminosity

For this study [9], the general ATLAS simulation package named SLUG (Simulation for LHC Using GEANT) was used. Twenty minimum bias events (corresponding to one beam crossing) were read from tape to generate each high luminosity event. The associated detector hits were added on top of the hits from a 100 GeV/c electron produced in the center of a detector at 90°. There were 6 sensitive detector layers, each of 0.6 % X_0 and one passive layer of 1.0% X_0, intended to simulate the support structure.

Hits were projected onto individual detector wafers and the effects of finite single track and two track resolutions were taken into account. In order to start from simpler pattern recognition cases it was assumed that all the detectors are of single sided strips. This should also give a feeling of the performance of the simplest possible 6 layer detector, for a reference. The single wafer length was assumed to be 6 cm, one track (r-ϕ) resolution 20μm and two track resolution 150μm. Experience from LEP experiments shows that the value of (r-ϕ) resolution chosen here already includes a significant safety margin for possible alignment problems. The pattern recognition algorithm was then run on the reconstructed hit positions.

Creation of an ultimate pattern recognition algorithm requires a long period of studies and Monte Carlo tests. In order to obtain preliminary quantitative results, a rather simple approach was chosen. It was assumed that the detector is 100% efficient. A track candidate should have a hit in every layer. It was assumed that the information from detectors at higher radii is sufficient to define a road through the SITV layers containing the hits generated by the high p_T track. For this task the calorimeter information should be sufficient. Possible tracking detectors situated outside SITV could be much more helpful. Until now only stand alone pattern recognition was tried however. The following criteria was used to find the tracks:

1. Hits should belong to a road containing the expected high p_T track. In ϕ the road size was 20°, in z the size was 10 cm at r=30 cm and 25 cm at r=0. This includes the uncertainty on the z position of the primary vertex.

2. For every two neighboring points of a track candidate, the angle α between the line going through points the direction towards the beam spot in (r-ϕ) plane was calculated. The combination was rejected if α was bigger than 10° for any two points.

3. For every set of 6 points fulfilling 1. and 2. the helix fit in space was performed. The χ^2 cut was used to reject fake hit combinations.

Steps 1. and 2. were used in order to reduce the number of combinations to which the helix is fitted. The algorithm is at present very combinatorial. The helix is fitted many times per event and the CPU time needed to analyze one event limits the statistics severely. One should note however, that a high luminosity event has on average 3800 hits in the SITV (in case of rapidity coverage of ±2). It requires a more mature and sophisticated pattern recognition algorithm to reduce the processing time.

250 events were analyzed. The reconstructed tracks having $\chi^2 > 5.0$ were too copious to be stored and were skipped. Numbers of good and fake reconstructed tracks are shown below:

cut	number of tracks	
	good	fake
$\chi^2 < 5.0$	249	135
$\chi^2 < 1.1$	244	18
$\chi^2 < 1.1$ and $\|z\| < 20$ cm	244	9

It was observed that the fake tracks are often inclined in θ and have a reconstructed starting z value different from that of the real tracks (which is 0 μm in the case of our electrons). One could apply an extra cut on the starting z of a reconstructed track to further reduce the number of fakes. This corresponds to the third line in the table above. The efficiency is 98% and the number of fake tracks found is 4%. The observed loss of real tracks is due to hard bremsstrahlung in the detector material. In this case, the track gets a kink and is not seen as a smooth helix. The χ^2 becomes bigger and the simple pattern recognition rejects the track.

No primary vertex spread in z and no variation in the angle of production was taken into account during the electron tape production. All the hits from the electron tracks have $z = 0$. Therefore they lay in the plane of a detector symmetry. In every layer the central wafer is crossed in the middle. Thus the real tracks have no measurement error in z and their χ^2 values are too low on average. If the electrons were produced in a more random way the χ^2 cut would have to be higher and some increase of the background would occur. Further studies are planned.

2.3.3 Pattern Recognition in Jets from $t\bar{t}$ Events

The events used were the selected $t\bar{t}$ ones, described in section 2.1.3. They serve here as an example of interesting jets. The GEANT processing of these events was done recently and some preliminary results for pattern recognition were obtained.

An attempt is made to find all the tracks with $p_T > 1$ GeV/c. Moderate luminosity of 10^{33} cm^{-2}s^{-1} is assumed and no minimum bias background event is added. The jet event itself poses a significant difficulty for pattern recognition, considering that in this case we do not limit the search to a single very high p_T track.

The track finding algorithm is similar to the one discussed in the previous chapter. In this case the regions of interest are defined in the outermost layer only and not across all the 6 layers. For every interesting point in the outer layer a separate track road is then constructed, taking into account a curvature of 1 GeV/c track and a spread of the primary vertex in z. Because there is a larger region of interest in this case much bigger detector volume is analyzed.

An event produces on average 890 hits in a detector. The number of considered hit combinations is so big that even after all the preliminary rejections 67000 of them on average per event pass to the stage of the helix fit. The number of events which were processed is only 70 (due to CPU time limitation), the total number of reconstructed tracks having $\chi^2 < 10.0$ is 2155. Only the central detector region, corresponding to the rapidity coverage of ± 1 was used. Acceptance for real track and percentage of fake tracks among the reconstructed tracks are shown in the following table for some chosen values of χ^2 cut.

χ^2 cut	acceptance [%]	fraction of fake tracks [%]
10.0	94	46
5.0	91	32
2.0	87	20
1.5	83	18
1.0	75	15

In this case the track loss is higher than in 2.3.2. Tracks of lower p_T are more likely to get scattered in the detector material, so they do not pass the χ^2 cut. Also the number of fake tracks indicates that this is a more difficult pattern recognition case. It was checked, that the track loss is not due to overlap of hits (finite 2 track resolution). The tracks inside jets have the same probability to get lost as the isolated ones. Fake tracks, on the other hand, tend to appear in the neighborhood of real ones, therefore more likely in jets.

2.3.4 A comparison Between Strips and Pixels Capabilities for Pattern Recognition in High p_T Jets with Pile-up

We find [12], from simulations run with Pythia 5.6, Jetset 7.3 and Geant 3.15, an average 1σ width and population for gluon jet (and similar for quark) of 12 mrad and 7 tracks at an energy of 1 TeV. At a radius of 11.5 cm from the beams, these result in spot widths (δz and δ(r-ϕ)) of 1.4 mm.

Assuming an inner detector instrumented with pixels of dimension 50 μm (r-ϕ) and 200 μm (z), we find 196 pixels within 1σ of the jet axis. The occupancy is around 3.6%.

For a strip detector with orthogonal strips of pitch 50 μm (r-ϕ) and 200 μm (z), we find 28 (r-ϕ) strips in the jet core with 7 hits (25% occupancy) and 7 (z) strips with 7 hits (100% occupancy).

One should also notice that assuming 10 hits in a detector (7 plus some noise), there would be 90 ambiguities with 90° crossed strips while less than one ghost hit with pixels (if the time stamping is done by lines and columns 3.1).

In this study [10], track reconstruction starts from the beam spot and the the innermost layer (layer 1) and reconstruct the track in the outer layers.

1. Get each hit in the innermost layer (layer 1).
2. Use each hit in layer 3 that lies in a cone given by the minimum p_T cut required (p_T cut of 2 GeV/c in this analysis).
3. Extrapolate in the fifth layer with an helix going through the beam spot (r=0) and through the found hits in the first and middle layers.
4. All hits in the outer layer are examined and a match is attempted. The criteria for the match depends on the resolution achieved in the different layers. The r-ϕ and z cuts are applied independently.
5. Apply further matching constraints with the other layers (layers 2 and 4 in this case).
6. Refit the track removing the beam constraint in order to allow tracks with a large impact parameter. All tracks with $\chi^2 \geq 5$ are rejected.

The matching cuts must be chosen optimally to obtain the required efficiency for good tracks and reject as much as possible fake tracks that are reconstructed as random combinations of hits in the different layers. On the other hand, particles may make multiple scattering (or interactions). The cuts must then be not too strict.

The analysis was done using a 5 layers SITV detectors in the barrel region ($\eta < 1.1$). The different layers considered were equipped with:

- 90° crossed strips with 50 μm in (r-ϕ) and 200 μm in z; strips are 6 cm long in both projections;
- 10 mrad crossed strips with 50 μm pitch; strips are 6 cm long;
- pixels of 50 μm in (r-ϕ) and 200 μm in z.

The cuts of this analysis have been optimised to obtain an efficiency above 97.5 % for tracks of $p_T > 2$ GeV/c. The following table gives the fraction of fake solutions obtained for different detector configurations (number of pixel superlayers, stereo angle for strips).

	90° crossing	10 mrad crossing
No pixel	310 %	25 %
Superlayer 1 in pixel	28 %	10 %
Superlayers 1+2 in pixels	8.1 %	3.1 %
Superlayers 1+2+3 in pixels	0.1 %	

The remaining fake solutions can be separated into two categories.

- The first one contains random associations of hits in the different layers. The number of such fake tracks depends on the number of possible hits in the different layers (n*(n-1) in the case of crossed strips).

- The second category contains pairs of tracks that have a very small $\Delta\phi$ or Δz. For each pair of tracks, the two real solutions will be found but also two fake solutions will be found in the case of the 90° stereo angle. Out of these 4 reconstructed tracks 2 will be very close to the two others. In fact they are almost identical and could be removed.

In conclusion, the pattern recognition and tracking capabilities are improved once a layer of pixel is used. The fraction of fake tracks comes down from 25 % without pixel layer to 10 % with the two inner layers made of pixels. While at first sight, it seems that the small stereo angle reduces better the number of fake solutions found (28 % for 90° and 10 % for 10 mrad), further cleaning might reduce this difference. One has also to remember that small stereo angle gives a poorer z resolution than 90° crossing (hence no three-dimensional tracking). Also the number of channels is larger in the small stereo angle case compared with the 90° crossing because of the difference in the strip pitch (50 compared to 200 μm). The number of channels could be reduced by 37.5 % if one decides to use 200 μm strips crossed at 90°. It is anticipated that the use of 50 μm x 50 μm 90° crossed strips could reduce a little the number of fake tracks but the number of ghosts will be the same. It would of course improve the z resolution but at the expense of a larger number of channels.

2.3.5 Conclusions

From the preceeding sections, we see that the biggest pattern recognition difficulty comes from the tracks in the jets themselves, rather than from the effects of tracks from pile-up events outside the jets. We conclude therefore that the pattern recognition problems even in initial low luminosity LHC running will be as serious as those in the later high luminosity running.

2.4 Amount of Material in the SITV Detector

Fig 5 shows the amount of material crossed by particles, as a function of pseudorapidity, for the three candidate SITV detector geometries so far investigated (discussed in detail section 5). All geometries have about 5% X_0 in the central region, but this increases in the forward directions where support structures are encountered. The use of ceramic beryllia, beryllium metal or carbon composite materials is envisaged to minimise the material traversed, and all support structures and service connections would be placed to minimise interference with the outer detectors.

3 Progress in Related Detector Technologies

3.1 Pixel detector development by the RD19 Collaboration

During the last two years the RD19 collaboration has made considerable progress. In particular, a complete hybrid detector of 1006 pixels has been built and successfully tested in the beam of the Omega heavy ion experiment [11]. The electronic circuits include a preamplifier, comparator, delay, coincidence logic and memory. The pixel size is 75 μm x 500 μm and the measured transverse resolution is 26 μm. The measured noise is 60 electrons ENC and the power consumption is 35 μW per pixel. Another circuit has also been tested, which includes a sparse data scan of the hit pixels. It directly addresses the hit lines at a frequency of 10 MHz and for each line, it reads the hit pixel address at the same clock frequency. This means that one may expect for 5 hits in a chip of 10000 pixels, all hits to be transfered in memory in less than 1 μsec. For now these circuits have a relatively slow amplifier, and are not in a radiation-hard technology.

Regarding the radiation damage [4, 5] on the detector (see also section 3.2), the main effects are the leakage current, the type inversion and the increase of the depletion voltage. The leakage current by detector element is proportional to the surface area of the element which, in the case of pixels, is a factor 250 less. This means that with pixels we will not have to cool the detector to $-20°C$. Regarding the type inversion and the increase of depletion voltage, one can gain a factor 2 by reducing the pixel detector thickness (since the signal to noise ratio is very high and, since this type of detector is single sided, we can choose a p-type substrate). If this is not enough (tests are under way), an alternative is to consider building the detector in GaAs. The electronic chips are assumed to be in very radhard technology (Thomson SOI3HD or DMILL [13]). We then expect that the pixel detectors will be able to continue to work at 1-1.5 cm from the beam, at the maximum luminosity, for 5 to 10 years (40 Mrad).

Two fast amplifiers are currently under study at CPPM in Marseille; one implemented in Thomson SOI3HD (CMOS) technology, and another in DMILL (mixed technology [13]). For ATLAS, the proposed readout system is based on a sparse data scan [14], but with 15 ns time stamping by lines and columns (fig 6). For that purpose, one may use registers controlled by the same circuitry as the analogue pipeline of the SIT (RD2) and the ADB of RD20 [15]. Because the time stamping is done by lines and columns, one might expect ghosts if pixels are hit out of time at the crossing points of lines and columns where pixels are hit in a trigger event. However, for 15 hits in a 10000 pixel chip (a jet with noise superimposed) we have computed only one ghost hit (to be compared with 200 ambiguities in crossed silicon strips with the same resolution).

The pixel electronic readout chips, will probably have an area of about 1 cm^2. One advantage of the hybrid technique is that one can have a large detector substrate with many such chips bump bonded onto it. One can also have the interconnecting buses and the supplies on the detector substrate. Test structures and detectors are being built for a prototype of such a multichip.

Using the hybrid technique, the thickness of the detector has to be reduced. Tests are under way to reduce the detector wafer thickness to 200 μm and the electronic wafer 80 μm in order to have a total thickness of 300 μm, including the bump bonding. We are

also studying a possible monolithic detector with IMEC (Leuven, Belgium), using a high resistivity SOI wafer (SIMOX or ZMR). The results from the first prototypes show that the HR silicon does not degrade too much after the SOI process. Tests of circuits implemented on the SOI silicon are under way.

The DELPHI experiment has expressed a strong interest in one to three layers of pixel detectors in the very forward region. This should be achieved in about two years from now, using the sparse data scan matrices and the hybrid multichip technique, in the shape of about 2 x 48 detectors of 2 x 5 cm^2 per layer: fig 7. We believe that detectors adapted for ATLAS will be available well in advance of the construction of the experiment.

3.2 Silicon Microstrip Detector Development by the RD20 Collaboration

The RD20 collaboration recently presented its status report [15] in which progress in the development of radiation-resistant silicon microstrips and front end signal processing electronics, and mechanical studies for large area silicon microstrip SITV detectors were reviewed, and plans for future work (June 1992-93) were outlined. In particular, the collaboration has made significant progress in the understanding of radiation damage in silicon strip detectors at LHC luminosities and in the development of on-detector analogue signal processing electronics.

Neutron and photon irradiations were begun with single-sided p-type microstrips of the DELPHI geometry. Parameterisations of radiation damage (manifested for example as increased leakage current) with integrated doses for neutron and gamma irradiation have been established.

Assuming radiation levels [4] at a luminosity of 10^{34} of the order of 10^{13} neutrons/cm^2/year and 4. $10^6/r^2$ Gray/year, where r is the distance from the beam axis in cm, the results of the RD20 radiation damage tests indicate that strip leakage current increases should be tolerable (1.1 and 0.9 μA for strips at radii of 30 and 50 cm respectively), operated continuously at $20°C$ over 10 LHC "years", each of 10^7 seconds. This would correspond to an equivalent noise charge (from all sources, but including leakage current increase after 10 "years" operation), that would still remain below 2000 electrons at short (40-50 ns) shaping times. These results overestimate the leakage current increases by not allowing for annealing during shutdowns. Also, further reductions in leakage currents could be achieved by cooling the detectors.

While these predicted performances are encouraging, it should be noted that [4] assumes an intensity only half of the full LHC luminosity. When corrected to the full LHC luminosity the data are in rough agreement with more recent and more complete radiation dose simulations [5], which include the effects of the 2 Tesla magnetic field and the contributions of gamma conversions in realistic thicknesses of material.

With current technology however, it is doubtful whether silicon microstrips (the leakage current of which (for a 50 μm x 5 cm geometry) increases by 4 μA at 10 cm radius in 10 half luminosity LHC "years" at this radiation dose) could survive as useful detectors at the full luminosity. It is at the innermost radii with the highest radiation doses that pixel diodes, with their much smaller geometries and higher radiation resistance, are well suited.

Substrate doping changes, where bulk damage leads to increasing p-type substrate dopant density in originally n-type material, are still under investigation in RD20, but it is evident

that p-type doping continues to increase after irradiation at a rate strongly dependent on the detector temperature. The operating and ambient temperatures of the detector will need to be carefully chosen, both from mechanical considerations, and to maximise detector lifetime, but it is also possible that the temperature-dependent annealing effects will set a limit to the temperature differences that can be tolerated in various sections of the detector to ensure uniformity of doping at a given radius. Further, long term studies of these effects are planned.

In addition to the tests on "existing" structures, new n- and p- type test structures carrying silicon strips with widths varying between 5 and 50 μm (DC coupled, biased and unbiased AC coupled, with and without inter-strip stops), and other test devices including diffused and polysilicon resistors, MOS capacitors, multi-guard structures, gated and ungated diodes and multi-metal crossing structures) have been designed and submitted for fabrication. P-type structures have been delivered and are under test, while delivery of n-type test structures is planned for the summer.

The fabrication of LHC prototype double-sided detectors, which awaits the results of the p- and n-side structure tests is expected to begin in Autumn 1992.

The design of all three elements of the front-end signal processing system; a 45 ns preamplifier-shaper, analogue pipe line and an analogue pulse shape processor (APSP) is complete and all have been implemented in hardware.

The preamplifier-shaper has a measured power consumption of 1.6 mW per channel and an equivalent noise charge of (400 + 65/pf) electrons at 45 ns RC-CR shaping. A radiation resistant version (possibly in a 1.2 μm CMOS process) is under consideration.

The analogue delay and buffer (ADB), built in 1.2 μm CMOS, has 15 ns sampling, with 84 storage cells and a total delay of 1005 ns (67 cells for delay, 16 for buffers and 1 for initialisation reasons). It is capable of handling up to 4 consecutive first level triggers. Power consumption is presently 0.4 mW/channel, but is expected to be reduced. After a level 1 trigger, data from the ADB are transferred to the APSP, which retrieves the original signal timing by a hardware deconvolution with a shorter time constant, based on the three or four 15 ns "snips" of the signal from the 45 ns preamplifier output signals [16].

The University of Oslo and SI (Senter for Industriforskning, OSLO) is investigating advanced readout architectures using a net of "Switched Interconnections of Parallel Processors" (SWIPP) [17]. Such a network represents a flexible interconnection scheme for heterogeneous nodes. The nodes, "Compute Engines" (CE), would be of various types: processors, memory modules, storage devices, input/output devices or bridges to other networks. A detector module (DM) represents a CE. The CEs would be interconnected through "Protocol Engines" (PE) with data flow via pairs of optical fibres through 16:16 bidirectional crossbar switches, at up to 1 Gbit/s simultaneous data transfer for each channel, and multiple switch stages (1 to 16). At the detector module level, the transport of Front End chip I/O signals would be handled by buses (fig 8). An ADC would be implemented on the module so that data could be transported to and from the module in digital form over a pair of fibres. A PE would be responsible for the transport. Fibres from many detector modules are concentrated in switches up to the capacity of one fibre pair. Each module "cluster" would be handled by a Local Level 2 (LL2) trigger processor, which reduces the amount of data, and further concentration would be accomplished by a second stage of switches.

A complete readout system of this form is illustrated in fig 9. Simulations of data rates

and the required capacities of buffers and data lines are presently under way.

The RD20 collaboration is also considering a variety of possibilities for low mass mechanically stable support and cooling structures. These are reviewed separately in section 5.

3.3 GaAs Detector Development by the RD8 Collaboration.

3.3.1 Introduction

Interest in GaAs detectors has revived over the last few years after a gap of almost twenty years since the first investigations of their potential as gamma-ray and X-ray detectors [18]. Variability of the GaAs material and the unpredictability of the performance of early detectors led to a period of stagnation in their development. Substantial improvements have recently been made, however, in the quality of the semi-insulating GaAs wafers which are the standard for device fabrication in an expanding world-wide industry [19]. The urgent requirement for very fast, radiation-hard detectors for the new generation of large hadron colliders has therefore prompted us to re-examine the prospects for GaAs detectors fabricated from the higher quality, cheaper wafers which have now become available.

It is perhaps worthwhile recalling the principal advantages and disadvantages of GaAs as a semiconductor. In its favour are a large, direct band-gap (1.4 eV), high electron mobility (up to six times higher than that of silicon), higher specific energy loss (5.6 MeV/cm) and its compatibility with potential opto-electronic read-out devices in similar III-V semiconductor materials. Its disadvantages are its shorter radiation length (2.3 cm) compared to silicon, the crystalline imperfections of commercially-available substrate wafers and the mechanical fragility of the thin layers from which high energy particle detectors might be constructed. In what follows, an attempt is made to demonstrate that it is indeed possible to construct acceptable detectors for HEP applications, using relatively simple processing to manufacture Schottky barrier diodes.

To summarise our conclusions after about two years, we have established that it is possible to fabricate simple diodes and microstrip detectors in our own institutes, with a turn-around time of a few days. The detectors have an efficiency for recording the passage of minimum ionising particles which exceeds 97%, typically, for thicknesses of 200 μm or above [20]. (This is roughly equivalent to twice as thick a layer of silicon in terms of charge released by a m.i.p.). Due to the presence of traps in the semiconductor material, the efficiency of charge collection is substantially less than 100%, although it continues to increase with applied reverse bias voltage up to more than 50% for a bias of around 1V/μm. The leakage currents which we have measured are also much higher than in silicon, typically by more than an order of magnitude. We are attempting to understand why these currents are so high and how much we may be able to reduce them by better care in preparation and processing of the wafer. In any event, the leakage currents do not appear to increase significantly when the detectors are irradiated with gamma rays, up to a total dose of at least 20 MRad, or with 1 MeV neutrons up to a fluence of at least 10^{14} n/cm^2. The charge collection efficiency falls for neutron fluences exceeding this level [21], but the detectors continue to distinguish m.i.p. signals from noise up to almost 10^{15} n/cm^2. Measurements of the speed of response have been made with picosecond laser and slow proton excitation [22]. The measured pulse

base width of 4 - 5 nsec seems satisfactory for potential applications at the LHC. Microstrip detectors have been fabricated on different wafer materials and shown to work satisfactorily in high energy pion test beams at CERN. Radiation hardness of these microstrip structures has also been established at the level of 10^{14} n/cm^2. The measured signal to noise ratio from these detectors was around 6-8:1 for 400-500 μm thick detectors with an AMPLEX [23] read-out system.

We are continuing to test a variety of different wafer materials and hoping to improve the quality of our microstrip detectors by improved processing. With a view to constructing a prototype detector suitable for a forward tracker element of an LHC detector [24], we are conducting tests to evaluate how thin and how large an area is practical in the relatively brittle GaAs. We are in contact with industry with the aim of obtaining thick samples of epitaxial GaAs wafers, which should deliver better performance than the semi-insulating material but probably at a much higher cost. Industrial advice is also being sought about the possibility of providing mechanical support for thinner detectors in the form of thin glass or ceramic backing layers. We hope also to be able to test prototype GaAs read-out electronics elements this summer. We expect to have a hybrid version of a preamplifier using HBT technology and a low-noise MOSFET preamp for comparison with our AMPLEX system.

3.3.2 The Test Beam Set-up

Preliminary test beam evaluation of the first GaAs microstrip detectors was made in June 1991 at the CERN PS, with 6 GeV/c pions. These other microstrip detectors were more extensively tested in the X1 beam of the CERN SPS during August 1991, using pions and electrons from 20 GeV/c up to 70 GeV/c. The particle trajectories were defined by means of crossed scintillation counters, (5 mm wide as seen by the beam particles), and more precisely by two silicon microstrip counters.

In November 1991, a further test beam run was carried out in the PS test beam. The aim of this series of tests was mainly to investigate the deterioration in performance of two of the previously tested GaAs microstrip detectors which had subsequently been irradiated with 1 MeV neutrons to a total flux of 10^{14} n/cm^2 in the ISIS facility at RAL [25].

3.3.3 The Detectors Tested

A total of ten GaAs microstrip detectors was subjected to test beam evaluation. The Schottky diode detectors fabricated in Glasgow, using facilities provided by the Department of Electrical and Electronic Engineering, were made using two different masks from Micron Semiconductors Ltd. The first type had strips 17 mm long and 300 μm wide, with a 30 μm interstrip gap. The strips of the second were 25 mm long, 265 μm wide and 100 μm apart. The detectors were all 500 - 600 μm in thickness. Details are given in Table 1. The microstrips of Schottky detectors made at the University of Modena on a 600 μm substrate were 44 mm long, 100 μm wide and separated by 100 μm. In addition to these microstrip detectors which were fabricated "in-house" in university laboratories, two commercially-made Schottky detectors were tested. These were supplied by Telettra SA in Milan. The microstrips were 18 mm long, 100 μm wide and 100 μm apart on a substrate of 450 μm thickness. One interesting aspect of the process used in their fabrication was the use of silicon nitride surface passivation. We were very anxious to learn whether the use of this type of surface protection

might lead to a deterioration in the radiation-hardness of the detectors, in similar fashion to the effect of trapped surface charge in silicon detectors. An alternative to using Schottky diode technology is to fabricate detectors as *p i n* detectors, using an MBE-grown n-type layer and in-diffused Zn p-layer to form the junction. One microstrip detector of this design, fabricated at the University of Sheffield III-V Facility, was tested in the SPS beam at CERN. Dimensional details of this device are given also in Table 1. Both approaches to detector fabrication will continue to be studied within the RD8 collaboration.

Detector	Microstrip length (mm)	width (μm)	pitch (μm)	thickness (μm)	E_{max} (V/cm)	ϵ_c%	ϵ_d%	S/N
SB3	16	300	330	500	4600	10		5.1
SB4	16	300	330	500	4600	11	94	5.5
SB5	25	275	375	600	6667	16.5	97	8.6
GLADYS	25	275	375	600	4167	11	97	9.1
Telettra I	18	100	200	450	9444	19	90	7.4
Telettra II	18	100	200	450	6670	16	90	6.3
Sheffield *pin*	25	275	375	400	9375	9	> 80	7.5
Modena I	44	200	400	650	13077	41	-	17.5
Modena II	44	200	400	650	12300	27	-	11.5

3.3.4 Analysis of Data from the Test Beam

For each of the GaAs microstrip detectors tested, data were collected for a range of reverse bias voltages up to the breakdown threshold, using incident pions to monitor the corresponding variation of the pulse height due to minimum ionising particles (m.i.p.). Pulse height spectra due to m.i.p. were obtained as follows: the strip containing the maximum pulse amplitude after pedestal subtraction was first found. The pulse amplitude in each neighbouring strip was then added to this, to allow for sharing. The resulting spectrum shows a typical Landau distribution (fig 10). Using the measured alignment of the silicon and GaAs horizontal strips, the pulse height spectrum was obtained for a particular GaAs strip, defined by a simultaneous hit in the nearest silicon strip.

Figs. 10 (a-f) shows typical pulse height spectra obtained at a reverse bias close to the breakdown threshold for the different detectors. (This breakdown voltage was always considerably smaller than that expected for a uniform voltage gradient across the material and the known breakdown strength of GaAs.) The superimposed smooth curves result from a fit to the data of a Landau distribution into which a Gaussian noise distribution has been folded, together with a Gaussian background of arbitrary position and width [26].

The standard deviation of the noise distribution from the fit, 34.8 ± 1.4 channels is 15% broader than that expected from the measured pedestal width, due to fluctuations in gain from strip to strip. This is illustrated in fig 11 (a and b), where the peak position in the appropriate strip of the GaAs detector is plotted as a function of (a) the hit strip in the silicon detector and (b) the position along the strip length. The distributions for the edge

strips had long tails and have been omitted from the plots. Two read-out channels (30 and 32) were not working properly. Apart from these exceptions, the figures indicate that the deviations from uniformity observed in the response of the microstrip detectors from strip to strip and also along their length are not more than around ±10%. This is likely to be acceptable for collider tracking applications.

Two approaches were made to the determination of the efficiency of each detector for collecting the charge signal deposited by traversing particles. The first used a comparison of the GaAs pulse height with that from the silicon detectors which were assumed to have full charge collection efficiency. Allowance was made for the difference in thickness and specific ionisation of the two detectors. The second method required absolute calibration of the read-out electronics with pulses of known charge from a pulse generator. The charge collection efficiency was calculated from the ratio of the charge equivalent to the measured peak pulse height to the charge expected from a minimum ionising particle, assuming that the energy required to produce an electron-hole pair is 4.2 eV in GaAs [18]. The two methods were found to give consistent results.

So far, the detectors tested have been relatively coarse-pitched microstrip devices. The measured sharing of charge between adjacent strips, shown in fig 12, amounts to only a few per cent of the peak strip signal, typically. Further tests are planned with finer strips on a narrower pitch to evaluate the sharing in conditions more akin to those expected in LHC applications.

Fig 13 illustrates the variation with reverse bias of the measured efficiency for collection of the charge released by the passage of a m.i.p. It can be seen that the charge collection efficiency, ϵ_c, is typically less than or of order 20%. This value is certainly influenced by the existence of charge-trapping centres in the GaAs material. An explanation has still to be found for the observation that the performance of the microstrips is more than a factor of two worse than that of simple, single pad detectors. Relatively large numbers of these have been tested since the beginning of this programme of research and give typical values for ϵ_c which are well above 50%.

Two of the microstrip detectors, (SB5 and TelettraII), were subjected to neutron irradiation to an integrated dose of 10^{14} n/cm^2 at the ISIS irradiation facility. They were then tested again with 6 GeV/c pions in a CERN PS test beam. As shown in fig 14, for example, the most probable pulse height from m.i.p. and the pulse height resolution are scarcely affected by the irradiation.

Gamma irradiation tests have also been carried out on another of the Telettra detectors up to a total dose exceeding 20 MRad. The detector was continuously biased during the irradiation. Changes in the measured reverse bias leakage current and in the pulse height due to m.i.p. did not exceed a few per cent. It may be concluded that GaAs detectors are well able to withstand typical irradiation doses to be expected in the forward regions of an LHC spectrometer.

3.3.5 Conclusions

Although many questions remain to be answered about the behaviour of GaAs as a particle detector, in particular with respect to charge collection efficiency, optimum thickness and most cost-effective detector size, there are now grounds for optimism that this material can

offer device characteristics which are essential for highest luminosity operations at the new generation of large hadron colliders.

4 Status of the Silicon Inner Tracker Design for the SDC experiment at SSC.

4.1 General

The status of the SDC silicon tracking detector conceptual design is summarised in [27]. Together with outer tracking superlayers in the solenoidal field volume and chambers at large radius outside the calorimeter for tracking muons, it forms the SDC charged particle tracking system. The silicon array will provide charged particle detection at radii smaller than 50 cm. The goals for the (entire) tracking system of SDC are given in [27], which stresses that for the field and magnet dimensions proposed for SDC it would be extremely difficult to meet the SDC goals for momentum resolution at large or small rapidities, for vertexing, or for rapidity acceptance using detection elements restricted to radii greater than 50 cm. Thus the silicon forms a critical element in the tracking system. In addition it is expected to provide a critical role in pattern recognition at high luminosity.

Fig 15 shows a quarter section of the SDC silicon system. It has cylindrical layers (total area 6.8 m^2 of silicon) giving at least 6 planes of coverage out to a rapidity of 0.9, with planar disk layers (total area 10.2 m^2 of silicon) giving at least 6 planes of coverage out to a rapidity of 2.5. An option for the detector is to have the layers inside 15 cm (the first two barrel layers) made of pixel detectors. Relevant pixel R&D results are summarised in [28].

4.2 SDC Tracking Requirements

The summary of the SDC tracking requirements is lengthy, and is given in full in [27]. In this report, only those specifications pertaining to the SDC SITV detector are reproduced:

- *Acceptance and p_T resolution:*
  1. Pseudorapidity coverage out to at least $\pm$ 2.5 ($H^0 \rightarrow$ 4 charged lepton geometrical efficiency $\geq$ 60 % for $m_H \geq$ 200 GeV/c^2).
  2. Reconstructed (as opposed to parametric) vertex constrained momentum resolution for isolated charged tracks of $\sigma_{p_T}/p_T^2 \leq$ 20 % TeV^{-1} for (-1.8 $\leq \eta \leq$ 1.8), allowed to rise to 100 % TeV^{-1} as $\eta \rightarrow \pm$ 2.5.
- Reconstruction efficiency within this acceptance $\geq$ 97 % for isolated tracks having $p_T \geq$ 10 GeV/c, with $\leq$ 0.1 false tracks of $p_T \geq$ 10 per trigger. (Efficiency greater than 90 % for detecting all four leptons from $H^0 \rightarrow$ 4 charged leptons, exclusive of lepton identification - E/p and η,ϕ matching - and trigger cuts). This requirement is specified for design luminosity (10^{33} $cm^{-2}sec^{-1}$, but with occupancy assumed twice that calculated by Monte Carlo for pp $\rightarrow$ X.
- Reconstruction efficiency as in (2) $\geq$ 90 % for 10 times the design luminosity.
- B tagging efficiency for top studies with 125 GeV/$c^2 \leq M_t \leq$ 250 GeV/c^2:
  - reconstruction efficiency $\geq$ 80 % for tracks of $p_T >$ 5 GeV/c with less than 10 % fakes, within jets of p_T up to 100 GeV/c for b tagging using leptons;

- b tagging efficiency $\geq$ 25 % with $\geq$ 90 % purity using detached vertices. This implies impact parameter resolution $\leq$ 20 μm for stiff tracks, $\leq$ 100 μm for p_T around 1 GeV/c, and $\geq$ 85 % efficiency for finding tracks with p_T > 1 GeV/c within jets of p_T up to 100 GeV/c.

- Material $\leq$ 15% X_0, $\leq$ 7% X_0 inside 50 cm (average over -2.5$\leq\eta\leq$+2.5) for efficiency of electron ID (E/p cut).

- Jet charged multiplicity measurement within 15% for jets up to p_T = 500 GeV/c (to distinguish isolated W's, and to study fragmentation for QCD studies and background modelling).

- Resolution for measurement of the z component of the vertex of 2 mm, to separate pile-up interactions.

- Survivability at standard luminosity for $\geq$ 10 years.

- Allows a natural path for upgrading to a system with survivability of $\geq$10 years at 10 times the standard luminosity with emphasis (eg momentum resolution, pattern recognition, isolated track efficiency) to be decided based on what is learned during initial running.

4.3 Mechanical Alignment Considerations.

The microstrip detectors will be double-sided with 6 and 12 cm strips at 50 μm pitch on each side and a stereo angle (u,z) or (v,z) of $\pm$10 mrad (1.5 mm resolution) on radially-adjacent detector pairs. The total number of electronic channels is estimated at 6 x 10^6. The quantitative effects of systematic alignment errors and some ideas for wafer location measurement during assembly, using X-rays, are discussed in [29, 30]. The work already done in trying to understand alignment-related uncertainties is of great interest to our developments for LHC.

The SDC momentum resolution goals allow a degradation of $\leq$ 10% due to random placement errors and $\leq$ 33% for correlated errors. These lead to the following goals for the detector stability relative to a data base of positions:

- circumferential position error $\leq$ 5 μm;

- radial location error $\leq$ 80 μm;

- longitudinal location error $\leq$ 250 μm.

4.4 Mechanical Structure and Cooling Considerations.

Fig 16 shows the SDC Silicon Tracking System baseline mechanical layout. The mechanical structure is envisaged to be of graphite-epoxy composite materials chosen in some locations (the main support shells) to have effectively zero thermal expansion, and in others (the silicon ladder supports) to be matched to the thermal expansivity of silicon, with kinematic mounts between. Much research has been undertaken to find composites that exhibit combinations of the required expansivity characteristics with radiation tolerance.

It is planned to cool the detector evaporatively with a (flammable) hydrocarbon (butane). A conceptual design has been developed for a refrigeration and recirculation system and the necessary safety and thermal interlocks. Attempts have been made to understand the operating procedures and make failure analyses. The FY92 mechanical R&D will concentrate heavily on the development and testing of manufacturable (eg polystyrene) wick structures of very long radiation length. It has been estimated that the wick material must contain pores of 6 μm diameter to hold the liquid butane against up to 2 meters of hydrostatic head.

5 Development of a Conceptual SITV Geometry for ATLAS

5.1 Candidate Mechanical Geometries.

In this section we discuss the baseline SITV geometry (fig 2), proposed by a group from RAL, now being considered for the ATLAS detector and presented in the letter of intent, and compare it with two other SITV geometries that have been studied. The baseline geometry has pseudorapidity coverage out to $\eta = \pm 1.5$, and is extendable, by virtue of its mechanical support structure, to higher rapidities at extra cost. It combines an innermost superlayer of pixel detectors, at about 11.5 cm of the beams [31], with double-sided silicon microstrips at larger radii of 21.9 and 33.0 cm, together with wheels of forward pixels or strips at z = 48 and 56 cm. Also supported from the same structure will be wheels of GaAs strip detectors detectors at z = 57 - 70 cm and z = 96 - 109 cm from the interaction point having an overlap in η with the SITV for relative alignment purposes.

The support structure for the three superlayers would be provided by three concentric beryllium cylinders, and would exploit the simplicity of a light, all metal construction. The gaps in each detector layer, caused by the electronics substrates, are covered by additional silicon detectors mounted on the outside of each cylinder, so that three full double layers of silicon are provided. Each beryllium cylinder could be made of "composite" construction [31]. In a preliminary study, a 0.8 mm thick beryllium foil is preformed into a "zig-zag" section, and is sandwiched (by brazing) between two skins of 0.8 mm beryllium; the "composite" cylinders thus formed also carrying the coolant in roughly 10% of the internal channel spaces. These cylinders are split axially into two halves to embrace the beam pipe.

The RAL group has unparalleled experience in the successful engineering of beryllium structures for SITV detectors (having just finished the commissioning of the SLD pixel inner tracker) and has unique relationships with the very few fabricants of non-military beryllium structures. Tentative quotations received (10/4/92) [31] for cylinders of this construction of 1.5 meters (longer than needed) and radii between 10 and 30 cm encourage us to believe that a cylindrical support structure capable of carrying silicon detectors out to high pseudorapidities could be built at a reasonable cost. It is to be expected that these cylinders of beryllium will be a particularly stable mechanical support structure, though great care will needed in all designs using beryllium due to the dissimilarity (a factor of about two) between its thermal expansion coefficient and that of silicon.

Possible microstrip detector configurations include 50x50 μm, 60x60 μm or 100x100 μm with small angle (10 mrad or 1°) stereo, or 50x200 μm with larger angle (up to 90°) crossing. The final choice of strip pitch and crossing angle will be determined from a study of pattern recognition capability at high luminosity, and economic constraints. It is worth noting here that 50x200 μm pitch at 90° crossing reduces the channel count by nearly 40% compared with 50x50 μm pitch with small angle stereo.

The outer two superlayers will contain about 4 10^6 detector elements on about 2500 silicon wafers (30-60 mm x 60 mm). Because of the large number of sensitive elements, data reduction and sparsification will be done locally at the detector, the data from one or more detector wafers being read out serially on a single optical fibre. Each layer of pixels will contain about 372 detector wafers, with about 8 10^7 detector elements. It is envisioned to

read out the pixels on each wafer with an array of 1 cm^2 readout chips (typically 10^4 pixels per chip) directly bump bonded to the wafers. The outputs of the pixel readout chips on each wafer will be further multiplexed, and we hope to read out each wafer with a single optical fibre.

We continue by reviewing the two other SITV geometries that have so far been considered:

1. A design of the Cracow group [6, 32, 33, 34] (fig 17) which envisages a geometric layout of nested ellipsoidal surfaces giving 3 double layers of silicon microstrip detectors of 50 μm pitch with a small stereo angle (10 mrad) out to (originally) $\pm$ 2 units or (more recently) $\pm$ 1.5 units of pseudorapidity.

   The three ellipsoids would be mounted in an open geometry through which gas would be forced at high velocity to convectively cool the wafers. Its attractiveness lies in its particularly light construction: in particular the use of helium gas cooling would require no coolant ducting built in the support structure. The three detector superlayers are envisioned to be supported from carbon composite shells each made up from honeycomb cylinders of several different radii (fig 19). The ellipsoidal shape would eliminate the need for separate end caps, thus simplifying the mechanical construction, and reduces the surface area of silicon by 30% relative to an ***all cylinder*** geometry with the same rapidity coverage.

   A recently-proposed reduction in pseudorapidity coverage from $\pm$ 2 units [6, 32, 33] to $\pm$ 1.5 unit (including $\pm$ 6 cm vertex smearing in z) [34], has reduced the length of the two outer ellipsoidal arrays from 1700 and 1040 mm to 995 and 750 mm respectively. The channel count for double-sided microstrips at 50 μm pitch with small angle stereo is now about 5.5 10^6. The latest geometry, though not well suited to subsequent upgrade higher rapidity, is light - 5.8 kg for an area of 8.3 m^3 of silicon, since the silicon itself forms part of the structural reinforcement. The equivalent radiation length versus pseudo rapidity is shown, together with that of the other candidate geometries in fig 5.

   Since in this geometry, it is particularly important to locate all power supply and readout cables so as not to impede the coolant gas flow (fig 20), two open ladder full scale models have been constructed with cooling studies in mind. Detailed power supply and readout cable geometries will worked out and convective cooling tests on full-scale models will be made.

2. A design of the CPPM Marseille group [12, 35] (fig 18) which envisages a geometric layout of cylindrical and conic detector surfaces giving at least 4 layers of detector coverage out to $\pm$ 2 units of pseudorapidity, with the outermost surfaces being double layers of 200 μm x 50 μm pitch double-sided silicon microstrips at 90° crossing, combined with the innermost surfaces as double layers of 200 μm X 50 μm pixel detectors.

   Although of similar implementation in the central or "cylindrical" region, the proposed CPPM geometry has a wider pseudorapidity acceptance, with cones covering the interval ($1.23 \leq \eta \leq 2.0$), rather than the wheels of the baseline design. The coolant would be carried in axial (i.e. parallel with the z direction) rectangular support channels to which one (z) edge of each wafer is attached. The ends of these liquid channels are then attached to support and cooling rings (and also to support rings at their 1/3 and

2/3 length positions) to form effective cylinders with nominal radii 11.5 cm (2 layers of wafers), 20 cm (1 layer) and 32 cm (2 layers). The support rings and cooling channels are proposed to be made from beryllium.

We have continued to develop the geometry ($\eta \leq \pm 2.0$: including a beam spot variation of $\sigma_z = \pm$ 80 mm) first proposed in [12] by optimising (minimising) the overlap between the silicon wafers. The same acceptance can be provided with a total of 3.6 10^6 50 μm x 200 μm double sided silicon microstrips with 90 $^\circ$ crossing together with 2.24 10^8 50 μm x 200 μm pixel detector elements, on a total of about 3000 wafers. The use of forward cones is particularly valuable for maximising rapidity acceptance with the minimum area of silicon out to higher rapidity.

Studies of geometries with acceptance out to ($\eta \leq \pm 1.5$) have been made to find the number of silicon wafers and detector elements needed in an all (tapering) cylinder projective geometry (a), and in a non-projective cylinder and cone geometry (b).

(a) 3.4 10^6 50 μm x 200 μm double sided strips at 90^o with 1.6 10^8 50 μm x 200 μm pixels on a total of 2600 wafers;

(b) 3.1 10^6 50 μm x 200 μm double sided strips at 90^o with 1.6 10^8 50 μm x 200 μm pixels on a total of 2500 wafers.

We see that going from an acceptance of $\eta \leq \pm 2.0$ (cylinders and cones) to $\eta \leq \pm 1.5$ (cylinders and cones), the number of channels is reduced by only 20 % with similar physical performances ($\Delta p_T/p_T$). The same acceptance ($\eta \leq \pm 1.5$) with projective geometry requires cylinders with only 10 % increase but with somewhat better physical performances in forward region.

5.2 Consideration of the Cooling Variants

Recent studies by the RD20 collaboration of the temperature dependence of self annealing in silicon wafers exposed to radiation doses of the same order as those expected in LHC operation suggest [15] a maximum tolerable temperature difference of 5^oC for uniform long-term, low-noise operation of an LHC SITV detector.

5.2.1 The CPPM Marseille Cooling Variant.

The extremely high heat capacity of water (4180 J $kg^{-1o}C^{-1}$) makes it a very attractive coolant for a SITV detector with a high power dissipation. Its use promises a particularly simple and inexpensive recirculation and control system. With silicon detector bonded to coolant channels, a very high degree of wafer to wafer temperature uniformity would be expected.

A systematic series of finite element simulations and measurements [35, 36] has been made of the efficiency of water cooling power dissipating silicon wafers which are tightly attached to axial cooling channels.

These results, which are internally consistent, have however shown that the thermal gradients expected across silicon wafers dissipating a realistic 0.4 Watt/cm^2 (over the whole wafer area in the case of a hybridised pixel wafer, or at the edge(s) in a silicon microstrip

detector wafer - assuming 2 mW/channel and a maximum strip density of 200/cm in the (r-ϕ) direction that is orthogonal to the axial cooling channels) can exceed $5°C$ for silicon wafers of dimension 4-6 cm along a side.

These results indicate that one or more of the following novel approaches will be necessary to reduce the thermal impedance seen by the SITV detector readout electronics in the (r-ϕ) direction for use with axial cooling channels if smaller wafers are not to prove necessary:

1. The use of a very high thermal conductivity substrate material for the readout electronics, which would then be both thermally and electrically bonded to the lower thermal conductivity detector wafer; (RAL has some experience in handling beryllia, which is a material in this category).

2. The use of a very high thermal conductivity component in parallel (and thermally bonded) with the readout electronics substrate material; for example a heat pipe with its cold (condensive) end bonded to the liquid cooling channel and its hot (evaporative) end in contact with the electronics to be cooled (fig 21), if these can be manufactured inexpensively in bulk from a low mass material such as aluminium, or better still beryllium. CPPM has made an extensive series of heat pipe studies for this application, and the results are presented below.

3. The use of auxiliary cooling techniques such as (convective) gas flow or evaporative cooling: (both these techniques are described in some detail later).

Water Cooling Channel and Heat Pipe Cooling Studies.

Commercially-manufactured heat pipes offer a very simple and modular technique for the removal of large amounts of heat in the direction perpendicular to the axial flow of cooling water. Making use of the latent heat of vapourisation of a liquid in pressure equilibrium with its vapour, and in the absence of all other uncondensible gases (i.e. in an extremely clean, sealed enclosure), the heat pipe evaporation- condensation cycle can generate thermal conductivities 100-1000 times higher than that of copper. In our application, the evaporation takes place at the end in contact with the electronics, and the condensation at the end in contact with the cooling channel. Machined grooves or an internal wick in the heat pipes continuously bring liquid by capillarity the few centimeters to the evaporator end. Fig 21 shows a thermal conductivity study made on a heat pipe in a very useful rectangular geometry.

Figure 22 shows a simulator for a 50 mm square silicon microstrip wafer. Alumina substrates carry heater elements that simulate the dissipation of microstrip readout electronics: assumed to be 1000 channels at 50 μm pitch perpendicular to the water channel (representing (r-ϕ)), and in z. A heat pipe is held in contact with the heat producing element, connecting it to the coolant channel through a very low thermal impedance. Power dissipations equivalent to 1.5, 2.0, 2.5 and 3.0 mW per channel were considered. Platinum resistance thermometers were placed on the alumina readout strips and the (indirectly heated) silicon detector wafer itself, and in the input and output water flow. At a realistic power density of 2 mW/channel, a temperature gradient of about 2°C was seen between the outboard edge of the heated electronics substrate, and the cooled inner edge. No heat was generated on

the 50 x 50 mm detector, since in real detector, the heating effects of strip leakage currents would be small compared to those of the readout electronics.

Figure 23 shows a simulator for a pair of 25 x 50 mm silicon pixel wafers. Heated surfaces representing hybrid readout electronics bump-bonded to the entire area of the detector wafer are connected via rectangular heat pipes to the water cooling channel. Power dissipations equivalent to 0.2, 0.4, 0.6 and 0.8 Wcm^{-2} per channel were considered (0.4 Wcm^{-2} represents a dissipation of 40 μW per pixel for the readout electronics). Platinum resistance thermometers were placed on the readout surfaces, and in the input and output water flow. The worst case temperature gradients were of the order of 2.5 °C, and we believe these were dominate by the non-optimised thermal contact between the sensors and the heated surface itself.

Based on the very encouraging results of figures 22 and 23, the next phase of our thermal study will be to investigate the cooling of a linear array of pixel and microstrip detector wafers in a realistic LHC SITV geometry.

Note. The RAL group proposes to use thermal conductivity materials (principally beryllium and beryllia) to provide a low thermal resistance path to the water-cooled beryllium support cylinders. Although the temperature difference is expected to be of the order of $5 - 10°C$,this should not cause a problem as the temperature differences between any two detectors should be small. (All the heat paths will have very similar resistances). To equalise the temperatures further, an inert gas may be purged through the detector volume. This gas would be pre-cooled to the desired (average) silicon detector temperature. In this way it is aimed to maintain a ΔT between detectors of less than $0.5°C$. Finite element analysis of this proposal, for comparison with those of the CPPM close-coupled liquid channel scheme, is under way, and construction of a test sector is planned.

5.2.2 The Cracow Cooling Proposal.

The Cracow group has made some preliminary studies of the cooling that might be afforded an SITV detector by a high volume flow of helium gas. Helium gas is a particularly attractive cooling possibility for two reasons:

1. it would require no coolant channels in the support structure;
2. its density is seven times less than air, while its heat transfer coefficient four times that of the same mass flow of air.

The open ellipsoidal geometry is necessary for each wafer to have its own flow of cooling gas. In this geometry, it is particularly important to locate all power supply and readout cables so as not to impede the coolant gas flow. Electronic elements on the wafers and side walls of the silicon ladders are connected by kapton cables as shown in fig 20. The side walls would be hybrids on which all power supply and fibre optic links are located. With cooling studies in mind, two open ladder full scale models have been constructed. Detailed power supply and readout cable geometries will worked out and convective cooling tests on full-scale models will be made.

For a power dissipation of about 2 mW/channel, a temperature difference of $3.3°C$ was calculated [6] at the helium input and output for a volume flow of 3 m^3/sec (7 ms^{-1} linear

flow), while the temperature difference between the wafers and the gas was calculated to be about 8° C.

In the RD20 framework, a programme of work on computer simulation and experimental testing of the gas cooling concept has been undertaken, giving the following results:

1. *Finite Element Analysis*

   - The heat transfer coefficient for helium gas flow at a Reynolds number of about 3300 is four times that of air.
   - The dynamic (vibration, deflection) effect of helium flow at this Reynolds number is negligible.
   - The maximum temperature difference between the helium gas (7 ms^{-1}) and a double sided detector wafer is between 7 and 11 °C, assuming a power dissipation of 2 mW/channel. The worst case was when two rows of readout chips (small angle stereo readout) were placed on the upper and lower surfaces of the detector (one above the other).
   - Deflections of the wafers caused by temperature gradient are below 1 μm.
   - The maximum deflection of a 500 mm long self-supporting silicon ladder module, subject to gravity load when its ends are simply supported was below 3 μm.

2. *Test Results*

   - The deflection of the 35 mm free end of a silicon wafer under a perpendicular air flow of 2.5 ms^{-1} was about 1 μm (2.5 ms^{-1} gives the same dynamic pressure as 7 ms^{-1} of helium).
   - In the experiment, with a measurement accuracy of 1 μm, no vibrations were observed for a silicon module situated in an air flow of 5 ms^{-1}.
   - The maximum temperature differences between the cooling air and the detector, for flow rates of 4 ms^{-1} and 1 ms^{-1}, were about 9 and 13 °C respectively. In both cases, the power dissipation was 1.1 mW/channel for a double-sided wafer with chips placed one above another (see fig 25).
   - The maximum temperature difference between the cooling air (1 ms^{-1}) and the detector was about 19 °C, for a double-sided wafer with a power dissipation of 2.5 mW/ channel, and with chips placed perpendicular on the two sides. This result, recalculated for 7 ms^{-1} of helium gives 8°, see fig 25.
   - The maximum deflection of a 500 mm long self-supporting silicon ladder module, subject to gravity load when its ends are simply supported was about 14 μm.

A helium recirculation loop and several dummy silicon modules now under construction will allow a number of thermal and deformation studies to be made, including:

1. That of "micro" gas flow, channelling between the inner and outer silicon wafer ellipsoids of each ladder, using thermo-anemometry techniques with equipment already in hand, with a view to establishing the efficacy of the cooling afforded to those wafers on the lee side.

2. Actual temperature measurement, following the attachment of resistive heater pads to the wafers to simulate electronics power dissipation.

3. "Macro" gas flow distribution (i.e.: radial, azimuthal or axial between the ellipsoidal superlayers) studies on full size, full geometry models with realistic cable routing simulation.

5.2.3 Other Cooling Studies.

Within the RD20 Collaboration, the University of Oslo, S.I., RAL and CPPM have been considering the possibilities and implications of evaporative and multiphase cooling using inert (and environmentally acceptable) fluorocarbons. The inert liquids contain no chlorine, are non-flammable and essentially non - reactive chemically. Their dielectric strength is very high.

Of particular interest are radiation damage studies of these materials [37, 38] that indicate in particular that fluorine liberation under neutron bombardment will be at such low levels as not to be hazardous for long term operation at LHC. Prior calculations indicated that less than 10^{-5} of the fluorine atoms would be liberated, but these assumed that the energy spectrum of the neutrons extends up to only a few MeV. Measurements are under way to experimentally investigate whether higher energy neutrons accelerate the fluorocarbon molecular disintegration.

Oslo and SI are developing a design for a possible mechanical structure made of organic fibre material (such materials can have long radiation lengths $\geq$ 20 cm, low mass and good mechanical and thermal stability) through which a bi-phase fluorocarbon refrigerant is passed. The same structure might be used both for distributing the cooling liquid and the electrical bus lines.

A prototype support structure has been used, using a composite of woven Kevlar fibres, in an epoxy matrix. Since Kevlar is an insulator the electrical lines are printed directly onto it. The material was laminated in a mould under a pressure of 50 Ncm^{-2} at a temperature of 150 °C and a novel technique was developed to print the electrical circuits onto the support substrate in the same operation. Using a single mould, the ladder elements from which the structure is made are identical to high precision.

Ladders with a wall thickness of 180 μm have been made. The thermal expansion of Kevlar along its fibres has been measured to be very close to that of Silicon. The material has been exposed to high levels of neutron doses (10^{13} cm^{-2}) without any measurable changes in its mechanical or thermal properties. After 2 hours the induced radioactivity is about 350000 disintegrations per minute mainly due to impurities.

A detector with some 20000 channels of Silicon strips and with VLSI circuits in CMOS to amplify, digitise and store the signals has been constructed using this technique, and is being used as a tracker in the luminosity monitor of the DELPHI experiment at LEP.

It is proposed to bond the VLSI-chips directly onto the Silicon detectors using the non-active area as substrate, making one rigid mechanical piece - the detector module. The modules are precision-mounted on the ladder elements. The proposed Kevlar structure would contain cooling channels for the fluorocarbon refrigerant. Due to the very high cooling efficiency achieved by evaporative cooling the detector area would not be appreciably heated, and the thermal gradient between the heat source (VLSI- readout electronics chip) and the

liquid (at boiling temperature) will be very small. Assuming 15KW of dissipated heat in the detector volume, a flow of only about 0.115 l/s of the Fluorinert liquid would remove this heat in ideal conditions. The actual amount will depend on the heat transfer efficiencies in the constructed system.

Two designs for the cooling system have been considered:

1. Studies of "closed" cycle (channelled) multiphase fluorinert cooling investigations by SI [39] indicate that very high heat transfer coefficients are in principle possible. In such a system the detectors and the VLSI-chips are not in direct contact with the fluorocarbon liquid/vapour. A two phase flow will exist inside the cooling channels of the support structure. One challenge will be to obtain a smooth two phase flow and to reduce the thermal resistance between the VLSI-chip and the liquid, but another concern is local vapour locks in the system which would inhibit the cooling of certain areas of the detector.

2. In an open loop system [27, 37] the evaporation takes place directly at the VLSI chip. This minimises the thermal resistance. The vapour is transported through the open space inside the detector by flushing air, nitrogen or helium. Some work has been done to make small perforated Silicon membranes used to "dispense" a suitable amount of liquid onto the VLSI-chips. Some first experiments have been done using ladder structures of porous polymeric material. At SI different Silicon test chips have been manufactured for thermal management evaluations. The test chips contain heating elements and temperature sensing elements diffused into the silicon. With these chips the actual chip temperature can be measured. In "open" systems, the greatest anticipated difficulty is that of maintaining a steady flow of liquid fluorocarbon to the packaging of the electronics to be cooled by a spray or mist, or by capillarity through a wick-like medium.

6 Cost Estimates.

Cost estimates are dominated by the cost of the silicon and processing and are to first order directly proportional to the area of silicon.

The figures quoted here are based on the estimates from the RD20 and RD9 collaborations for producing radiation hard detectors and SOI, and on large extrapolations from present day (and area) detectors. At the time of the Evian General Meeting on LHC physics and detectors (March 1992) [40], the SITV was estimated to cost 24 MSF. Since that time, we have begun to consider the costs in more detail, and have made the distinction between "material" or "industrial" costs - including detectors, structures and front-end readout electronics, and the support (engineering and technical) needed from the participating institutes necessary to develop, construct and commission the detector.

As a guiding principle, all manpower for industrial products as well as for industrial support is included in the material costs, but no explicit contingency is included at this stage.

Material Costs

Our present estimates are summarised below in millions of Swiss Francs (MSF) and man years of support:

1. Cost of Detectors and Mechanics: **15 MSF**
2. Cost of Front End Electronics : **10 MSF**
   (Excluding Data Acquisition and Slow Control)

Institute Support Required (Man-years)

Our present best estimate is that a total of 300 man years of technical and engineering support from the participating institutes (50/50 electronics/detectors) will be required for the SITV verification, construction, installation and commissioning. Large extrapolations from present detectors make detailed breakdowns unreliable at this time, but we have identified some principal areas where significant support will be required.

Verification

1. Detector Verification;
2. Readout Burn-in;
3. Readout/Detector Bond Tests;
4. Readout/Detector Assembly Testing.

Mechanical Construction

1. Industrial Liaison;
2. Component Inspection;

3. Trial Assembly;

4. Trial Assembly Initial Survey;

5. Cooling System Development, Assembly and Leak Checking.

Installation & Commissioning

1. Cable Routing (Detector Level) and Planning;

2. Cable Routing (Experiment Level) and DAQ Integration;

3. Mechanical Structure: Final Assembly;

4. Mechanical Structure: Final Assembly Layer-by-Layer Survey;

5. Mechanical Structure: Detector Integration & Final Installation;

6. Mechanical Structure: Final Post-Installation Survey;

7. Final Assembly and Installation Clean Rooms and Facilities;

8. Fabrication & Assembly of Installation Tooling.

7 Conclusions

This paper has described the motivation for an SITV for ATLAS. At this stage a general concept has evolved, technological R & D programmes have been initiated, but much remains to be done before a design can be considered optimised.

Obvious (and very productive) areas for continued development remain both within the DRDC collaborations, and within the ATLAS community. Particular examples of necessary continued development are:

1. Radiation resistant detector and front end readout electronics;
2. Sparse scan pixel readout electronics with time-stamping;
3. Cooling technologies;
4. Stable mechanical structure and alignment;
5. Data acquisition.

While 1. and 2. are strongly supported within DRDC programmes, 3., 4. and 5. will need significant support within ATLAS. The three cooling technologies of 3. (liquid, gas, evaporative) must continue to be studied, though each has hitherto indicated a different mechanical construction and different distribution of introduced material. A decision can only be taken after full-scale detailed simulation studies and prototyping. It is planned that the studies of these technologies will continue in their originating institutes, with continued fruitful exchange of ideas and information within the SITV group framework: indeed the final solution adopted may contain elements of more than one cooling technology.

Such a large system of silicon detectors requires a detailed system-engineered study to understand problems such as the design of individual detector modules which must be fully tested and measured, then installed and aligned but must still be exchangeable. The overall structure must be maintained with a stability of the order of 10 μm with the minimum amount of additional material. Thus the careful planning of distribution of power lines and signal cables (which will not only introduce more material but could also give pickup problems and/or unwanted motor forces at the large currents involved) is essential. These problems are all under study, and will increase their demands on our ingenuity during the immediate future.

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Figure Captions

Fig (1) The Two ATLAS Inner Tracker Configurations.

Fig (2) The ATLAS Preferred Silicon Inner Tracker and Vertex Detector Geometry.

Fig (3) Impact Parameter Resolution (μm) and Radiation Dose (Mrad/year) for an Innermost SITV Detector Layer at Various Radii from the Beams at LHC (L = 2 10^{34} $cm^{-2}s^{-1}$).

Fig (4) Effective Cylindrical Area of a SITV Detector as a Function of Rapidity Acceptance.

Fig (5) The material in equivalent radiation lengths for three ATLAS SITV geometries under consideration, as a function of η: (a,b & c) from refs [6, 35, 31] respectively).

Fig (6) Sparse data scan, analogue data buffer and time-stamping readout for pixel detector, as being considered in the RD19 collaboration.

Fig (7) Possible layout for a conical surface pixel detector (48 wafers) for the upgrade to the very forward region of the DELPHI microvertex detector.

Fig (8) A possible SITV front-end readout architecture, using Switched Interconnections of Parallel Processors (SWIPP's: [17]) and optical fibre data transfer.

Fig (9) A possible complete SITV readout architecture using SWIPP's: showing detector module clustering and data sparsification via local Level 2 trigger processors [17].

Fig (10) Pulse height spectra from 70 GeV/c pions, in (a) the Sheffield GaAs *pin*, (b) SB4, (c) SB3, (d) TelettraII, (e) SB5 and (f) Modena GaAs detectors.

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Fig (13) Variation of ϵ_c with reverse bias for a Modena GaAs detector.

Fig (14) Pulse height distribution from the TelettraII GaAs detector after 10^{14} n/cm^2.

Fig (15) Quarter view of the SDC Silicon Tracking System.

Fig (16) Baseline Mechanical layout of the SDC Silicon Tracking System.

Fig (17) Cracow proposal for an SITV detector geometry for ATLAS using nested ellipsoidal arrays of microstrip detectors for a coverage of $\pm$ 1.5 units of pseudorapidity.

Fig (18) CPPM proposal for an SITV detector geometry for ATLAS using cylindrical and conic detector surfaces for a coverage of $\pm$ 2 units of pseudorapidity. The structure is of beryllium, optimised to minimise material at all η.

Fig (19) The proposed carbon composite support shell structure of the Cracow geometry.

Fig (20) The open construction of the silicon microstrip wafers in the Cracow geometry, to allow cooling by forced gas convection.

Fig (21) The principle of operation of a heat pipe, and Results of Conductivity Measurements.

Fig (22) Test Results Obtained at CPPM for Cooling a Simulated Double-sided Silicon Microstrip Wafer with a Heat Pipe.

Fig (23) Test Results Obtained at CPPM for Heat Pipe Cooling a Simulated Silicon Pixel Detector Wafer.

Fig (24) The possible use of heat pipes to aid the cooling of silicon detector wafers. The evaporative ends of heat pipes are in contact with the electronics to be cooled, and the condensive ends are in contact with the cooling liquid channels.

Fig (25) The results of finite element analyses and cooling measurements for a double-sided silicon microstrip wafer in a stream of gas.