



PCS
A solution for
the phase calibration of
the Monitored Drift Tubes
in ATLAS

The Phase Calibration System (PCS)
proposed in this paper does not need
precise cut cables or extensive calibration
of components before or after installation.
It is inexpensive and fault tolerant.

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Phase Calibration

For the Atlas muon detector the required momentum resolution restricts the errors allowed in the time-measurement to approximately 500 ps. This means that correction factors have to be determined that enable the event reconstruction from the TDC measurements in respect to the actual beamcrossing, within this accuracy. This is called phase calibration.

The TDC¹ used has a resolution of 0.78 ns. This means an error of $0.78 \text{ ns} / \sqrt{12} \approx 225 \text{ ps}$ RMS. The system calibration should therefore have approximately the same accuracy. We use the following figures:

- Systematic error 250 ps max.
- Statistical error 250 ps max.

For the phase calibration we split the problem in two parts. We calibrate the channels so that we know their relative errors. That is from the wire up to the read-out of the TDC. This relationship includes the following:

- Differences in the ASD² channels,
- Differences in the TDC inputs,
- Differences in the clock-phases of the TDCs.

Systematic errors are introduced by the interconnecting traces on the PCB from the MDT connection to the ASD input. These can be calculated (and measured), thus reducing their influence. By analyzing the measurements off-line, the systematic errors can be reduced further.

The phaseshift of the electronics in respect to the beam-crossing can only be determined off-line. That should be possible by comparing reconstructed tracks to the beam-crossing pattern. The gaps in the beam-crossing pattern are essential in this reconstruction.³

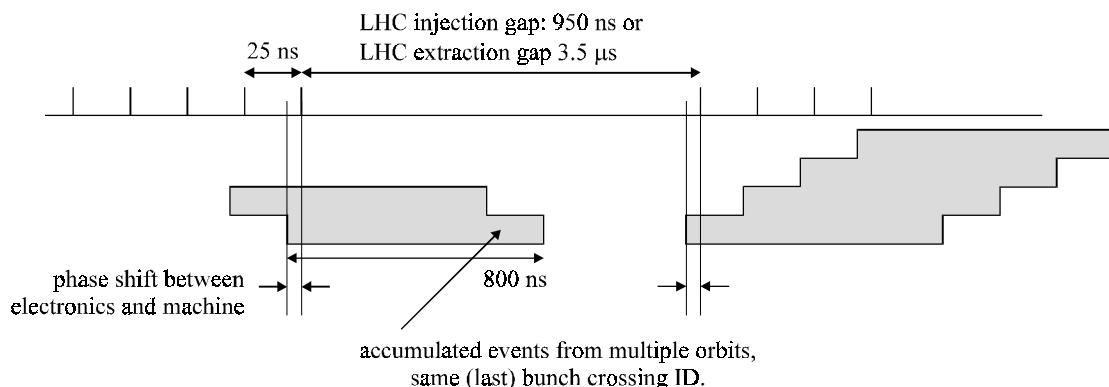


Figure 1

The problem is to build a system that is precise, not expensive and tolerant on defects. How this may be solved, is described hereafter.

¹ 32 channel TDC, Christiansen CERN/ECP

² Amplifier, Shaper Discriminator.

³ See: A Study of Auto-calibration for ATLAS MDT System, by Z.Y.Feng and T.Zhao

Principle

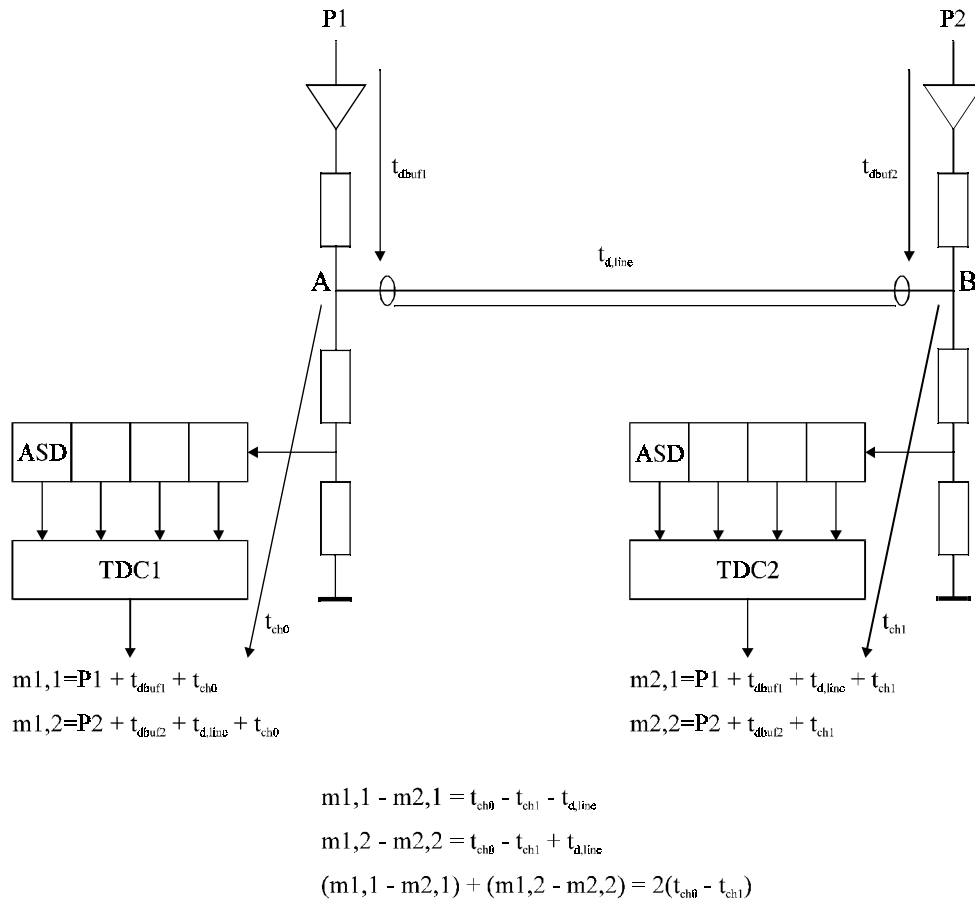


Figure 2

Two FEBoards are shown here and the P1, P2 pulses come in from a distribution system. P1 is pulsed at an arbitrary moment. From point A there is a passive distribution to the ASD chips using terminated 100 ohm lines. Using statistical methods⁴ we can find the relationship between the 32 channels in TDC1. Just their relative differences, not in respect to the LHC clock.

Via the interconnecting cable (A-B), the pulse from point A also drives TDC2. We can compare the results from TDC1 and TDC2. We know the relative phase-differences between the channels in two TDCs now. The unknown factor is the interconnecting cable.

When we pulse P2 we get a new set of timing relations. The pulse travels in the other direction (B-A). By subtracting these data sets, we can eliminate the delay of the cable. In this way we can create relations between two interconnected cards, without knowing the delay in the buffers or the interconnecting cable.

⁴ The single measurement error of ≈ 250 ps is reduced by the square root of the number of measurements.

Extending the system

The system can be extended by giving each FEBoard two drivers. More than two pulses are needed to drive the whole system. This is shown in the numbering P1, P2 and P3. Cards close to each other cannot be pulsed at the same time, since the pulse ripples through the passive distribution system. The values in the picture give an indication of this ripple through when P3 is pulsed. A provision may be needed on the FEBoards to suppress this. E.G. Boards that are not pulsed could short-circuit the ASD input.

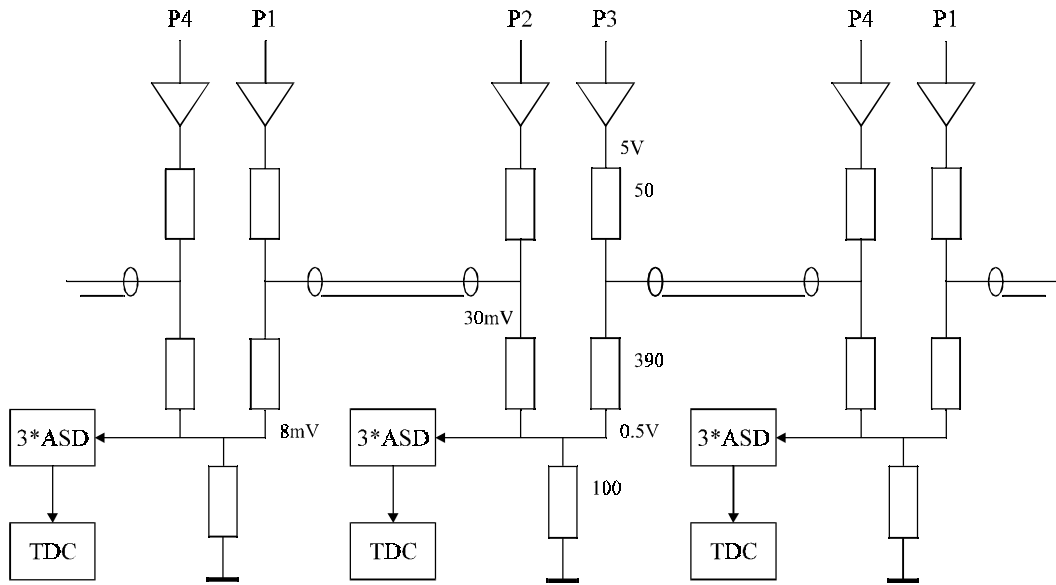


Figure 3

Using this scheme, a long chain can be build. The measurement errors are small since the pulses used are not related to the TDC's clock and many pulses will reduce the statistical error. Nevertheless, building a long chain, will increase the RMS error. Either the initial error must be small, requiring a lot of pulses and generating a lot of data, or the length of the chain must be limited. Furthermore, a long chain is rather vulnerable to defects, such as a connector problem. Therefor a different scheme is used.

Breaking the chain

More than two pulses can be connected to a FEBoard. This gives the possibility to make some 'cross-connections' to build a bigger system, avoiding the drawbacks of a long chain. To build a more flexible system, the pulse distribution is not directly wired. Using a separate selector, one pulse for the whole system would be enough. JTAG could be used to make the selection and enable/ disable a particular driver. A very flexible system can be build this way. For reasons of speed and redundancy, more than one timing pulse should be used to drive the system.

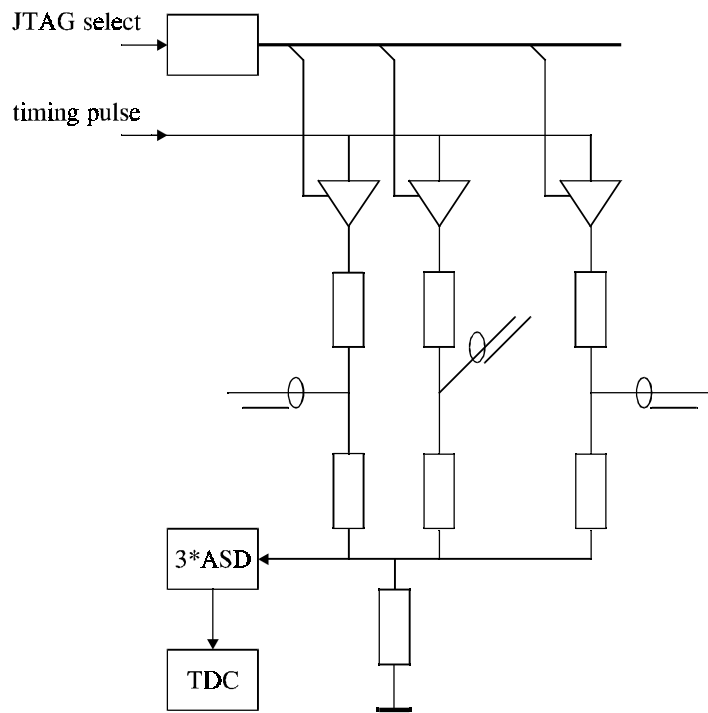


Figure 4

Now a scheme is needed to interconnect a complete tower or even the complete detector.

Tower wiring

Since we do not introduce systematic errors using the interconnecting cables, these do not need to be extremely short or of equal length. So FEBoards on a chamber can be interconnected and then chambers are interconnected at a few points. The figure below shows an example of such a scheme in a tower. Each square represents a FEBoard. Using the loose ends on both sides and some other points, towers can be interconnected in Φ and Θ . The interconnection scheme has to be studied further.

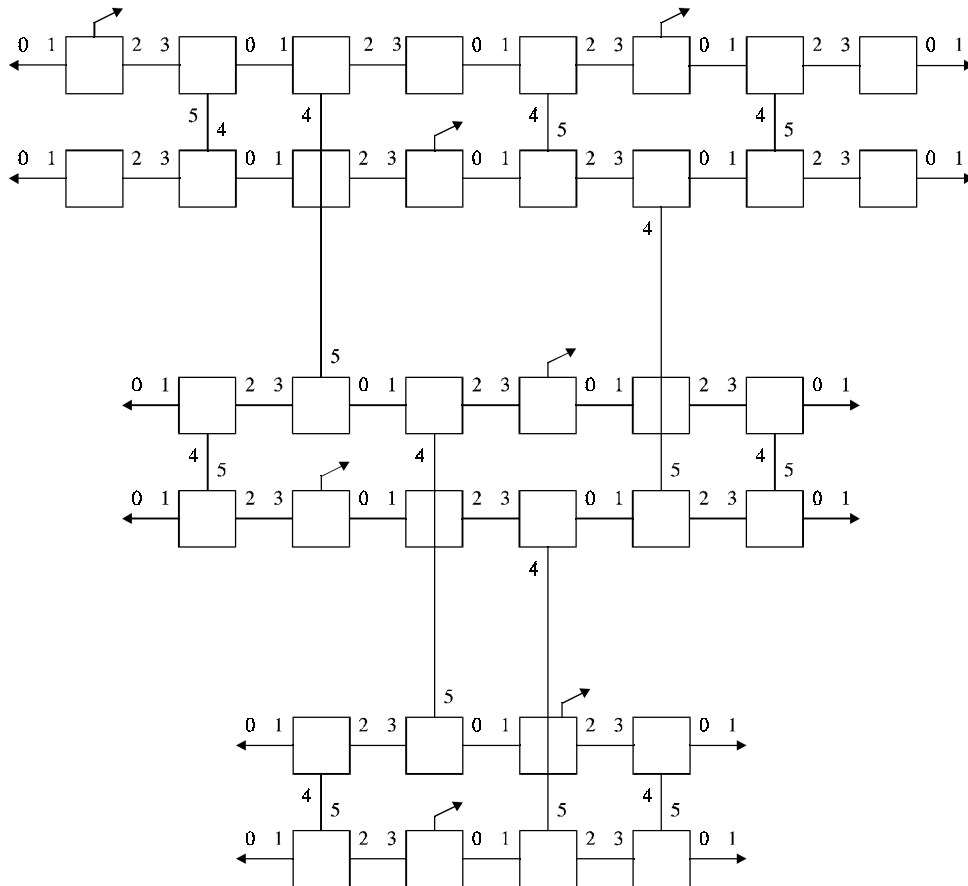


Figure 5

The numbers in the figure indicate the points that can be driven simultaneously if the ripple trough in the passive distribution scheme is low enough to be neglected. Values of the ripple trough are given in a later section. But using JTAG to enable the pulse drivers ensures a flexible scheme. To be on the safe side, more than one inactive card should be located between two simultaneously pulsed cards.

Differential scheme

Using coaxial cable for the interconnections is very expensive. A logical step is to use differential signals. For the big (ATLAS) system it even works better. It generates less noise and is less susceptible to common mode noise. The ASD chip is already provided with differential inputs. Since only one of the ASD's differential inputs is connected to the MDT wire, there is a slight mismatch in the differential termination. This effect can be neglected in this scheme.

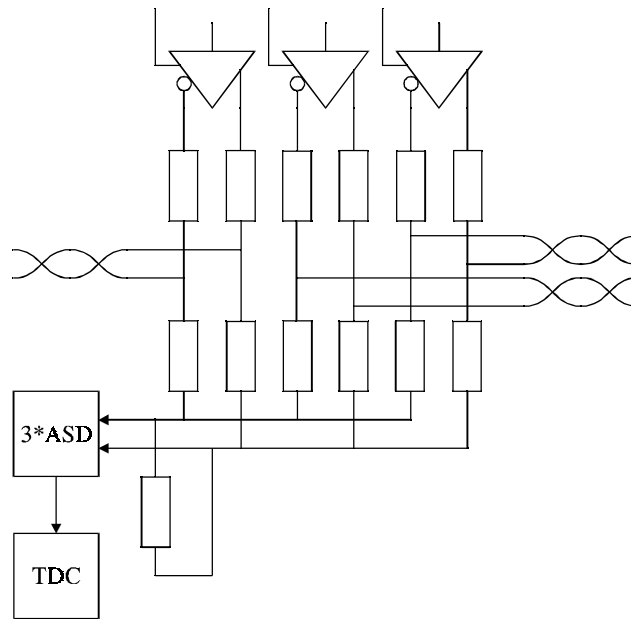


Figure 6

RS422 driver

To get a feeling for the figures, let us have a look at the signals generated by the MDT chambers. A track in the tube generates $\sim 700 e^-$. About 200 of these primary electrons contribute to the signal development. The gas amplification is $\sim 2 \cdot 10^4$. Because of the ion-tail and the shaping time of the ASD input, the normal signal in the ASD chip is $\sim 0.05 \times 200 \times 2 \cdot 10^4 e^- \approx 32 \text{ fC}$. The ASD test input will have a programmable input capacitance. We assume a 3 bit setting with 8 fC per bit (64 fC max.). With a maximum capacitance of 160 fF (20 fF/bit), a pulse of 0.4 V is needed.

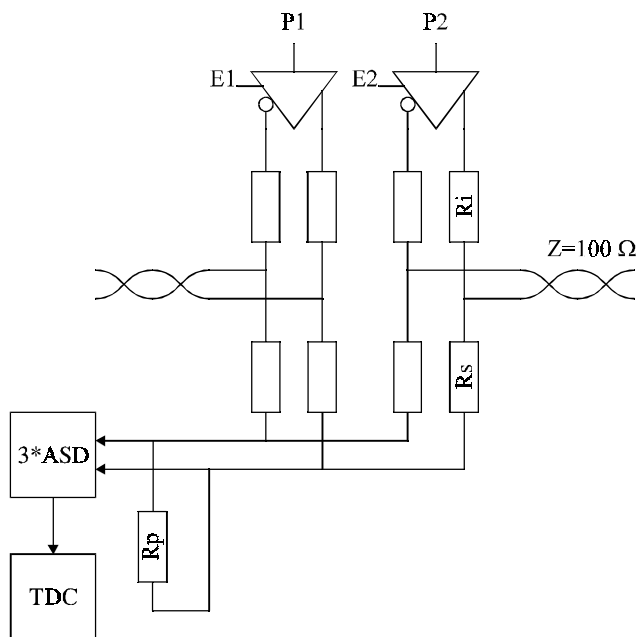


Figure 7

Therefore, the ASD on the other end of the link receives pulses of 66 mV. One link further from the excitation point, the amplitude is reduced to 13 mV. The signal reduces with a factor of 5 after each link.

The resistors R_i are not really needed. They act as the back-termination of the cable, but do not (cannot) have the right value to do so properly. This would only be needed if the other end of the cable is expected to be incorrectly terminated. If this is the case, the line can probably not be used for calibration anyway. They are useful however to reduce the load on the drivers.

For the example two links to other FE-Boards are used. The drivers are RS422 types, generating $\pm 3 \text{ V}$ differential signals. For the resistors we choose: $R_i = 50 \Omega$, $R_s = 33 \Omega$ and $R_p = 47 \Omega$. The impedance at the ASD input is $\sim 33 \Omega$ then. When P1 is pulsed, the P2 driver is disabled. Also the driver on the other end of the link is disabled. The $2 \times R_s + R_p$ on the other end terminate the link. If the drivers could not be disabled, it would be hard to design a properly terminated system. Also the power consumption would be much higher.

The pulses are $\pm 1 \text{ V}$ on the driven link and $\pm 0.33 \text{ V}$ at the ASD input. Unfortunately the link, not driven by its own driver, is still driven with 200 mV.

Practical values

To reduce the ripple-through, the impedance of the R_s - R_p combination should increase. In such a scheme an extra resistor is needed to terminate the cable properly. An other advantage could be that a bigger part of the cable signal can be transferred to the ASD input. The limiting factor here is the fact that the ASD chips are distributed over the PCB (Printed Circuit Board). R_p is used to terminate the line. Therefore the differential impedance of the interconnecting traces on the PCB determine the values of R_s , R_p and R_c .

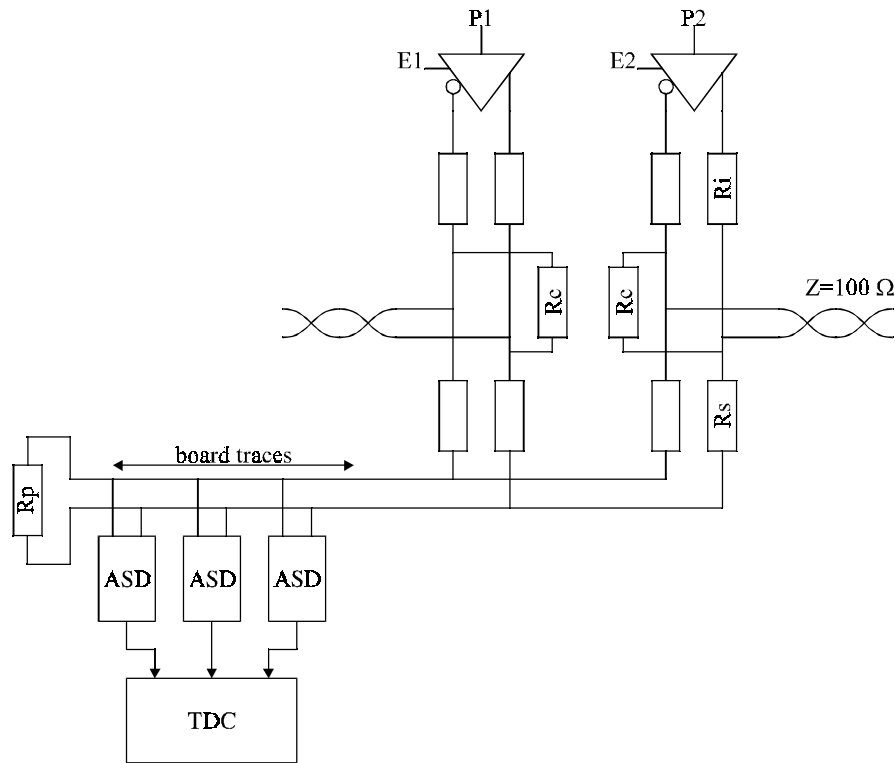


Figure 8

A practical limit for the impedance of a differential line on a PCB is $\sim 100\ \Omega$. R_p terminates the line and must therefore be $100\ \Omega$. Choosing R_s is a matter of the amplitude of the test signal and the ripple through. When we take $100\ \Omega$, R_c must be $150\ \Omega$ for proper cable termination. When $R_i = 25\ \Omega$, the signal on the cable is $\pm 1.5\ \text{V}$. The ASDs receive $\pm 380\ \text{mV}$ and the other cable is driven with $\pm 45\ \text{mV}$. Thus the next ASD receives $12\ \text{mV}$.

The ripple trough can be improved by increasing R_s . If we take $R_s = 220\ \Omega$, R_c must be $120\ \Omega$. The ASDs receive $\pm 230\ \text{mV}$ and the next ASD only $\pm 2\ \text{mV}$.

It must be noted that the differential stripline is not properly back-terminated. This will be solved later.

LVDS driver

Using LVDS drivers for the test pulses would reduce power consumption and radiated noise. In this case too it is necessary to disable the outputs of the drivers not used for the current test pulses. A drawback of this choice is that the amplitude of the pulses are lower (nearly a factor of 10). Therefore the input capacitor in the ASD must be bigger.

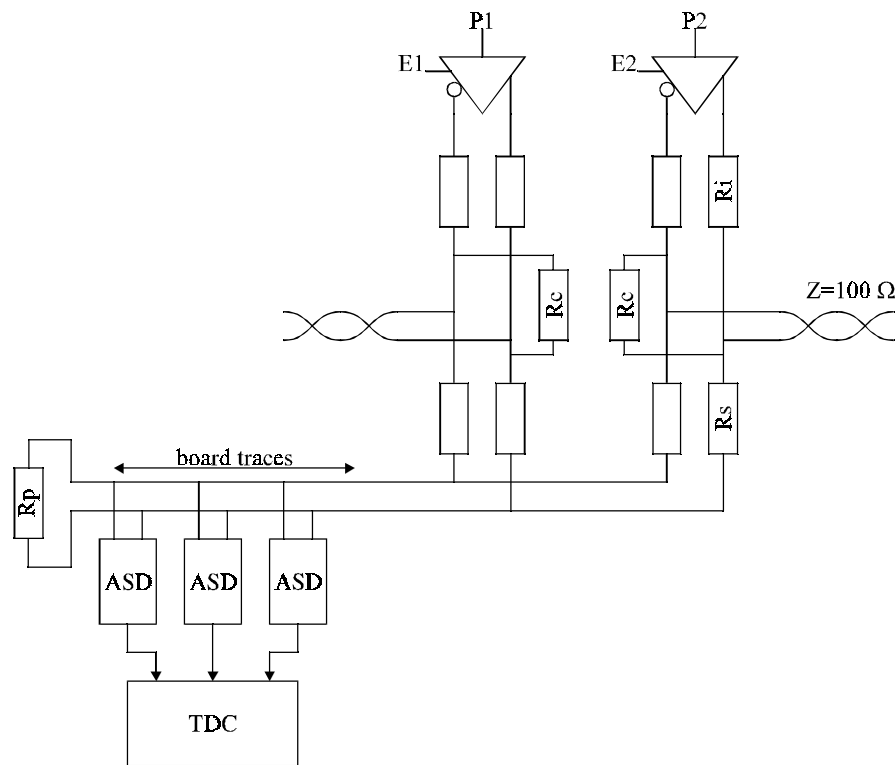


Figure 9

We can use the same resistor values as in the previous example: $R_p = 100 \Omega$, $R_s = 220 \Omega$ and $R_c = 120 \Omega$. The LVDS driver delivers $\pm 4 \text{ mA}$. The cable signal is $\pm 200 \text{ mV}$ then. The ASD gets $\pm 31 \text{ mV}$ and the ripple through to the next ASD is $\pm 0.3 \text{ mV}$. Again a factor of 100 difference in amplitude between the real test-pulse and the ripple through signal is achieved.

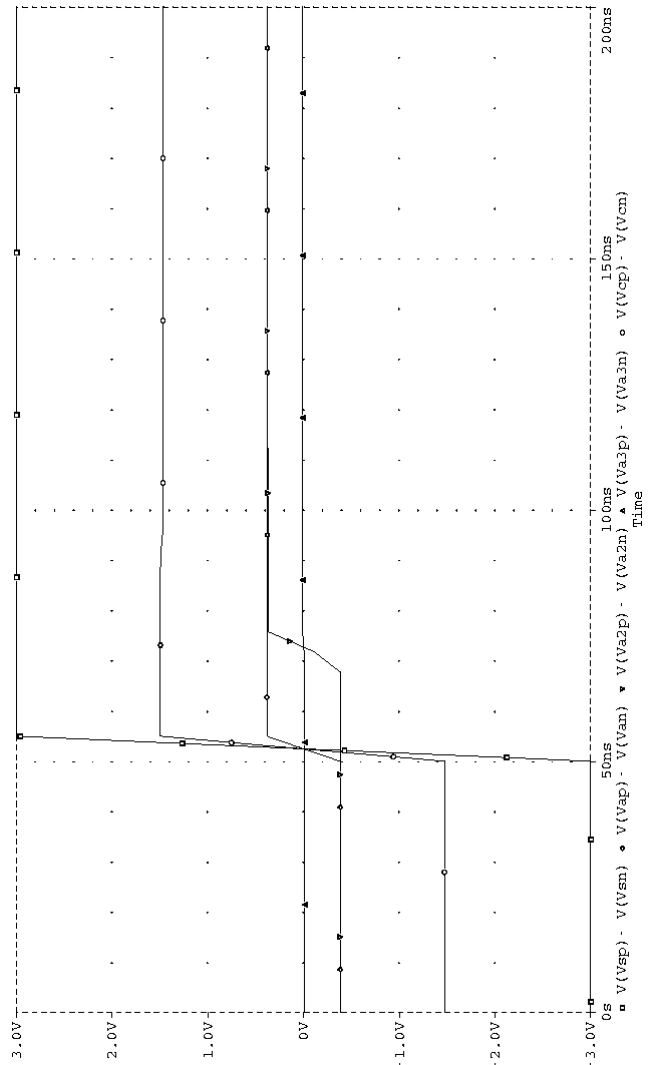
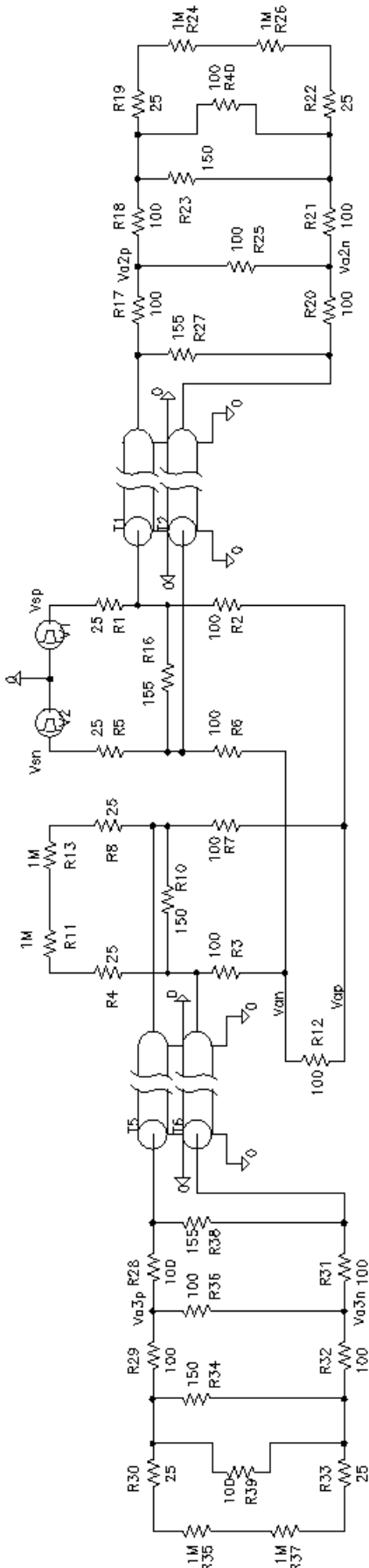
In this case one would choose to increase the signal on the local ASD at the cost of an increased ripple trough. When we choose $R_s = 100 \Omega$, R_c should be 158Ω . The local ASDs receive $\pm 52 \text{ mV}$ and the next ASDs $\pm 1.6 \text{ mV}$.

The LVDS drivers generate a much smaller signal than the RS422 drivers. To inject enough charge into the ASDs, the test-input capacitors must be much bigger. A larger area would be needed for these capacitors, which makes the chips more expensive.

At this moment there are no LVDS drivers available with individual enable lines. So for the moment the choice would be to use RS422 anyway.

Simulations

The values are checked by simulating a simplified scheme. The center circuit is the active driver. On the right is the neighboring FEBoard of which the phase relation is to be determined in respect to the active circuit. Left is a FEBoard receiving the ripple-trough signal. V1-V2 are the differential driver. Disabled drivers are represented by 1 MΩ resistors. R40 and R39 represent the cables to other FEBoards. The ASDs sit in parallel of the other 100 Ω resistors (R12, R25 and R36). The interconnecting cables are represented as delay lines (20 ns), to check for proper termination. The values correspond to the first example on the previous page.



There are small reflections (< 2 %) on the cable because the resistor values are rounded to standard values. The values of resistors and voltages given earlier are proven to be correct.

Figure 10

Different approach

The resistor network can be looked upon as a four-way splitter with internal losses. This is the case for three drivers on a FEBoard.

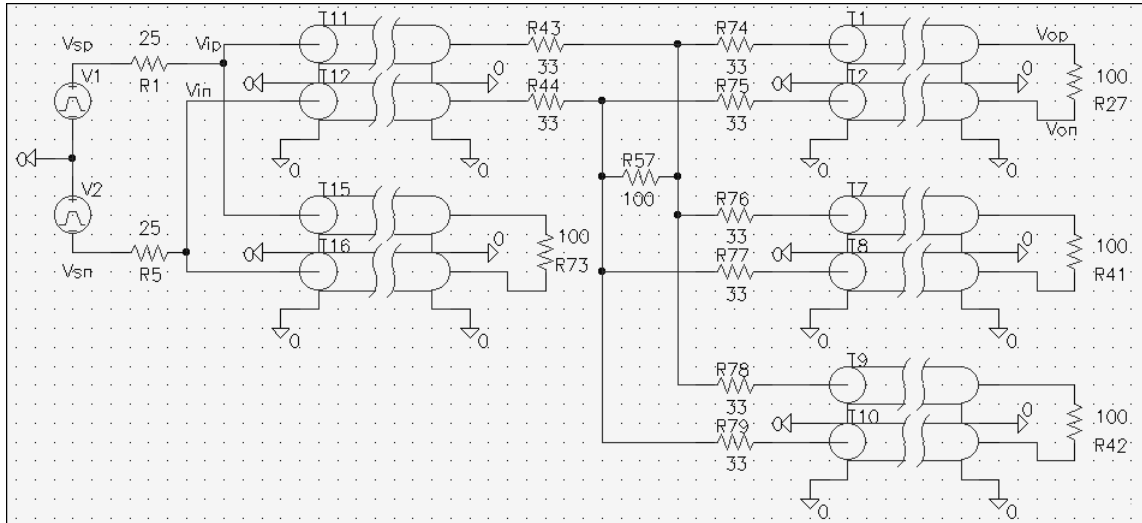


Figure 11

At the left is the active driver. The series resistors reduce the load on the driver. The delay lines ($T11$, $T12$) are used to check for proper termination only. The delay lines $T15$, $T16$ represent the driven cable to the other FEBoard. On the right there are three branches: Two other outgoing 'inactive' lines and the terminated trace on the board. The inactive drivers are not shown. Without the extra resistor $R57$, which introduces the loss, the series resistors must be 25 Ω . The attenuation would be a factor 3. That means that the ripple through is attenuated a factor 3×3 . With $V_i = \pm 1.5$ V, the ASD receives 500 mV and the ripple through is ± 170 mV.

With the values in the schematics above, the attenuation is ~ 4.7 . With $V_i = \pm 1.5$ V, the test-pulse is ± 320 mV and the ripple through is ± 70 mV.

The trace on the board is now properly back-terminated too.

When a fourth driver is added, $R57$ becomes 220 Ω . The attenuation becomes 4.8.

The striplines

Creating a 100 Ω differential line on a multi-layer printed circuit board is close to the upper limit. Higher values are very sensitive to manufacturing tolerances. The strips should be on an outer layer. When the dielectric thickness is 0.4 mm, the strips must be 80 microns in width and 400 microns apart.

The ASD inputs are a capacitive load to the striplines. Though the capacitor value is low, we must be careful not to introduce reflections on the board since they will change the rising edge of the calibration signal. In the scheme below, the board traces are simulated by 0.5 ns delay lines. The 10 pF capacitors form the (pessimistic) input capacitance of the ASDs. The 60 fF is a single test input. The amplifier is assumed to have an input impedance of 300 Ω.

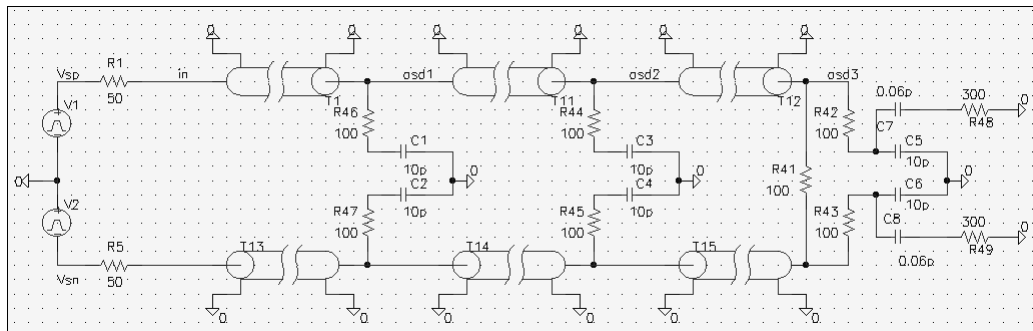


Figure 12

Two simulations are shown below. In the first simulation the series resistors are 1 Ω, in the second case they are 100 Ω as in the above schematic.

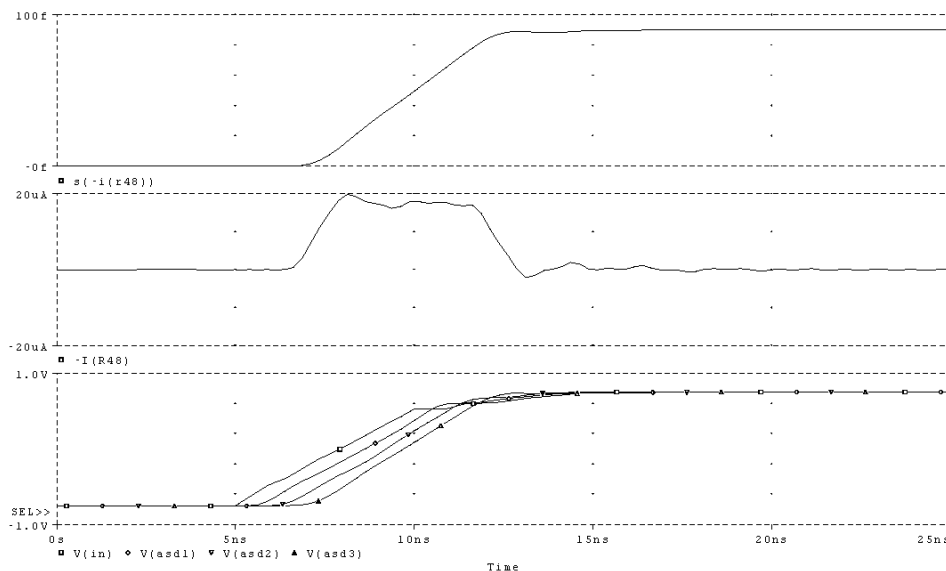


Figure 13

The bottom trace shows the voltages at the beginning of the line and at the points where the input resistors to the ASDs are connected. Reflections are seen due to the capacitive load. The middle trace shows the current into the ASD test input. The top trace shows how the charge accumulates.

The simulation with the 100 Ω resistors shows a much smoother behavior, as is shown below. These resistors must be placed on the board. Integrating them into the ASD is not easy, since the low values are hard to realize on a chip and have large tolerances.

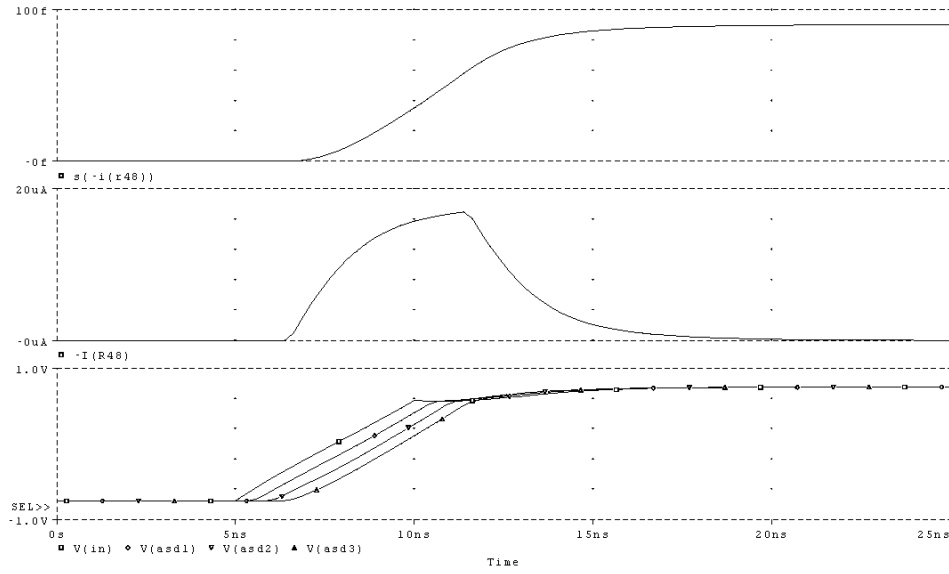


Figure 14

Conclusion

Three drivers on each FEBoard ensure enough flexibility to build a large system. However a fourth driver can be added, at the cost of signal size.

The LVDS drivers generate a much smaller signal than the RS422 drivers. To inject enough charge into the ASDs, the test-input capacitors must be much bigger. A larger area would be needed for these capacitors, which makes the chips more expensive.

At this moment there are no LVDS drivers available with individual enable lines. So for the moment the choice would be to use RS422 anyway.

Small series resistors at the ASD test inputs improve the signal quality and have no influence on the injected charge.

The only parameters that have to be determined before installation are the (difference in) delays of the traces from the MDT tubes to the ASD-chips and the delays of the traces between the passive splitter and the ASDs. These values can be calculated beforehand and checked by measuring them on the actual board. They will be very stable.