Electrical performance of ATLAS-SCT KB end-cap modules

M. D'Onofrio, A. G. Clark, M. Donegà, D. Ferrere, M. Mangin-Brinet, B. Mikulec, M. Weber

[a] *D.P.N.C., University of Geneva, Switzerland*

Y. Ikegami, T. Kohriki, T. Kondo, S. Terada, Y. Unno

[b] *KEK, High Energy Accelerator Research Organization, Japan*

H. Pernegger, S. Roe, R. Wallny

[c] *EP Division, CERN, Geneva, Switzerland*

G. F. Moorhead, G. Taylor

[d] *University of Melbourne, Australia*

J. E. Garcia, S. Gonzales, M. Vos

[e] *IFIC, CSIC-University of Valencia, Spain*

B. Toczek

[f] *Cracow FPNT, Poland*

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Abstract

The Semiconductor Tracker (SCT) is one of the ATLAS Inner Detector elements which aims to track charged particles in the ATLAS experiment. It consists of four cylindrical layers (barrels) of silicon strip detectors, with nine disks in each of the forward and backward directions. Carbon fibre structures will support a total of 4088 modules, which are the basic functional sub-unit of the SCT. Each module consists of single sided silicon micro-strip detectors glued back to back with a 40 mrad stereo-angle, and attached to a hybrid. The scope of this document is to present the electrical performances of prototype end-cap modules proposed for the ATLAS-SCT, as an alternative to the baseline [1]. The layout of these modules is based on the implementation of the barrel module hybrid in the end-cap geometry. A complete set of electrical measurements is summarized in this paper, including irradiated module tests and beam tests.

1 Introduction

The silicon microstrip detector system (SCT) [2] of ATLAS experiment consists of four cylindrical layers (barrels) of silicon strip detectors, with 18 disks in the forward and backward direction, allowing for charged particle tracking up to a pseudorapidity of +/-2.5. Each barrel and disk is equipped with modules of silicon detectors which each contain 1536 read-out channels. A module is the basic functional sub-unit of the ATLAS SCT. It consists of a set of single sided silicon micro-strip detectors glued back to back, an electronics hybrid which carries twelve ABCD read-out chips [3], and an interface to the cooling and mechanical support structure of the tracker. The SCT barrel modules have been shown to satisfy the electrical, thermal and mechanical requirements of the SCT [4]. However, the four first hybrid versions foreseen for end-cap modules showed unacceptable instabilities of some chips, particularly towards the outer edge of the hybrid, and extensive reworking requirements that were not consistent across the fabricated modules. The possibility of building an end-cap module based on the barrel hybrid – therefore named "KB", assembled in an end-tap configuration with the forward detectors, was therefore considered by some institutes of the collaboration.

A first prototype (later called b048) was successfully built in September 2001, followed by eight other outer modules in a final design configuration, assembled and fully tested. These included two irradiated modules, one of these latter being used for thermal tests only [5]. The module layout and particularities of its design are detailed in [6], together with the different assembly steps. In this paper we focus on the results of electrical tests performed on these KB modules. The first section is devoted to the summary of electrical requirements for SCT modules and the description of the set-up used for electrical characterization. The results of standard electrical tests for non irradiated and irradiated KB modules are detailed in respectively section 3 and 4. Section 5 is devoted to test beam results.

2 Standard Electrical Tests of Modules

2.1 Electrical requirements for the ATLAS-SCT end-cap module

The performance of the modules are matched to the demands at the LHC, both high interaction rates and high levels of background radiation. The complete end-cap module electrical specifications are given in [2] and only the most important ones are summarized below:

- The equivalent noise charge (ENC) for the front-end system, including the silicon strip detector attached to the hybrid, should be less than 1500 e- ENC for non irradiated modules, and less than 1800 e- ENC for irradiated ones. However, the total effective noise results not only from the front-end electronics contribution, but also from the channel-to-channel threshold matching. It can be parametrized as the addition in quadrature of this ENC for the front-end electronics with the contribution of the channel-to-channel threshold spread.

- The noise occupancy is required to be significantly less than the real hit occupancy to ensure

that the noise hit rate does not affect the data transmission rate or track reconstruction. The foreseen noise occupancy limit of 5×10^{-4} requires that the discriminator level in the front-end electronics is set to 3.3 times the rms noise.

To achieve this condition at the foreseen ATLAS operating threshold of 1 fC, the total equivalent noise charge should never be greater than 1900 e- ENC: assuming 3.3 fC median charge, that corresponds to a median signal-to-noise ratio of 10:1.

- To minimise the data to be read out and to simplify tracking, each hit has to be associated with a unique bunch crossing. The silicon charge collection time of 10 ns therefore requires edge-sensing discriminators with a maximum time walk of 16 ns for the nominal threshold settings and full range of input signals. The fraction of outputs shifted to the wrong beam crossing is required to be less than 1%.

- The double pulse resolution, which directly affects the efficiency, is required to be 50 ns, to ensure less than 1% data loss at the highest design occupancy. Thus, the detection of two tracks that are incident on the same strip is possible providing the separation time is at least two bunch crossings.

The modules are checked to satisfy these challenging performance requirements during the electrical characterization procedure, which is performed using a data acquisition system developed for the ATLAS SCT [7].

2.2 Set-up description and characterization tests

In all the measurements performed, the ASICs are powered with the prototype SCT low voltage power supply [8] (SCTLV3) and read out electrically via an SCT CLOAC-MuSTARD-SLOG system widely used in the SCT community to test modules. A schematic drawing of the set-up is shown in figure 1. This set-up contains:

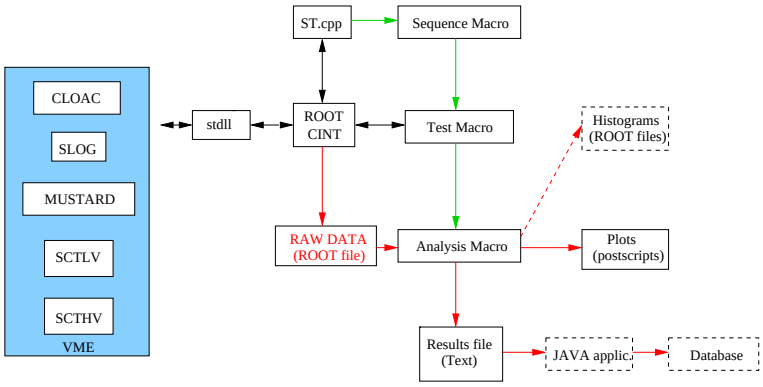

Fig. 1. Schematics of the SCTDAQ system.

- The MuSTARD [9] (Multichannel Semiconductor Tracker ABCD Readout Device), which is a VME module designed to receive, store and decode the data from multiple ATLAS SCT module systems.

- The SLOG [10] (SLOw command Generator), which allows the generation of slow commands for the control and configuration of ATLAS SCT front-end chips.

- The CLOAC [11] (CLOck And Control) module, which generates the clock, fast trigger and reset commands for the SCT modules, in the absence of Timing, Trigger and Control system.

- A prototype high voltage unit (SCTHV) [12] used to bias the sensors.

A software package – called SCTDAQ – has been developed for testing both the hybrids and the modules, using these VME units. It consists of a C++ compiled dynamic link library and a set of ROOT [13] macros. The methodology of each test implemented in SCTDAQ and the subsequent data analysis are described in [7].

To determine the front-end parameters of the modules, an internal calibration circuit that simulates a charge input is implemented in the ASICs. The gain and the noise for each channel are measured by performing threshold scans for different input charges and for each channel of the chips. A complementary error function is fitted to each threshold scan to yield values of 50% point efficiency (vt_{50}) and output noise for each channel. A multi-parameter fit to a set of vt_{50} points is used to obtain the response curve from which gain and offset for each channel are determined. The input noise is thus calculated by dividing the output noise measured at 2fC by the calculated gain.

Before any gain or noise measurement, a trimming procedure is performed in order to compensate channel-to-channel variations of the discriminator offset. Each channel can be addressed individually and is provided with a trim DAC of 4-bit resolution. The threshold correction can thus be applied channel by channel. For the trim DAC characterization, a scan for each electronic channel and for a fixed calibration pulse is performed. Applying the same analysis described as for the gain and offset measurement, an overall characterization of the trim DAC is obtained. During the trimming procedure, certain channels, which are either too noisy or stuck or with too low gain, are masked from the read-out on the ASIC.

3 Performance of non irradiated modules

For the non irradiated modules, the measurements have been performed with a minimal cooling, that is a chiller, providing a liquid coolant at $+15^oC$, which corresponds to a temperature on the hybrid [1] between 28 and 35^oC. The KBs were mounted in a dedicated test box (Al frame) that supports both ends of the module and cools it along its AlN facing at the rear with a cooling contact of $\sim 78\times8\text{mm}^2$.

Two types of corrections have to be taken into account to compare modules with each other. First, the amplitude of the calibration pulse issued by the ASICs needs a correction factor (referred below as "calibration factor"), that takes into account variations from the design value of the calibration capacitor on the front-end. To determine this variation, indirect measurements of this capacitance are performed by measuring the oxide thickness of the capacitor, and then

[1] the hybrid temperature is monitored by two thermistors glued onto the hybrid.

by comparing it to the nominal value. Five measurements by wafer are made and the correction factor is then deduced from the mean value of these tests. Table 1 shows the correction factor (C.F.) that must be applied in order to compare modules with each other. The real (corrected) gain and noise ENC are then given by:

$$\text{Real gain} = \text{Meas. gain}/\text{C.F.}; \qquad \text{Real ENC} = \text{Meas. ENC} \times \text{C.F.}$$

Module	*Cal. factor*	*Module*	*Cal. factor*
KB 048	1.13	KB 104	1.12
KB 100	1.12	KB 105	1.167
KB 102	1.13	KB 106	1.167
KB 103	1.13	KB 108	1.12

Table 1
KB calibration factors

On the other hand, the noise values have to be normalized to a given temperature. Evaluations of the SCT cooling system have led to an expected temperature on the baseline module hybrid of about 2^oC. Even if the extrapolation in the KB case is not straightforward, we choose to normalize the KB results to this same conventional value. The noise versus temperature dependence has been measured on two KB modules. As shown in figure 2, the ENC variation is linear with temperature and the correction to apply turns out to be about 5.5 e- ENC/^oC (non corrected for calibration factor) for non irradiated modules. This temperature dependence is similar to the one found for prototype barrel modules [14].

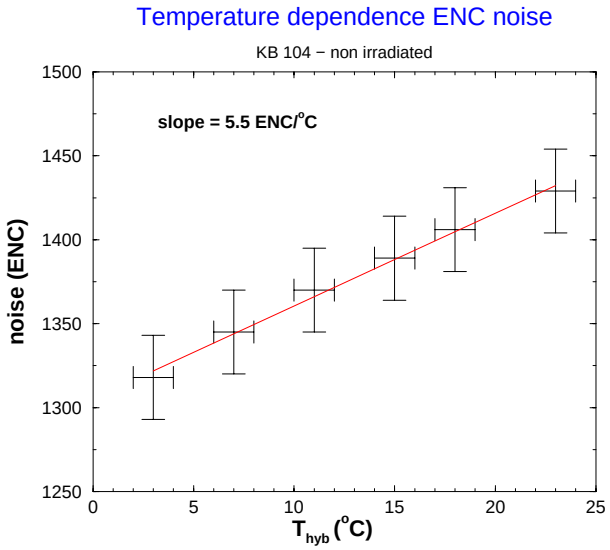

Fig. 2. Temperature dependence of the ENC noise for non irradiated KB 104 and 105. The slope is approximately 5.5ENC/^{o}C, including the calibration factor.

In table 2 the main electrical characteristics of KB modules are summarized, and both measured and corrected values of ENC and noise occupancy are displayed. The noise occupancy correction

was performed by fitting the occupancy as a function of the threshold, by a complementary error function, assuming that the noise is purely gaussian,

$$NO(t, ENC) = \frac{1}{2}\,\mathrm{erfc}(\frac{t}{ENC\sqrt{2}}) \tag{1}$$

where NO, ENC and t are the noise occupancy, ENC noise [2] and threshold values respectively. Inverting this complementary error function leads, for a given value of the noise occupancy, to a value of the ENC noise. This ENC noise is then corrected as specified above, and the corrected noise occupancy is obtained using once more the interpolation (1).

Module	*Gain*	*Thr. spread*	*T*	*Noise (e- ENC)*		*Occ.@1fC* $\times 10^{-4}$		*Masked*
	(mV/fC)	*@ 1fC (ENC)*	*(°C)*	*Meas.*	*Corr.*	*Meas.*	*Corr.*	*Chann.*
b048	48.7	136	28	1410	1450	0.05	0.09	7
KB 100	47.8	138	34	1448	1446	0.11	0.11	3
KB 102	49.0	203	35	1300	1287	0.02	0.02	1
KB 103	48.5	156	33	1416	1430	0.05	0.06	30
KB 104	50.1	170	28	1370	1391	0.04	0.06	1
KB 105	50.9	139	-	1357	-	0.06	-	0
KB 106	50.0	156	30	1380	1430	0.02	0.04	2
KB 108	50.0	138	29	1318	1328	0.03	0.04	13

Table 2
Electrical performance of the non-irradiated KB modules. The values of noise and noise occupancy indicated as *corr* are corrected for calibration factor and normalized to the SCT operating temperature, that is 2^{o}C on the hybrid thermistor. The gain is corrected as well by the respective calibration factors. Note that b048 is the first KB prototype that had been built with a slightly different geometry [6].

The noise occupancy of these modules at 1fC threshold is between $\approx 2 \times 10^{-6}$ and $\approx 10^{-5}$ – that is well inside the required specifications – with a gain of $\approx$ 50mV/fC and a (corrected) mean noise value of 1410 e- ENC. Figure 3 shows the noise occupancy plot of KB 104, together with the response curve and the dependence of gain on the threshold for one chip, representative of the results obtained with KB modules.

No instabilities were observed, as can be seen in Figure 4, where a set of four typical S-curves – superimposed – is displayed. We can note that the number of masked channels is well below

[2] It is worth noticing that this ENC value differs from that obtained by the response curve. The ENC deduced from the noise occupancy includes the contribution of both electronics noise and channel-to-channel variation. It therefore includes the threshold spread.

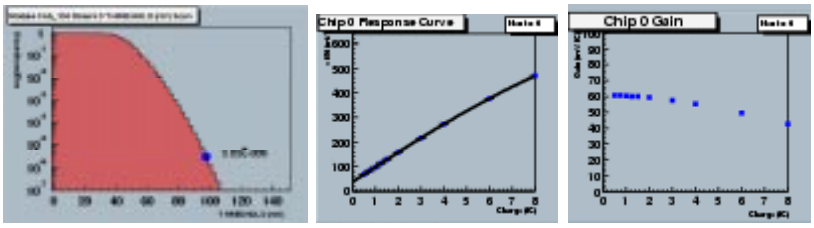

Fig. 3. Typical noise occupancy, response curve and gain vs threshold plots of a KB module.

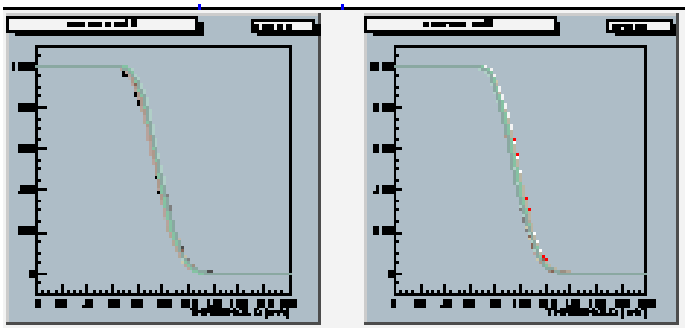

Fig. 4. Example of scurves of an unirradiated KB module: for all single read out channel, a correspondant 0.5 fC charge in mV is injected and a threshold scan is performed. This plot shows S-curves of four channels superimposed.

the 1% level required by the specifications, except for KB 103 for which the bonding procedure happened to be imperfect. In addition to these satisfactory mean values of noise and ENC, figure 5 shows that the ENC noise and the gain are very uniform across the modules, for all the tested KB modules.

Furthermore, the timewalk, not displayed here, is between 10 and 13 ns. The results are thus very satisfactory, and close to the barrel module performance [4]

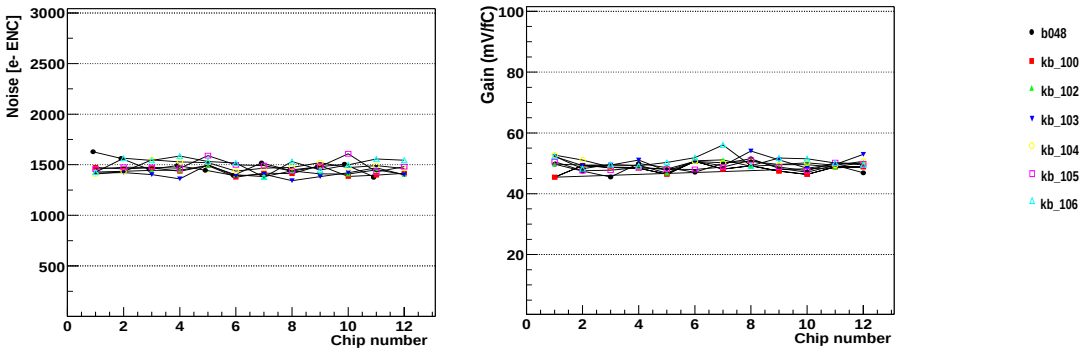

Fig. 5. *(a)* on l.h.s. plot: Measured Noise (e- ENC) distribution per each ASIC for all unirradiated KB modules tested in the same environment. All reported values are corrected for the calibration factor and normalized to $2°C$. *(b)* on r.h.s. plot: Gain distribution per ASIC, corrected with the calibration factor.

4 Irradiated module performance

SCT barrel and end-cap modules are required to remain operational after 10 years of LHC running. The highest accumulated radiation levels expected in the ATLAS SCT are reproducible irradiating the modules with a 24 GeV proton beam at the CERN PS[15]. Irradiation nominal fluence is 3×10^{14} protons/cm^2, distributed on a period of about 10 days. The irradiation is then followed by a 7 days period of annealing at 25 °C.

Radiation damage involves both the ASICs and the silicon detectors. ABCD chips are realized in BiCMOS technology, so they are sensitive to ionization effects as well as to displacement damage[16]. These contribute to a degradation of the current gain factor β of the input transistor, and consequently to an increase in the noise of the front-end; furthermore, offset spread of the discriminator and speed of the digital CMOS part are affected.

Silicon detectors are subject to both surface and bulk radiation damage. The first is mostly due to an accumulation of charges in the interface between silicon oxides and bulk; it affects for instance interstrip capacitance, the main contributor to the parasitic capacitance for the amplifier noise. The bulk is mostly damaged by displacement that leads to an increase of the leakage current proportional to the fluence and the silicon volume. Finally the general effect of irradiation is an increasment of the reverse bias current and of the depletion voltage.

The KB 100 module was irradiated in October 2002. The module was mounted on a plastic cradle and the hybrid was fully powered, while silicon detectors were biased at 100 V. Indications of the temperature conditions were given by thermistors mounted on the hybrid and during the whole period it didn't exceed 25 ^oC . Online tests were perfomed using the standard SCTDAQ test facility, to check the functionality of the ASICs and to monitor occurance of possible failures of chips readout. After irradiation, the module was annealed for 7 days at 25 ^oC monitored temperature, in order to stabilize the detector properties.
The module was subsequently tested in a climate chamber set at -7 ^oC; cold nitrogen was fluxed inside the metal box holding the module (N_2 flux $\simeq$ 1 l/min) and a Huber chiller set at -17 °C was also connected to the box providing a liquid coolant passing below the hybrid. Figure 6 shows a measurement of the leakage current made with the electronics unpowered: at 500 V bias voltage, the value that was used during all electrical tests, the leakage current stabilized around 1500 μA, and increased up to 2600 μA when the ASICs were turned on, due to the extra-heating transmitted by conduction from the hybrid to the detectors.

In addition to the standard electrical procedure described in the previous section, a few more tests are required to optimize the working conditions of the ASICs.

The front-end circuit for binary readout architecture is based on a transimpedance amplifier with a bipolar input transistor: for unirradiated ASICs, the nominal values for collector (preamplifier) and shaper currents are 220 μA and 30 μA respectively. As consequence of the β factor degradation, the optimum values of these currents decrease after irradiation; two 5-bit DAC's implemented on the ASICs permit to change the preamplifier and shaper currents[17] and the working point estimation is made checking different combinations of the two. Each chip can be independently adjusted and typical values found for KB-100 were 120 or 140 μA for the input transistor current, 27 or 30 μA for the shaper bias. This procedure, the so called current

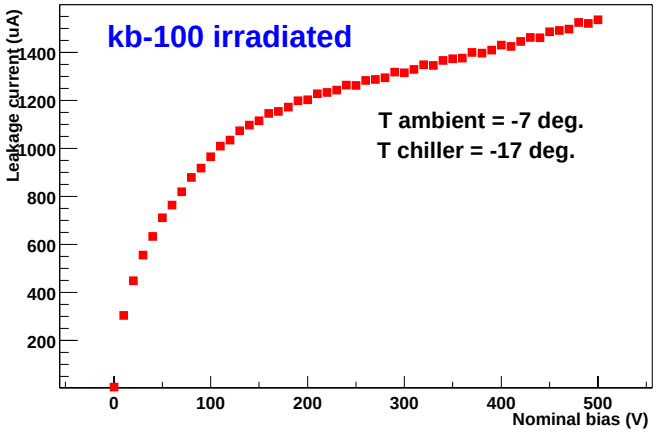

Fig. 6. Leakage current for the irradiated module KB 100 (chips unpowered): the measurement has been performed setting the environment temperature at -7 ^oC (foreseen ATLAS condition) and providing liquid cooling through a chiller set at -17 ^oC (correspondent coolant temperature $\simeq$ -15 ^oC).

scan, was made as the first step of the electrical tests, followed by a standard strobe delay and trimming test. For irradiated modules, the trim procedure is especially important, due to the increase in the ABCD discriminator threshold spread.

Table 3 shows the front-end parameters as measured on the KB module: noise in ENC and noise occupancy at 1 fC have been corrected with a calibration factor of 1.12, supposed to be the same before and after irradiation (no temperature normalization is applied (T(therm.) = +1 $^\circ C$)). In figure 7 the gain and ENC noise distributions across the channels are also presented: the noise is around 1980 e- and the efficiency in terms of number of working channel is $>$ 99.5 %.

A timewalk scan has been performed to evaluate possible degradation in the speed of the ASICs (see figure 8): 10 chips out of 12 are in the specifications, with an average timewalk of $<$ 16 ns, and only one chip on the bottom side having a mean time walk of about 18 ns.

Gain	*Thr. spread*	*T*	*Noise (e- ENC)*		*Occ.@1fC* $\times 10^{-4}$		*Masked*
(mV/fC)	*@ 1fC (ENC)*	*(°C)*	*Meas.*	*Corr.*	*Meas.*	*Corr.*	*Chann.*
30.0	586.0	1	1765	1978	15	40	6

Table 3
Front-end parameters as measured for the irradiated KB module. The occupancy at 1 fC threshold is higher than what is expected from the electronic noise and threshold spread. The measurements were affected by common mode noise due to the fact that they were performed in a very noisy environment (climate chamber) without an appropriate grounding - see also test beam section.

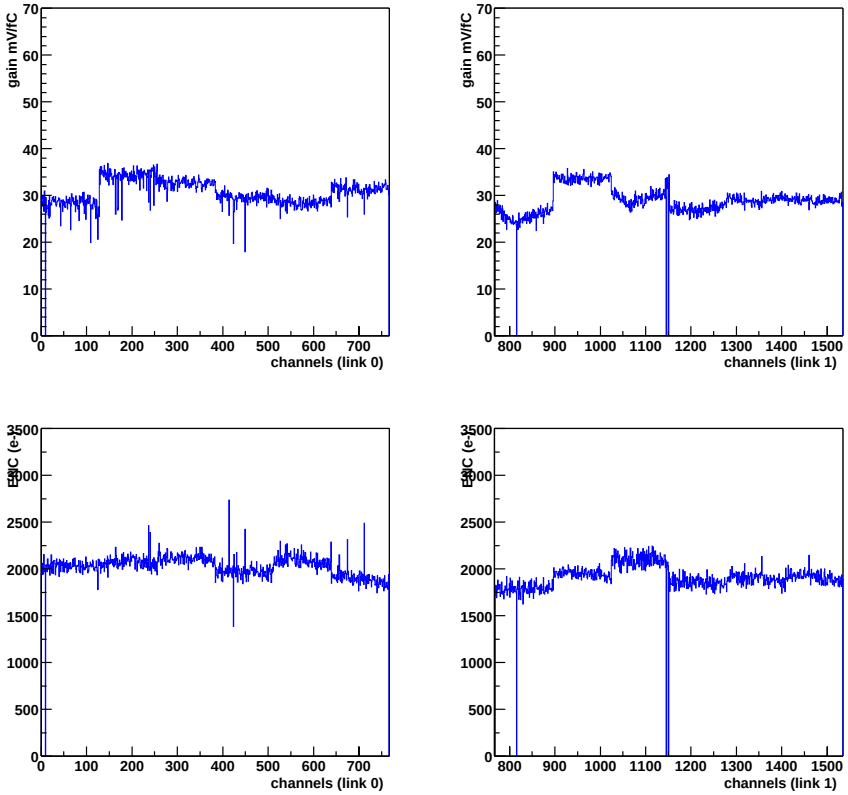

Fig. 7. Gain (on the top) and Noise ENC (on the bottom) distributions across the channels for KB 100 irradiated module: left and right plots refer to the two module sides.

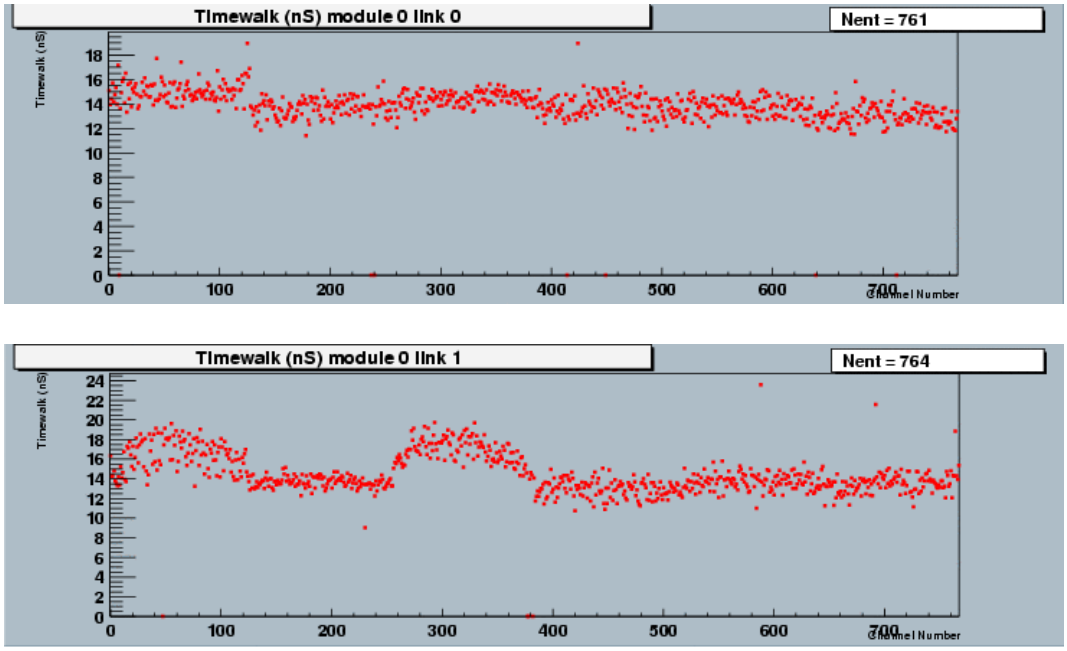

Fig. 8. Timewalk distribution of KB 100 irradiated, for link 0 and link 1.

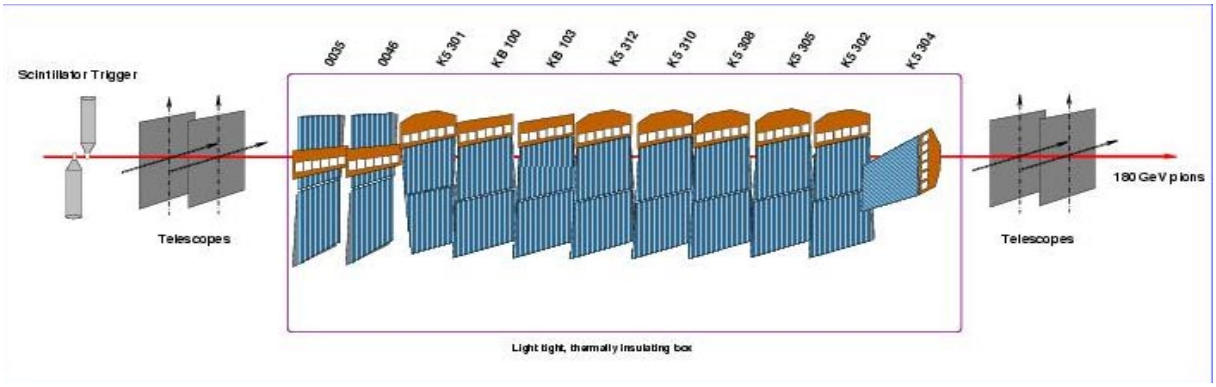

Fig. 9. Sketch of the test beam line of May 2002.

5 Test Beam results

Electrical tests using the calibration circuit and noise measurements enable characterisation of the general module performance, but in order to evaluate the capabilities of the modules as particle detectors, beam tests are desirable. At the ATLAS testbeam facility at the CERN SPS H8 beamline, data collected during 2002 involved KB prototype modules, as well as baseline K5 end-cap and barrel modules (see for more details [18] and [19]).

Figure 9 shows a typical arrangement of the system in the H8 beamline: the collimated beam - usually composed of 180 GeV/c pions with a minor contamination of muons - passes through two trigger scintillators and all the inline silicon detectors. The modules being tested are held in a light-tight and thermally insulated box, fixed to a massive and cooled aluminium base plate: each prototype is contained in its own metal box closed with perspex covers to make safe handling and interventions while minimizing the amount of material and consequent multiple-scattering effects. Active cooling to each module is provided by cold fluid flow into the individual aluminium boxes at the cooling block, with the fluid maintained between -15 and -20C. Humidity is also controlled by flowing cold nitrogen inside the environment chamber.

In addition to the prototypes binary modules, four XY pairs of tracking detectors are installed outside the main box (two upstream, two downstream), forming a silicon telescope system. For each of them, both X and Y sensors have 50 μm pitch, 640 strips per plane and are coupled with VA2 analogue readout chips with a 1 μs peaking time. The scope of the telescopes is to find tracks with a precision of few microns, in a coordinate-space independent from the under-test module rotations or translations; the conventional SCT test beam analysis is in fact based on the comparison between the real module response and the *predicted* track position, extrapolated from the telescopes.

The DAQ system used in the testbeam is the standard SCTDAQ setup, composed of VME control, read out, low voltage and high voltage power units. The software is an extension of the electrical testing system to handle synchronized beam triggers, and to perform event building and data recording.

Modules are usually calibrated in-situ just before each test beam period, using the internal calibration circuit of the ABCD chips: during this operation bad channels are identified and

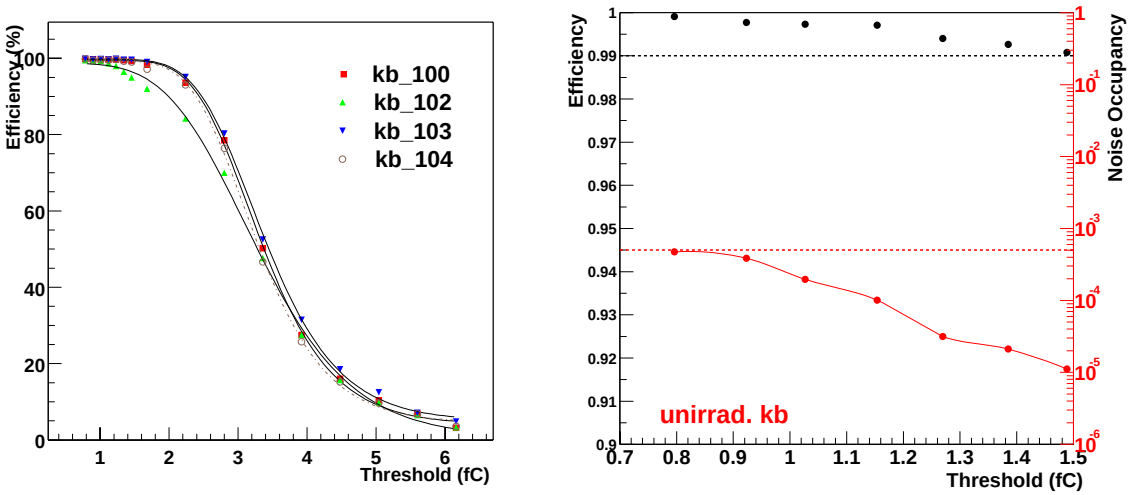

Fig. 10. *(a)* on l.h.s. plot: Efficiency vs. fC threshold curves for all the KB modules in 2002 test beam period. *(b)* on r.h.s. one: Example of single module efficiency and noise occupancy vs. threshold: the dashed lines indicate required specifications at 1 fC for both quantities.

excluded from the acquisition. The effect of masking channels is an efficiency loss of the single planes, less then 0.5 % for the unirradiated KB modules. For this reason, the results presented in this section are based on the analysis of good channels.

The basic measurement of the testbeam has been adapted to the binary readout electronics of the SCT, consisting of a scan of the input discriminator threshold in the range 0.7-6.0 fC. Around 20,000 events are acquired at each threshold point resulting in an efficiency s-curve. The deposited median charge is the extrapolated threshold value with an efficiency of 50 %: a combination of median charge ENC noise extracted from in-situ calibration gives the expected signal-to-noise ratio. Figure 10 (b) shows a typical S-curve for KB modules measured at 150 V bias voltage: the efficiency is measured as the ratio between the number of hits in the module closer than 120 μm from the track position predicted by the telescope system, and the total number of tracks extrapolated. For all the KB modules tested, the efficiency value at 1 fC threshold is over 99% while the median charge ranges from 3.3 to 3.5 fC.

Noise measurements could also be performed in the test beam: noise events are normally acquired separetly by the signal acquisition, in the out-of-spill period. The dependence of noise occupancy with the threshold for one of the KB module prototypes is shown in figure 10 (a) and table 2 summarizes the results for all the modules. During the test beam, two modules have been affected by an excess of occupancy due to the noise - almost one order of magnitude compared to laboratory performance. A dedicate offline analysis identified this extra noise source as a non-gaussian common mode noise. Further investigations have been performed, showing that a careful grounding connection of the hybrid avoids this sensitivity to noise pick up.
Several bias voltage scans were performed in the range 100 V - 350 V: an example is shown in figure 11, where the efficiency at 1 fC (left) and the median charge (right) at different bias values are reported. Most visible is an initial loss of charge at 100 V (below the nominal value) due to the ballistic effect (see ref. note tb 2000), and a plateau from 150 V up to 350 V.

With a binary read out the signal-to-threshold is maximal when all the charge is collected in a

Module	*Eff@1fC*	*NO@1fC* $\times 10^{-4}$	*Qmed (fC)*	*S/N*	*Plane res.*	*Clus size @1fC*
KB 100	99.7	0.7	3.4	14.2	22.5	1.08
KB 102	99.8	1.2	3.3	13.6	23.0	1.05
KB 103	99.3	1.1	3.3	13.7	22.8	1.1
KB 104	99.7	0.8	3.4	14.8	23.7	1.07

Table 4
The main results for unirradiated KB modules (bias voltage = 150 V): efficiency and noise occupancy at 1 fC, median charge and extracted Signal to Noise, spatial resolution for single plane and average cluster size in units of the strip number.

single strip, so there is a clear dependence between the efficiency and the inter-strip position of the track. Figure 12 (a) shows the efficiency as a function of the reconstructed track position with respect to the two strips: each step in the profile is 7 μm, that is the track resolution of the telescopes. An expected loss of efficiency is observed around the middle inter-strip position, where the charge sharing is maximized and the effective pulse height is decreased: the superimposed curves referred to different thresholds, showing how the effect is visible for a threshold above 1.5 fC, well above the operating value of 1 fC. The average cluster size as a function of the track position between two strips is also a measurement of the amount of charge sharing (see figure 12, where the threshold value is 1 fC): all these results satisfied the expected performance of SCT modules.

The spatial resolution for a single plane is calculated as the difference between the center of the binary cluster and the track position predicted by the telescopes: figures 13(a) and 13(b) show an example of residuals for two planes of an unirradiated KB module, where the resolution is given by the rms of a gaussian fit. The expected value for a 1 strip cluster size event is given by pitch/$\sqrt{12}$ and it is quite close to the obtained value (see table 4). Operating on single plane residuals, the real spatial resolution in XY is showed in figure 13(c) and 13(d).

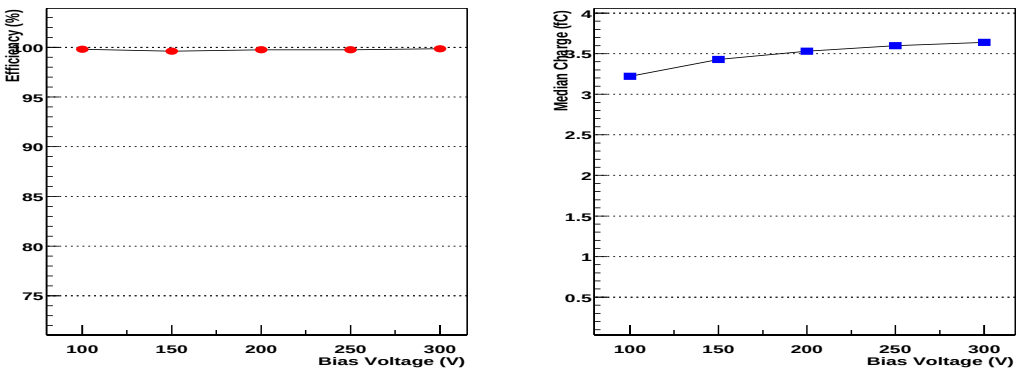

Fig. 11. Efficiency at 1 fC (a) and median charge (b) for a bias scan performed on unirradiated KB 100.

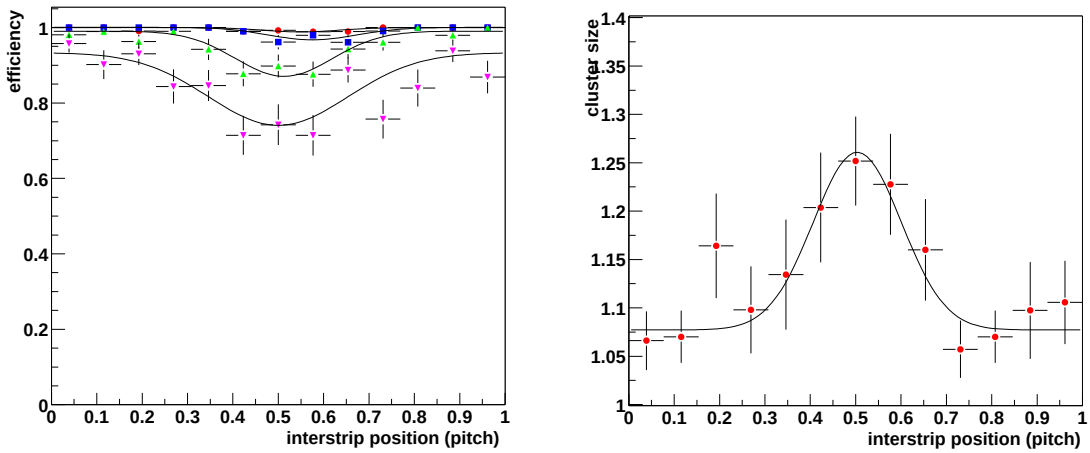

Fig. 12. *(a)* on l.h.s. plot: efficiency vs. interstrip position for a KB module at different threshold value. No lack are observed below 2 fC (up triangles). *(b)* on r.h.s. one: average cluster size in strip number at 1 fC threshold. A pick is observed right in the middle of strip-to-strip space, where probability to have charge sharing is higher.

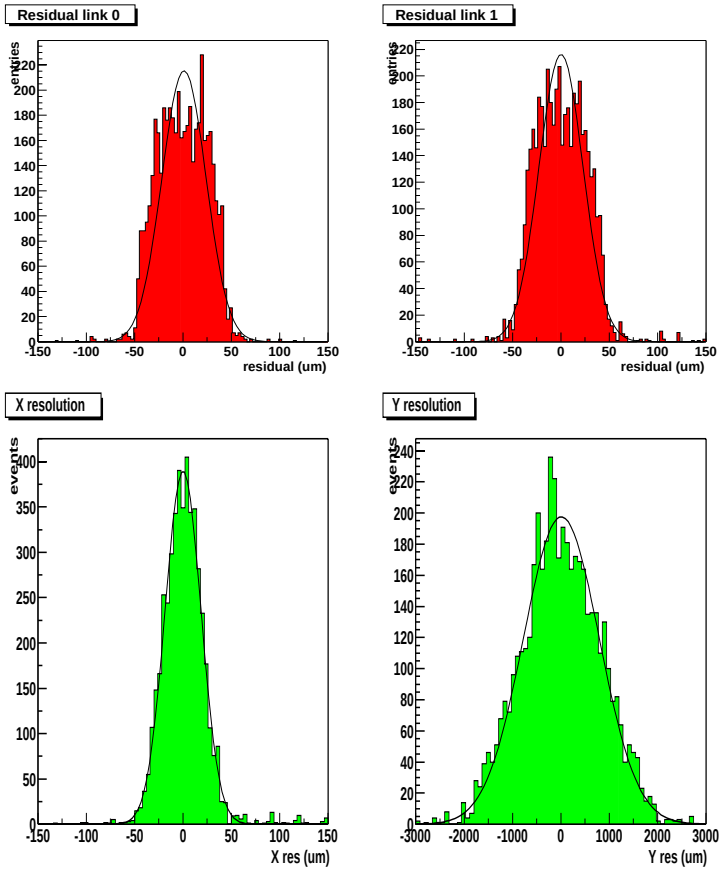

Fig. 13. *(a),(b):* Residual of the two single planes for an unirradiated KB module (KB-102). Combining the values an estimation of spatial resolution is obtained, giving X res. $\simeq$ 19 μm, Y res. $\simeq$ 750 μm, as expected from performed simulations *(c),(d)*[2].

6 Conclusion

The electrical performance of KB module prototypes has been described. Measurements have been performed on a single module test bench for outer end cap modules. From the electrical viewpoint, outer modules have the least favorable performance. Eight modules have been studied, and the results obtained are representative of the typical performance of this end-cap design. The performance of non irradiated modules are well within the specifications, with a noise occupancy not exceeding 4×10^{-5} at a 1 fC threshold and a mean ENC noise of 1410 e- ENC.
Of the eight KB modules built, one of them has been irradiated at a fluence simulating 10 years of ATLAS running. The noise occupancy then reaches a value of 4 $\times10^{-3}$ at a 1fC threshold and an ENC noise of about 1980 e- ENC.

We have demonstrated the validity of the alternative solution to the baseline modules [20], using a module design based on a barrel hybrid assembled in an end-cap configuration. Thermal measurements have also been performed and have been summarized in [5].

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References

[1] C. Lacasta, *Electrical Specifications and Expected Performances of the End-cap Module*, ATL-IS-EN-0008.

[2] ATLAS TDR 5, *Inner Detector Technical Design Report*, Vol II, CERN/LHCC 97-17, April 1997.

[3] W. Dabrowski et al., *Design and performance of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS Semiconductor Tracker*, IEEE Trans. Nucl. Sc., Vol. 47, No 6, Dec. 2000.

[4] Barrel Module Final Design Review, SCT-BM-FDR-1 to 9.

[5] M. Donegá et al., *Thermal performance measurements on ATLAS-SCT KB forward modules*, ATL-COM-INDET-2003-007.

[6] KB NIM paper, in preparation.

[7] P.W.Phillips, L.Eklund *Electrical Tests of SCT Hybrids and Modules.*

[8] http://scipp.ucsc.edu/groups/atlas/elect-doc/LVSpec.pdf.

[9] http://hepwww.rl.ac.uk/atlas-sct/mm/Mustard/MUSTARD.PS

[10] http://hepwww.rl.ac.uk/atlas-sct/mm/Slog/SLOG.PS.

[11] http://www.hep.ucl.ac.uk/ mp/C-C Master regs+busy memo.txt.

[12] http://scipp.ucsc.edu/groups/atlas/elect-doc/HVSpec.pdf.

[13] ROOT,*An Object-Oriented Data Analysis Framework*, Users Guide 3.02c

[14] P.W.Phillips, *Temperature dependence of barrel modules noise*

[15] P. Dervan et al. *Irradiation of ATLAS SCT Modules and Detectors in 2002* ATL-COM-INDET-2003-001

[16] W.Dabrowski et al. *Radiation Hardness of the ABCD Chip for the Binary readout of silicon strip detectors in the Atlas semiconductor tracker.*

[17] W.Dabrowski, *ABCD3TA ASIC: Requirements and Specification*, ATL-IS-ES-0039

[18] ATLAS Note ATL-INDET-2002-024.

[19] ATLAS Note on 2002 test beams in preparation.

[20] M.Mangin-Brinet et al. *Electrical test results from ATLAS-SCT end cap modules* ATL-COM-INDET-2003-008.