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ELECTRICAL CHARACTERISTICS OF SILICON PIXEL SENSORS

I. Gorelov, G. Gorfine, M. Hoeferkamp, V. Mata-Bruni, G. Santistevan, S. C. Seidel*)
New Mexico Center for Particle Physics, University of New Mexico, Albuquerque

A. Ciocio, K. Einsweiler, J. Emes, M. Gilchriese, A. Joshi, S. Kleinfelder, R. Marchesini, F. McCormack, O. Milgrome, N. Palaio, F. Pengg, J. Richardson, G. Zizka
Lawrence Berkeley National Laboratory and University of California, Berkeley

M. Ackers, G. Comes, P. Fischer, M. Keil, G. Martinez, I. Peric, O. Runolfsson, T. Stockmanns, J. Treis, N. Wermes
Physikalisches Institut, Universität Bonn, Bonn

C. Gößling, F. Hügging, J. Klaiber-Lodewigs, O. Krasel, J. Wüstenfeld, R. Wunstorf
Institut für Physik, Universität Dortmund, Dortmund

D. Barberis, R. Beccherle, C. Caso, M. Cervetto, G. Darbo, G. Gagliardi, C. Gemme, P. Morettini, P. Netchaeva, B. Osculati, L. Rossi
Dipartimento di Fisica e I.N.F.N., Genova

E. Charles, D. Fasching
Department of Physics, University of Wisconsin, Madison

L. Blanquart, P. Breugnon, D. Calvet, J.-C. Clemens, P. Delpierre, G. Hallewell, D. Laugier, T. Mouthuy, A. Rozanov, I. Valin
Centre de Physique des Particules de Marseille, Marseille

A. Andreazza, M. Caccia, M. Citterio, T. Lari, C. Meroni, F. Ragusa, C. Troncon, G. Vegni
Dipartimento di Fisica, Universitá di Milano e I.N.F.N. Sezione di Milano, Milano

G. Lutz, R. H. Richter, T. Rohe
Max-Planck-Institut für Physik, München

G. R. Boyd, P. L. Skubic
Department of Physics and Astronomy, University of Oklahoma, Norman

P. Šícho, L. Tomasek, V. Vrba
Academy of Sciences of the Czech Republic, Institute of Physics, Prague

M. Holder, M. Ziolkowski
Fachbereich Physik, Universität Siegen, Siegen

D. Cauz, M. Cobal-Grassmann, S. D'Auria, B. De Lotto, C. del Papa, H. Grassmann, L. Santi
Dipartimento di Fisica e I.N.F.N., Udine

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K. H. Becks, G. Lenzen, C. Linder
Fachbereich Physik, Bergische Universität, Wuppertal

ABSTRACT

Prototype sensors for the ATLAS silicon pixel detector have been electrically characterized. The current and voltage characteristics, charge collection efficiencies, and resolutions have been examined. Devices were fabricated on oxygenated and standard detector-grade silicon wafers. Results from prototypes which examine p-stop and standard and moderated p-spray isolation are presented for a variety of geometrical options. Some of the comparisons relate unirradiated sensors with those that have received fluences relevant to LHC operation.

*) Corresponding author. Address: Department of Physics and Astronomy, University of New Mexico, Albuquerque, NM 87131, USA. E-mail: seidel@glueball.phys.unm.edu. Telephone: 1-505-277-2616. Fax: 1-505-277-1520.

1 Introduction

Electrical measurements have been made on prototype n^+-on-n silicon pixel sensors [1, 2] designed for the ATLAS pixel detector [3]. This detector will be crucial for secondary vertex resolution and b-tagging at the Large Hadron Collider (LHC). The detector consists of three barrel layers and 2×3 disks. The smallest unit will be a module made of one silicon pixel sensor, 16 pre-amplifier chips, and associated high density interconnect and read-out electronics. The prototype sensors that were examined in this study display a variety of options in geometry, implant isolation technology, and substrate dopant concentration. Prototypes from four series (called 1a, 1b, 1c, and 2) were studied before and after irradiation to LHC fluences. Leakage current, breakdown and full depletion voltage, charge collection, and resolution were examined. All wafer designs included either two or three tiles, which are full size ATLAS prototype sensors to be connected to 16 pre-amplifier chips, and several "single chip" sensors, which are read out by one chip.

The n-type implants in these devices must be electrically isolated from each other to prevent their being shorted by the accumulation layer at the Si-SiO_2 interface. The two isolation techniques examined are the p-stop [4] and the p-spray [5].

The ATLAS prototype p-stop is a heavily doped ($5.0 \times 10^{13}/\mathrm{cm}^3$) p-type implant introduced between n-implants. Its geometry combines "atolls," which surround the individual n-type implants, and a common grid which pervades the full pixel array. A detailed description of these p-stops may be found in Reference [1]. The ATLAS p-spray [1] is a layer of p-type material of concentration approximately $10^{12}/\mathrm{cm}^2$ (for details, see below) implanted on the entire n-side surface before other processing, then overcompensated where n-implants are needed. While both techniques provide effective isolation for implants in the low fluence regime, p-spray devices increase their resistance to radiation as their dose increases, due to the fact that developing oxide charge compensates the p-spray type, leading to progressively lower electric fields at n-p boundaries as irradiation proceeds. Consequently the breakdown voltage of p-spray devices is at its minimum prior to irradiation and increases with radiation up to hundreds of volts.

On the p-spray devices, the requirement that the detector be able to be biased during testing, prior to attachment of the electronics chips, is met by a bias grid—a network of implanted bus lines, one between every other column pair of pixels. Each bus line is connected to an n^+ implant dot near each pixel. When voltage is applied to the grid, it reaches each pixel by punchthrough from its corresponding dot. Variations to this design are termed "small dot grid" (SMD), and "large dot grid" (LAD), for dot diameters of 10 μm and 15 μm, respectively, and the "no dot grid" (NOD), in which the dot is eliminated and the bias reaches the implant directly from the neighboring bus line. Figures 1, 2, and 3 illustrate the SMD, LAD, and NOD designs, respectively.

Two p-spray design options were examined: standard and moderated. These are distinguished by the p-type dopant density profile. For a wafer with standard p-spray, the entire surface has a uniform concentration of $3.5 \times 10^{12}/\mathrm{cm}^2$ of p-type implant. In moderated p-spray, the concentration varies from $1.5\times 10^{12}/\mathrm{cm}^2$ at the interfaces with the n^+ implants to $3.5\times 10^{12}/\mathrm{cm}^2$ in the center of the gaps between pixels. Figure 4 illustrates standard and moderated p-spray and p-stop isolation.

The density of standard p-spray, and the maximum density of moderated p-spray, are slightly higher than the observed saturation value ($3 \times 10^{12}/\mathrm{cm}^2$) of surface charge density and so maintain isolation throughout the radiation lifetime of the sensor. The lower density at the n-p interfaces in moderated p-spray reduces both the capacitance

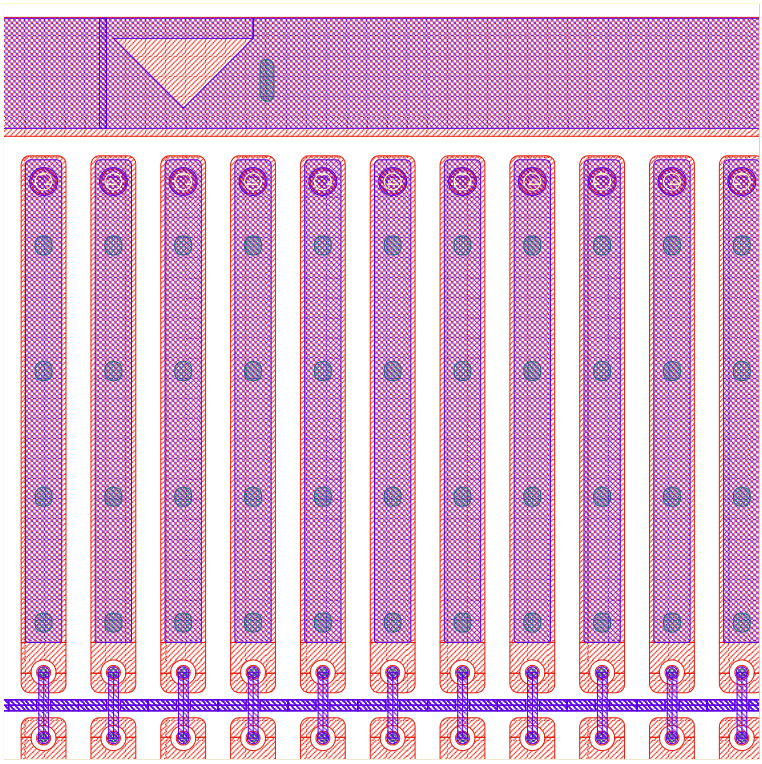

Figure 1: The SMD bias grid design.

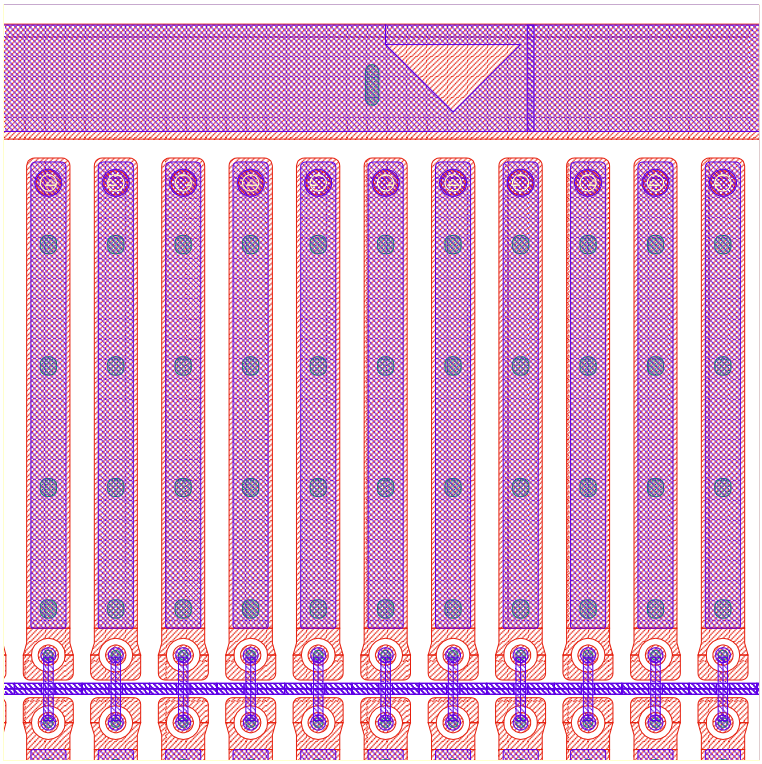

Figure 2: The LAD bias grid design.

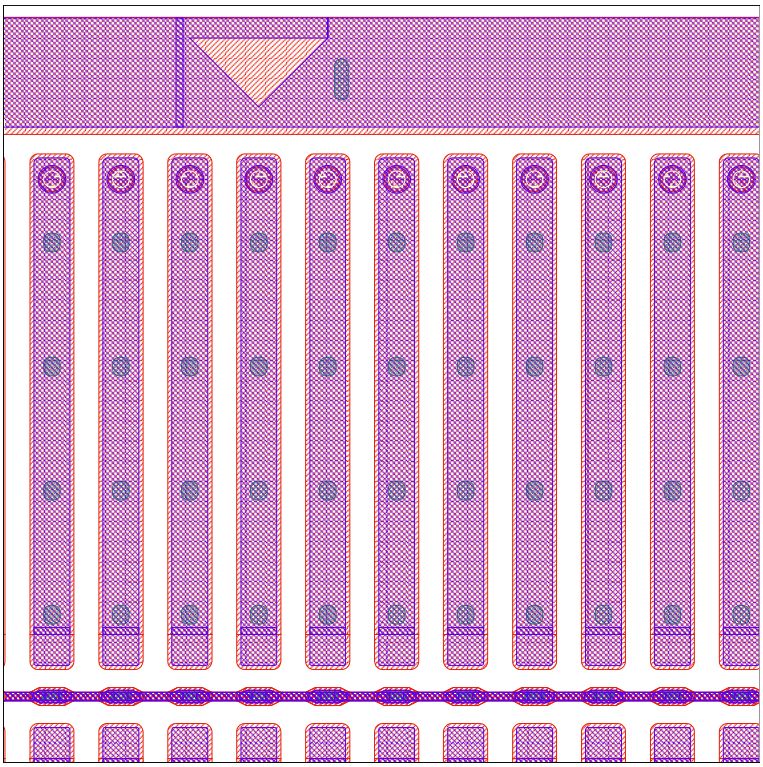

Figure 3: The NOD bias grid design.

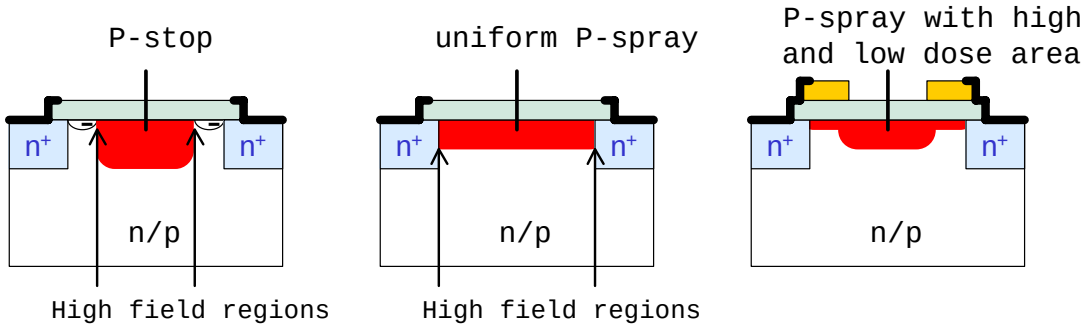

Figure 4: Isolation techniques, from left to right: p-stop, standard p-spray, and moderated p-spray.

between implants and the electric field at the interfaces.

The moderated design consequently has the property that, prior to irradiation, it provides higher breakdown voltage than does a comparable design in standard p-spray. As irradiation proceeds, the breakdown voltage rises just as in the case of normal p-spray. After being irradiated to the same fluence, a standard p-spray device and a moderated p-spray device show the same leakage current versus bias voltage characteristic.

The tolerance of silicon devices to radiation can be improved by deliberately introducing oxygen to the substrate [6]. Oxygenated wafers with concentrations ranging from $2 \times 10^{17}/\mathrm{cm}^3$ to $4 \times 10^{17}/\mathrm{cm}^3$ were examined. The oxygen enhancement was achieved by immersing the wafer for 24 hours in a 1150°C oxygen atmosphere prior to processing.

2 Characteristics of the Prototypes

Table 1 summarizes many of the features of the prototypes. Prototype 1a wafers included two tiles and 17 single chip sensors. The details of the Prototype 1a design were described thoroughly elsewhere [1] and are not all repeated here. The basic cell size was $50\mu\mathrm{m} \times 400\mu\mathrm{m}$. One of the tiles (Tile 1) and three of the single chips (ST1) had the same design and examined p-stop technology. The other tile (Tile 2) and three of the single chips (ST2) had a different design and examined p-spray technology. The remainder examined other geometrical options, including one called SSG, that used the p-spray technology and had no n^+ atoll surrounding the pixel (see below). This design eventually evolved into the ATLAS production sensor design (Tile 3). Figure 5 shows the features of the ST1, ST2, and SSG devices. Prototypes were fabricated by three companies: CiS (16 non-oxygenated wafers), Seiko (20 non-oxygenated wafers), and TESLA (9 oxygenated wafers and 7 non-oxygenated wafers). The thickness of the wafers was 300 μm for Seiko, 280 μm for CiS, and 280 μm for TESLA. The crystal orientation was $\langle 111 \rangle$ for CiS, $\langle 100 \rangle$ for Seiko, and $\langle 111 \rangle$ for TESLA. Of the CiS wafers, 13 had Si_3N_4 passivation and three, SiON passivation. All of the Seiko and TESLA wafers were passivated with Si_3N_4. In the figures of this paper, Seiko is indicated as "Vendor 1," CiS as "Vendor 2," and TESLA as "Vendor 3." Figure 1 in Reference [1] shows the Prototype 1a wafer.

Table 1: Characteristics of the ATLAS Prototype pixel sensor wafers.

Series	Isolation	Thickness (μm)	Oxy.	P-spray	Passivation	# Wafers	Vendor
1a	both	280	no	standard	nitride	13	CiS
		280	no	standard	SiON	3	CiS
		300	no	standard	nitride	20	Seiko
		280	no	standard	nitride	7	TESLA
		280	yes	standard	nitride	9	TESLA
1b	p-spray	200	no	standard	nitride	2	CiS
		200	no	moderated	nitride	1	CiS
		280	no	standard	nitride	2	CiS
		280	no	moderated	nitride	2	CiS
1c	p-spray	200	no	moderated	nitride	9	CiS
		280	no	moderated	nitride	19	CiS
2	p-spray	250	no	moderated	nitride	13	CiS
		250	yes	moderated	nitride	18	CiS

Prototype 1b wafers were fabricated with standard silicon and included two tiles and 17 single chip sensors, all with p-spray isolation. As we have reported elsewhere [1], the layout of Prototype 1a p-spray sensors produced a charge collection problem associated with the n^+ atoll surrounding the pixel. In prototype 1b the atoll was eliminated and the width of the pixel implant was slightly increased. Modifications were made as well in the bias grid to reduce some residual charge loss: whereas the bias lines of Prototype 1a had been implanted, the bias lines of Prototype 1b were metalized, with only the bias dot implanted. The bias dot was integrated with the primary n^+ implantation for its cell.

The single chip devices in Prototype 1b used the same geometries as the Prototype 1a versions with the exception of the design change mentioned; their names were correspondingly modified to SSGb, etc. Figure 5 shows the features of the SSGb devices. Relative to SSG, their dimensions in the short direction are changed from 37μm + 13μm (gap) to 30μm + 20μm (gap). Prototype 1b wafers used the same design for their tiles (called Tile 3) as for the SSGb single chip sensor. The 1b prototypes examined two thicknesses, 200μm and 280μm. Some sensors of each thickness used moderated p-spray while some used standard: of the four 280μm wafers, two were standard p-spray and two were moderated. Of the three 200μm wafers, two were standard p-spray and one was moderated. All seven Prototype 1b wafers were manufactured by CiS and used Si_3N_4 passivation and $\langle 111 \rangle$ crystal orientation.

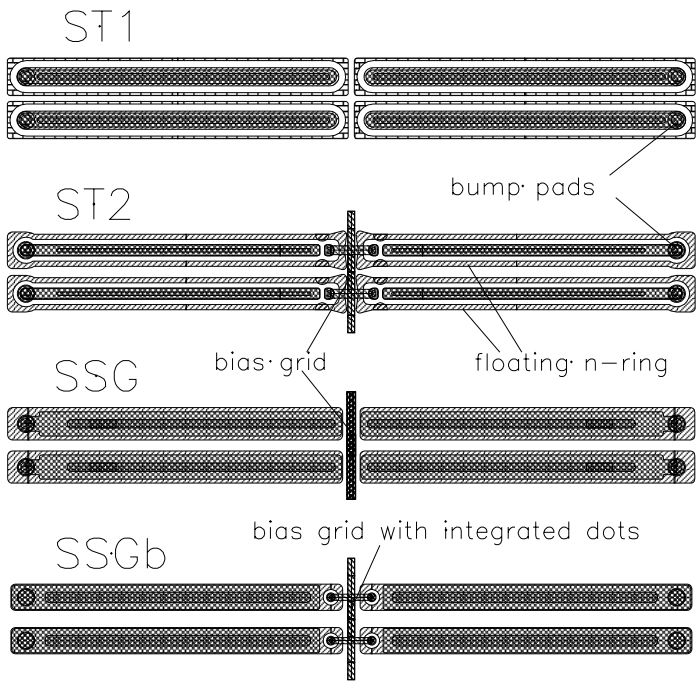

Figure 5: The ST1, ST2, SSG, and SSGb designs.

Prototype 1c wafers were geometrically similar to Prototype 1b wafers except for a revision in the dimensions of the contact openings in the oxide layer between the metal layer and the n^+ implant. The opening had been rectangular, of dimensions 306μm$\times 12\mu$m, in Prototype 1b. In Prototype 1c the structure was revised to four circular openings of diameter 13.5μm each. The revision was made to decrease the area of unprotected implant. Prototype 1c used standard silicon, Si_3N_4 passivation, $\langle 111 \rangle$ crystal orientation,

and moderated p-spray for all structures. CiS fabricated all Prototype 1c wafers. Nine wafers of thickness 200μm and 19 wafers of thickness 280μm were examined. Data from Prototypes 1b and 1c have been combined in the figures in this paper. (In cases where this is done, the devices are referred to as, for example, "SSGb/c.")

Three tiles and 12 single chips were included on each Prototype 2 wafer to test the SMD, LAD, and NOD bias grid designs. To allow a comparison, devices were fabricated with oxygenated and non-oxygenated substrates. All of the wafers were fabricated with moderated p-spray and the $\langle 111 \rangle$ crystal orientation, passivated with silicon nitride. The wafers were 250 μm thick. The Prototype 2 wafers were fabricated by CiS (18 oxygenated wafers and 13 non-oxygenated ones).

The final design selected for the ATLAS production sensors uses p-spray isolation and the SMD bias grid on oxygenated wafers of thickness 250μm. The pixel cells have dimensions 50μm $\times$ 400μm, the reduced-size oxide layer openings, $\langle 111 \rangle$ crystal orientation, and Si_3N_4 passivation. Each pixel consists of one rectangular n^+-implantation of dimensions 30μm $\times$ 382.5μm. The gap between two adjacent pixels is 20μm in the short pitch direction, 15 μm in the long pitch direction at the pixel side with the bump pad, and 20μm at the other pixel side, where the bias grid is located. The bias grid connection to each pixel is provided using a round n^+-implant integrated in the n^+-pixel implant with 10μm diameter and 5μm gap to limit the coupling from the bias dot to that particular pixel. The bias dots of all pixels in an adjacent pair of columns are connected via a metal line to an outer n^+-implantation which surrounds the border of the active sensor area.

3 Irradiation Conditions

A subset of the prototypes was irradiated with different fluences to simulate the ATLAS environment. Irradiations were performed with the 300 MeV pion beam at the PSI Laboratory, Switzerland and with the 55 MeV proton beam at Lawrence Berkeley National Laboratory, U.S.A. Unless otherwise noted, all fluences are quoted in 1 MeV neutron equivalent, designated as 1-MeV n_{eq}. Irradiations were made at room temperature without bias. Storage and subsequent measurements were done at or below -10°C to inhibit annealing of bulk damage. Quoted currents have been normalized to -10°C according to the equation $I(T) \propto (kT)^2 e^{-E/2k_BT}$, where k_B is Boltzmann's constant and $E = 1.21$ eV is the activation energy.

4 Measurements and Requirements

The techniques by which the measurements were made have been described previously [1, 2]. Figure 10 of Reference [1] shows the setup for measurements of leakage current versus bias voltage ("I-V"). Two probe needles are placed on the p-side, one on the active area and another at the wafer edge or device scribe line. The contact to the edge or scribe line is shorted to the n-side. The breakdown voltage is defined as the highest measured voltage for which the normalized leakage current is $< 1\mu$A for tiles and < 100nA for single chips. ATLAS requires the breakdown voltage of the unirradiated sensors to be greater than 150 V or $V_{\text{depletion}} + 50$V, whichever is higher. $V_{\text{depletion}}$ is required to be ≤ 120V. In this paper, because the distinction is small, we simply require $V_{\text{breakdown}} > 150$V. For all voltage measurements reported in this paper, the uncertainty on the central value is ± 5 V.

Charge collection and spatial resolution were measured at the CERN SPS accelerator with a pion beam of 180 GeV/c momentum. A beam telescope consisting of four pairs of silicon microstrip detectors (each with two planes of orthogonal strips) was used

to measure the transverse position of the incident beam particles. The position resolution of tracks projected onto the test devices varied from 3.0μm to 6.0μm depending upon the telescope configuration. The sensors were integrated in modules with prototype ATLAS electronics chips, which operate with a 40 MHz clocking rate and measure pulse height by recording the time that the amplifier remains above the threshold. Typical thresholds were about 3000 electrons, and threshold dispersion was 170 electrons rms. The noise was typically 150 electrons rms. Resolutions were measured for both analog and digital clustering algorithms [2] as a function of track incidence angle. The charge collected by the pixels was studied as a function of the point of impact of the traversing particles relative to a pair of pixel cells. For hits not at a pixel center, the signal was shared between several pixels, and the sum of the pixel measurements is reported. The electronics threshold was set at 2000 electrons for the charge-sharing studies. During test beam runs, unirradiated sensors were operated at 150 V and irradiated ones at 600 V (unless otherwise stated).

4.1 Isolation: p-stop versus p-spray

Figures 6 and 7 show the breakdown voltages of devices of the Tile 1 (p-stop) and Tile 2 (p-spray) designs for *unirradiated* tiles and single chip sensors, respectively. One sees that in a low radiation environment, the two designs show comparable breakdown voltage, with the Tile 1/ST1 being potentially slightly better. The decision between p-stop and p-spray isolation is, consequently, highly linked to the fluence expected.

Figures 8 and 9 show I-V curves for ST1- and ST2-type single-chip sensors, respectively, that have been irradiated to the same fluence (2.5×10^{14} 55-MeV p/cm^2, equivalent to 4.3×10^{14} 1-MeV n/cm^2), measured at -20°C (measurement normalized to -10°C), and are otherwise identical in fabrication and handling. One sees that whereas the ST1 breaks down at approximately 150 V (the exact value is not well defined due to the absence of a bias grid structure), the ST2 remains viable up to at least 500 V. This radiation resistance of p-spray motivated the selection of that technology for future prototype cycles.

4.2 Passivation

Figure 10 compares the breakdown voltages of ST2 sensors with nitride and SiON passivation. Both types behave acceptably, showing comparable breakdown voltages. Both could be compatible with bump bonding processes. Nitride was selected by ATLAS.

4.3 Geometrical Options Using P-spray Isolation

Figure 11 shows the average collected charge as a function of the position of the perpendicularly incident track on the cell in the short dimension, for ST1, ST2, and SSG sensors. Figure 12 shows the average collected charge as a function of the position of the perpendicularly incident track relative to a pair of pixels in the long dimension, for ST1, ST2, and SSG. Charge loss in ST2 was approximately 25% over the full cell. A 20% loss is attributed to the presence of the floating n-ring in the design. The remaining 5% loss is due to the implanted bias grid. The SSG and ST1 designs had good charge collection performance over the full cell except for minor local losses not exceeding 10% locally and not significantly affecting the average over the full cell. The approximately 10% local loss in the SSG design is similarly associated with its bias grid–in this case the dot structure. The 10% local loss in the ST1 is due to the fact that the gap between p-stops in that design acts (due to electron accumulation) like a small n^+ region. On the basis of these results, the SSG design was chosen over the ST2.

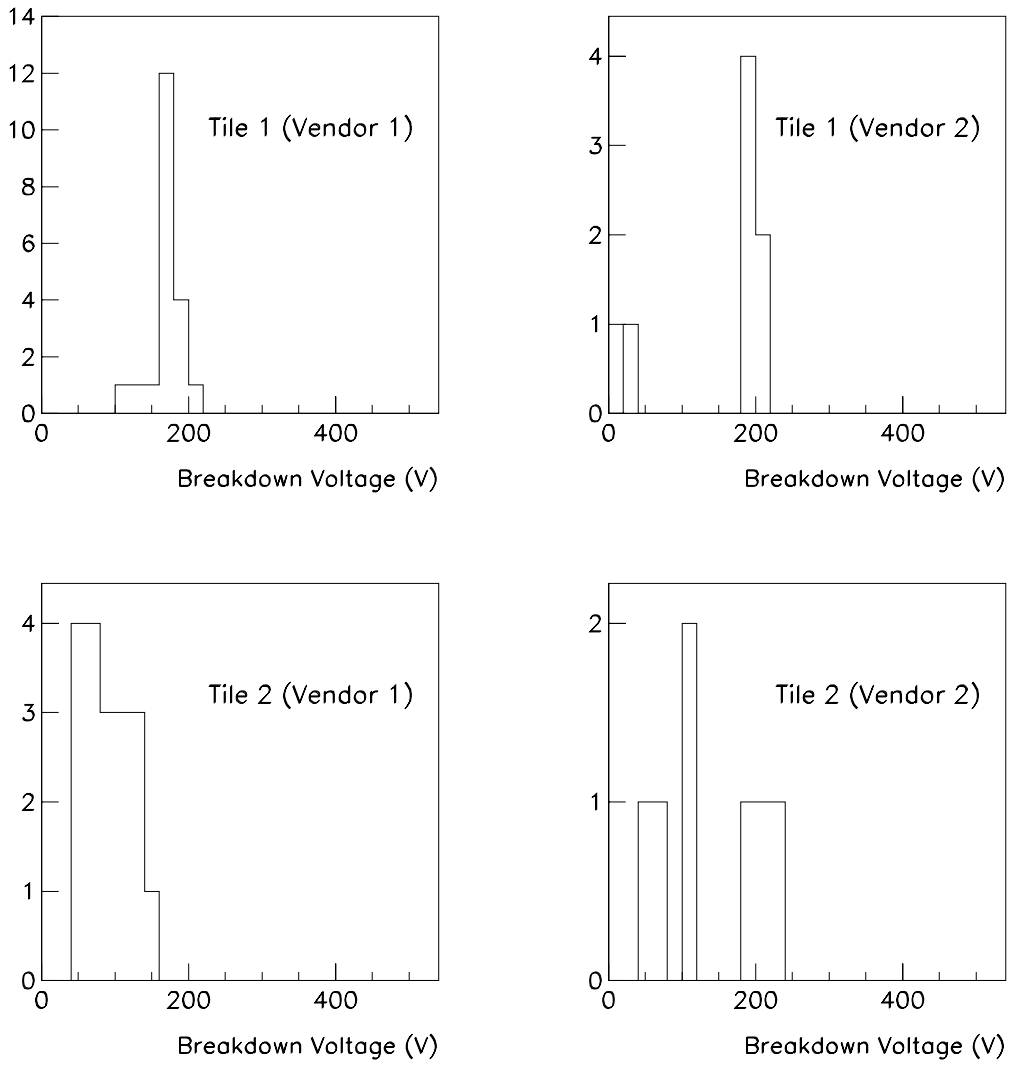

Figure 6: The breakdown voltages of unirradiated nitride-passivated Prototype 1 tiles of types Tile 1 and Tile 2.

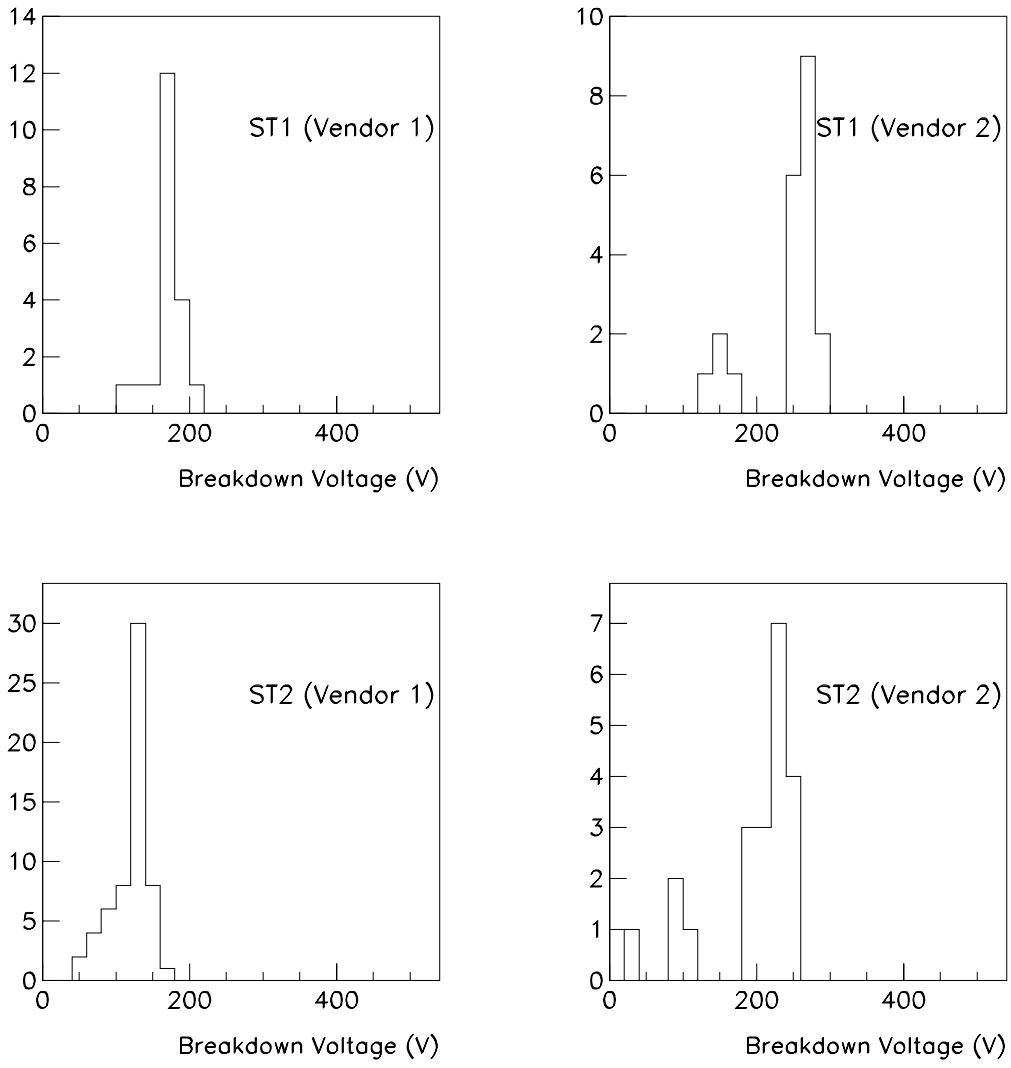

Figure 7: The breakdown voltages of unirradiated nitride-passivated Prototype 1 single chip sensors of types ST1 and ST2.

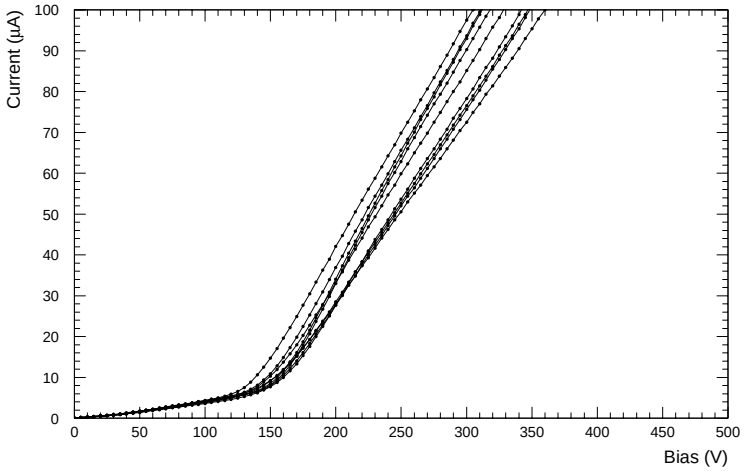

Figure 8: Current versus voltage of an ST1 single chip sensor fabricated by CiS, normalized to $-10°$C, after irradiation with 2.5×10^{14} 55-MeV p/cm^2.

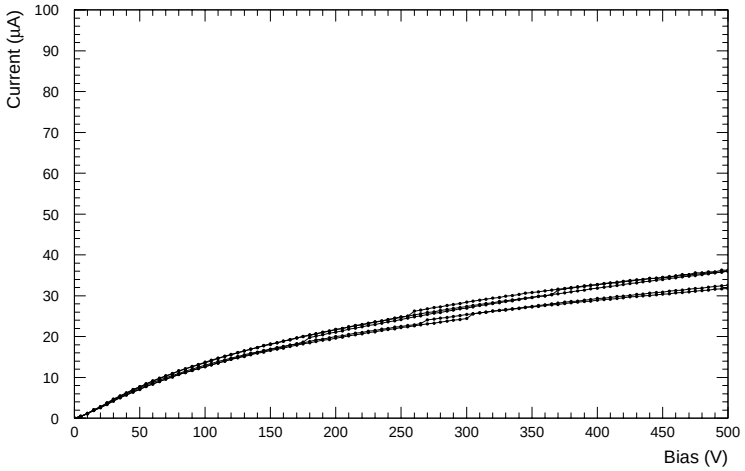

Figure 9: Current versus voltage of an ST2 single chip sensor with standard p-spray, fabricated by CiS, normalized to $-10°$C, after irradiation with 2.5×10^{14} 55-MeV p/cm^2.

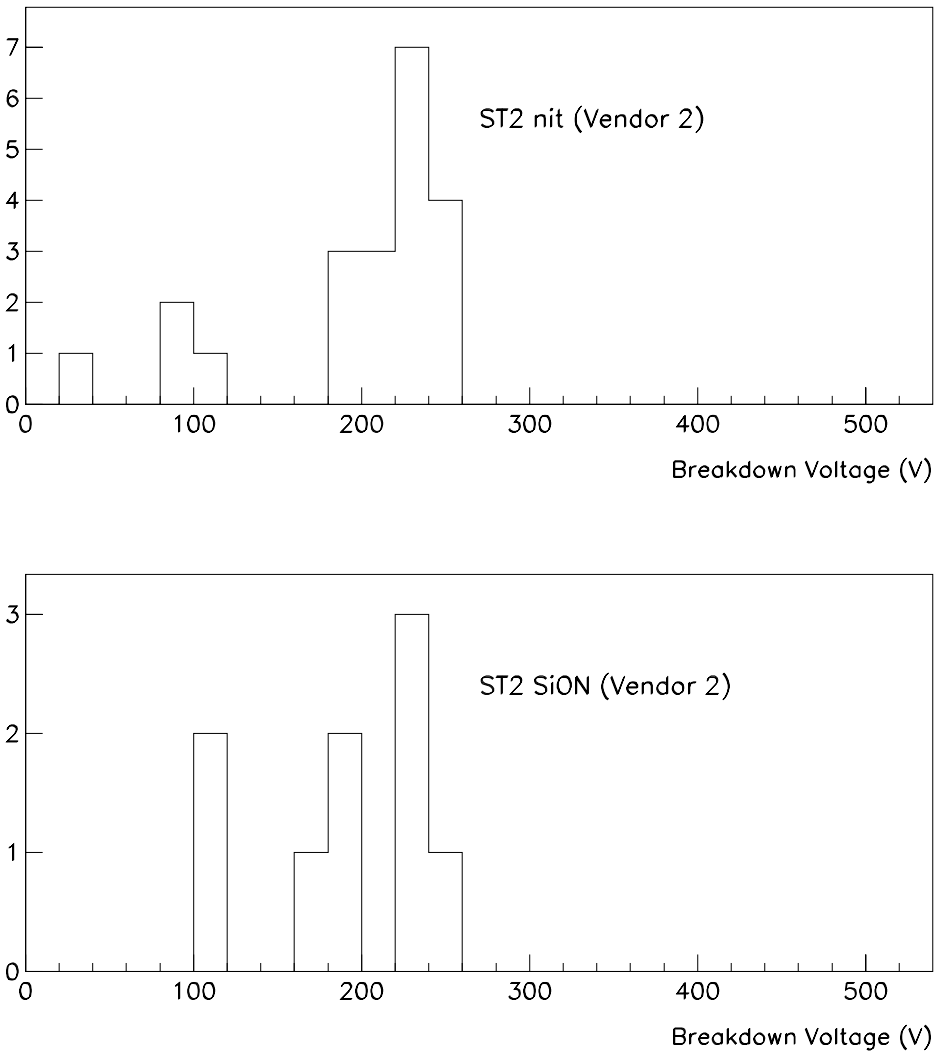

Figure 10: The breakdown voltages of unirradiated nitride-passivated Prototype 1 single chip sensors of type ST2 with nitride and SiON passivation.

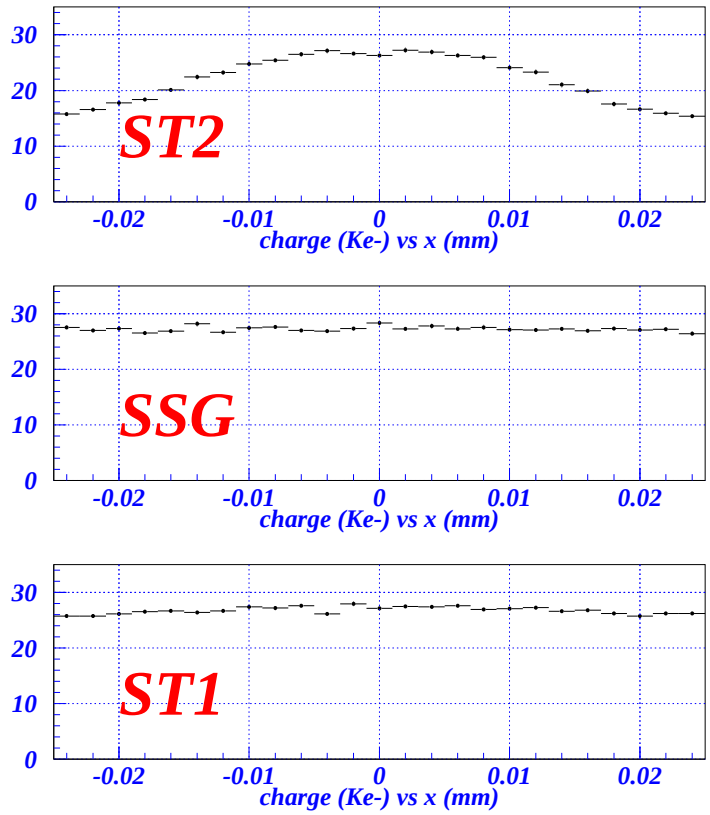

Figure 11: The average collected charge as a function of the position within a pixel cell of short dimension 50μm, for ST1, ST2, and SSG sensors. The total charge of the clusters is shown in units of thousands of electrons.

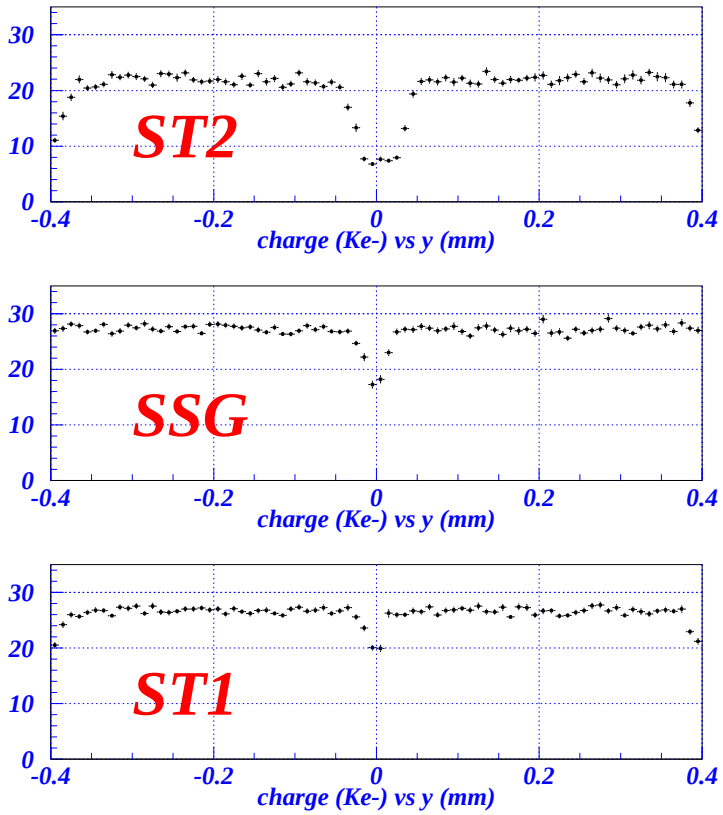

Figure 12: The average collected charge as a function of the position relative to a pair of pixel cells of long dimension $2 \times 400\mu$m, for ST1, ST2, and SSG sensors. The total charge of the clusters is shown in units of thousands of electrons.

Table 2, which uses information taken from Reference [2], summarizes measured spatial resolution for unirradiated ST1, ST2, SSG, and SSGb. As is discussed in Reference [2], the statistical uncertainties on the measurements of spatial resolution and charge sharing region in Tables 2-3 are of the order of 0.3μm, and the telescope extrapolation uncertainty (between 3μm and 6μm) has not been subtracted. The superior performance of the SSG and ST1 designs relative to the ST2 design is due to their negligible charge loss, allowing them to have a larger charge sharing region and better spatial resolution. The SSGb sensor included in Table 2 also showed negligible charge loss. Its smaller thickness (200μm) accounts for its slightly worse resolution for perpendicular incidence, its reduced charge sharing region, and the larger angle at which its best spatial resolution is reached. One sees that all of the proposed designs provide good resolution, so the decision among them can be based upon other features, including charge collection efficiency.

Table 2: Spatial resolution of unirradiated detectors. The data were taken with sensors biased to 150 V. The telescope extrapolation uncertainty has not been subtracted. The statistical uncertainties on the measurements of spatial resolution and charge sharing region are of the order of 0.3μm.

Design	ST1	ST2	SSG	SSGb
Thickness (μm)	280	280	280	200
At normal incidence:				
Charge sharing region (μm)	13.6	9.2	14.0	6.2
Digital resolution (μm)	10.7	12.1	10.5	12.7
Analog resolution (μm)	10.4	12.0	10.1	12.6
Best analog resolution (μm)	5.3	6.5	5.8	6.2
Corresponding incidence angle	10°	10°	10°	15°

Table 3, which uses information taken from Reference [2], summarizes measured spatial resolution and depletion depth for ST2 with three levels of radiation damage and SMD with high radiation damage. All of the data in this table were taken with with irradiated sensors biased to 600 V and unirradiated sensors biased to 150 V.. One sees that the resolution of a p-spray device remains consistent with ATLAS needs throughout the full expected radiation lifetime.

Tile 3 devices incorporate the improved SSGb bias grid and so addresses the charge collection problem present with ST2 devices. On standard substrates with standard p-spray, the good breakdown voltage characteristic demonstrated by unirradiated Tile 2 devices is maintained in Tile 3.

Figure 13 compares the breakdown voltages of tiles with the SMD, LAD, and NOD bias grid designs. All of the devices in that figure were fabricated with moderated p-spray on oxygenated wafers (see below). One sees that the SMD and LAD yield the same fraction of devices with acceptable breakdown voltage—approximately 75%—while the NOD does not in general meet the breakdown voltage requirement. As the SMD and LAD are equivalent in this regard, SMD was selected because the smaller dot leads to slightly lower charge loss in the region of the bias dot.

Table 3 summarizes measured charge sharing and spatial resolution information as well as depletion depth for an SMD design sensor at fluence 10^{15} n/cm^2. The sensor tested included all of the options ultimately included in the ATLAS baseline; performance superior to that obtained by ST2 designs irradiated to the same fluence is due to the

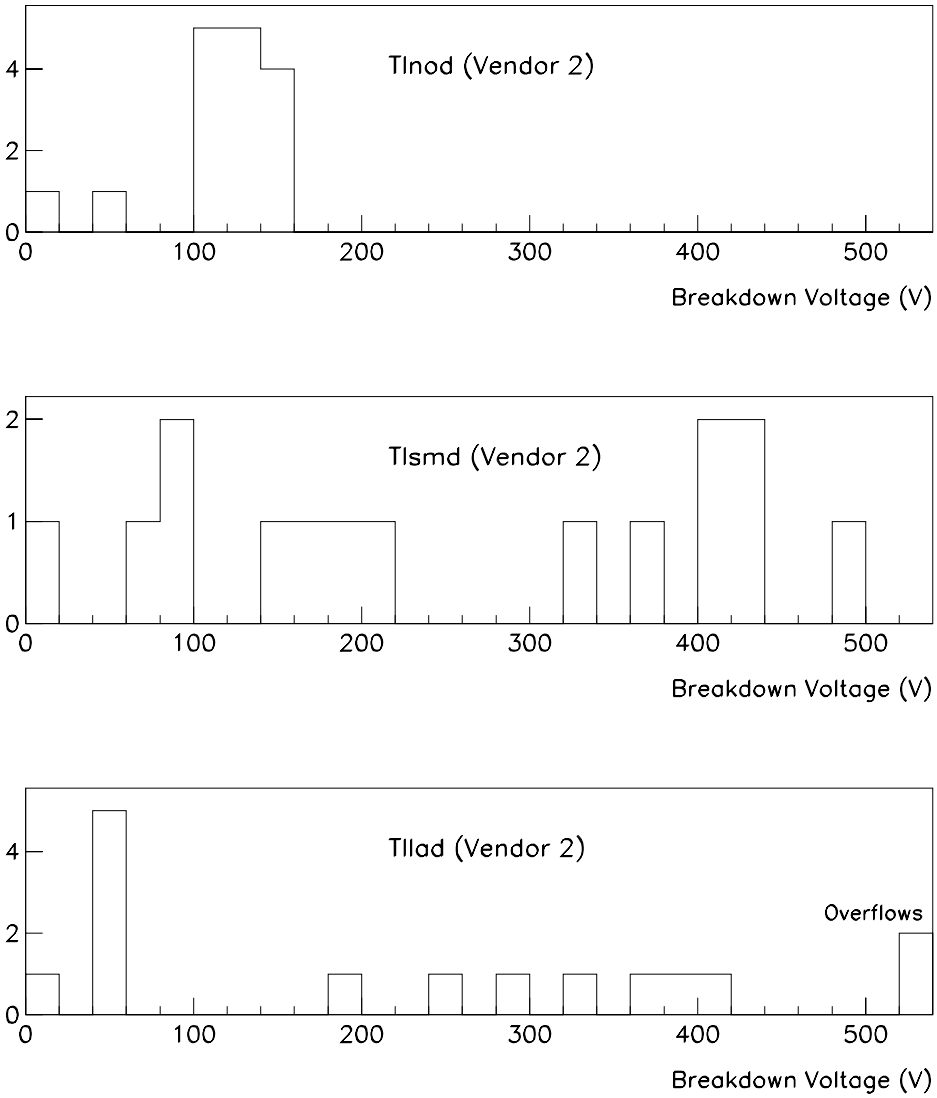

Figure 13: The breakdown voltages of unirradiated tiles of type NOD, SMD, and LAD.

Table 3: Spatial resolution and depletion depth of ST2 detectors for several fluences and of a highly irradiated SMD detector. The data were taken with irradiated sensors biased to 600 V and unirradiated sensors biased to 150 V.. The telescope extrapolation uncertainty has not been subtracted. The statistical uncertainties on the measurements of spatial resolution and charge sharing region are of the order of 0.3μm.

	ST2			SMD
Fluence (n/cm^2)	0	5×10^{14}	10^{15}	10^{15}
At normal incidence:				
Charge sharing region (μm)	9.2	5.8	3.5	4.3
Digital resolution (μm)	12.1	13.1	13.7	12.5
Analog resolution (μm)	12.0	12.9	13.7	12.4
Best analog resolution (μm)	6.5	7.3	9	7.4
Corresponding incidence angle	10°	10°	15°	15°
Depletion depth (μm)	280 ± 10	261 ± 8	203 ± 9	230

improved charge collection and fuller depletion achieved. One sees that the resolution for this design remains excellent at the maximum fluence required of the ATLAS design.

4.4 Moderated versus Standard p-spray

Figures 14 and 15 show the current-voltage characteristic of the same moderated p-spray sensor before and after irradiation to a fluence of 1.6×10^{14} 55-MeV p/cm^2 (2.7×10^{14} 1-MeV n_{eq}/cm^2) and normalization to the effective current at 20°C. The principal feature to notice is the increase in breakdown voltage with fluence, from about 580 V to well above 800 V.

Figures 16 and 17 in this section compare the breakdown voltage characteristics of devices fabricated with moderated p-spray and with standard p-spray. The figures reflect results from single chip SSGb/c and Tile 3 devices. One sees that pre-irradiation breakdown voltage is significantly improved by the moderated p-spray, which permits pre-irradiation breakdown voltages in excess of 300 V to be attained.

4.5 Oxygenated versus Non-oxygenated Substrate

The advantage of oxygenated substrates has been demonstrated in measurements both in the laboratory and in the test beam.

The laboratory procedure measures the depletion voltage of silicon sensors bump-bonded to electronics chips. The method uses a γ-ray source and measures the interaction rate in the sensor as a function of the bias voltage. Figure 18 shows the setup for the measurement: the γ source irradiates the p-side of a single-chip sensor integrated with a prototype ATLAS electronics chip. During the measurements the device and the source are maintained at about -5°C.

The interaction rate produced in the sensor by the 60 keV photons of a sealed ^{241}Am source is related to the sensor sensitive volume, which is a function of the bias voltage. It is given by the hitbus signal, which is a fastOR of the 18×164 pixel matrix. Through a completely automated program, a bias voltage scan is performed, and at each step several measurements of the hitbus frequency are taken. The mean of these measurements is plotted, yielding a function which rises at low voltages and is flat at high voltages (for which the sensor is overdepleted). Lines with different slopes are fitted to the two regions

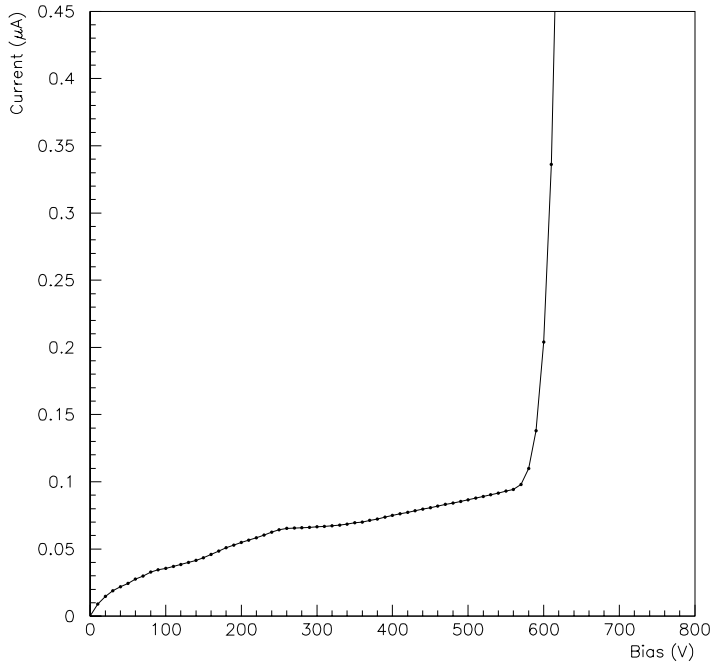

Figure 14: Leakage current versus bias voltage of an unirradiated SSG-type single chip sensor fabricated with moderated p-spray, normalized to 20°C.

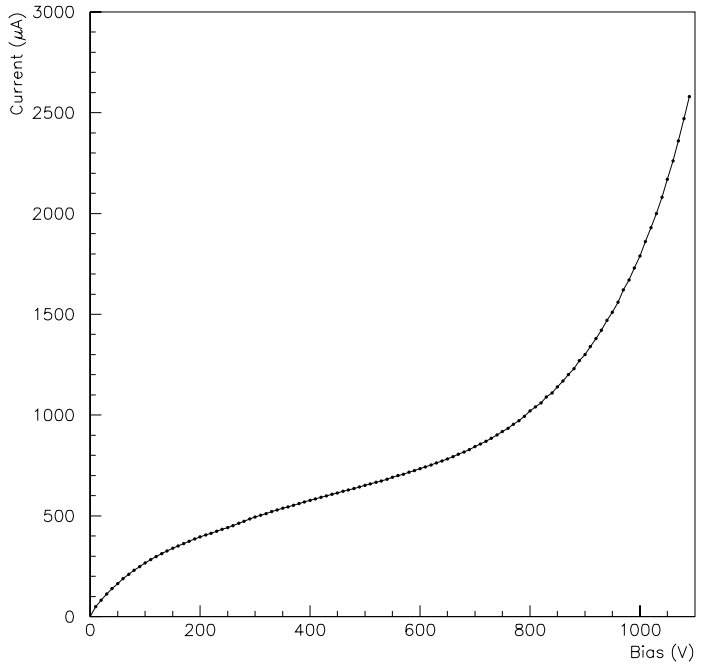

Figure 15: Leakage current versus bias voltage of an SSG-type single chip sensor fabricated with moderated p-spray, normalized to 20°C, after irradiation to a fluence of 1.6×10^{14} 55-MeV p/cm^2.

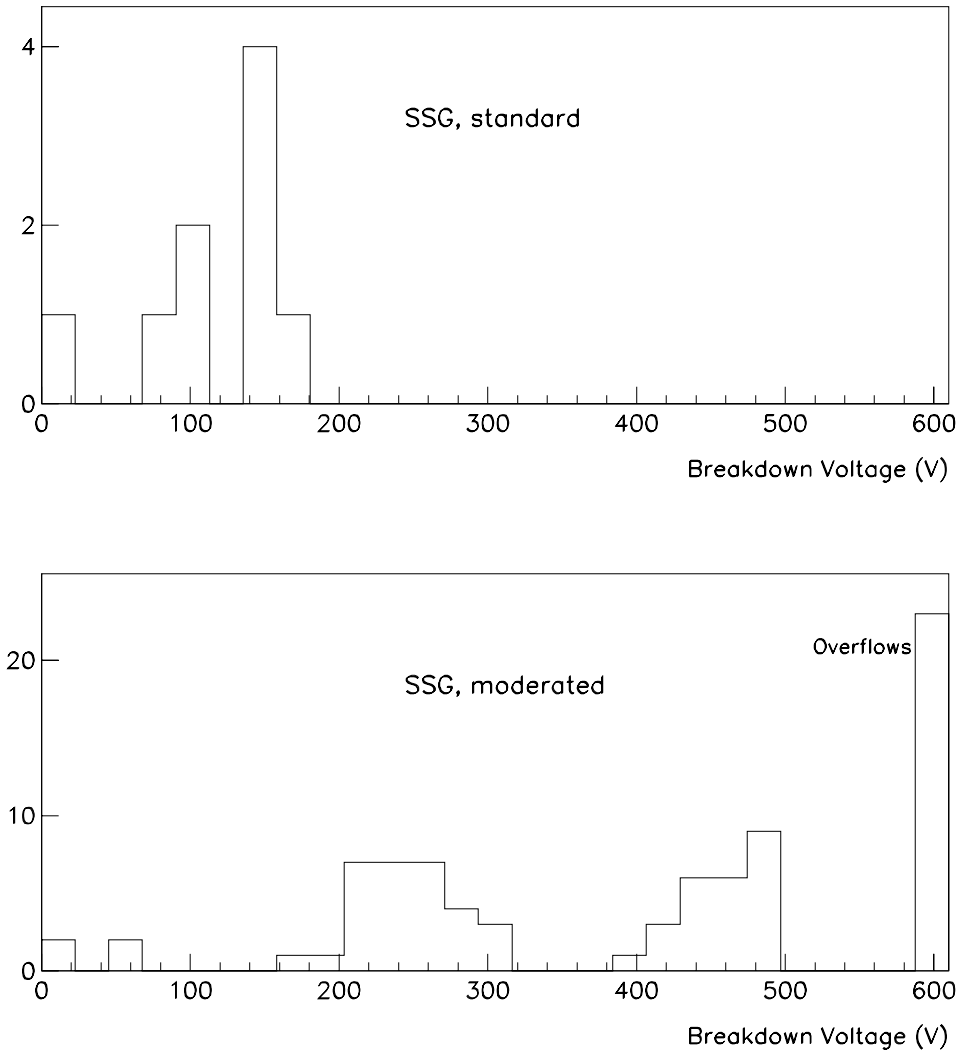

Figure 16: The breakdown voltages of unirradiated tiles of type SSGb/c with standard (upper figure) and moderated (lower figure) p-spray.

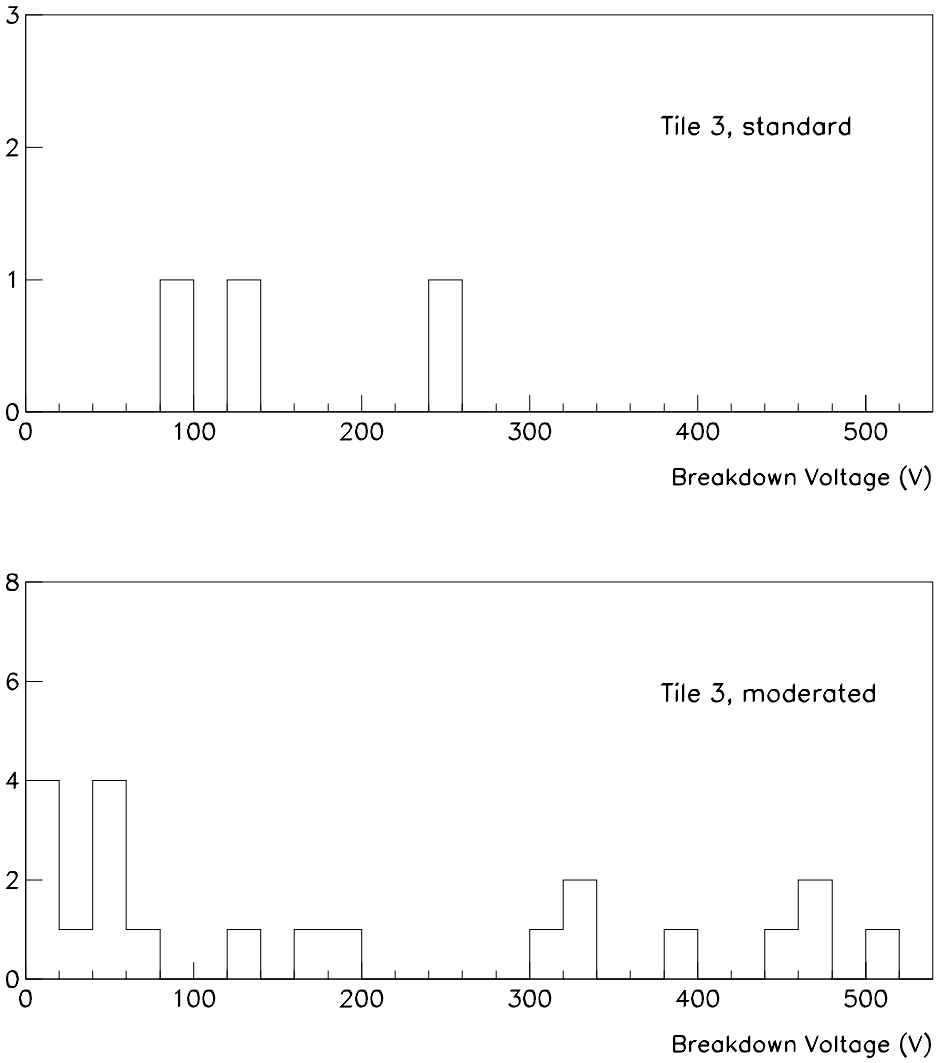

Figure 17: The breakdown voltages of unirradiated tiles of type Tile 3 with standard (upper figure) and moderated (lower figure) p-spray.

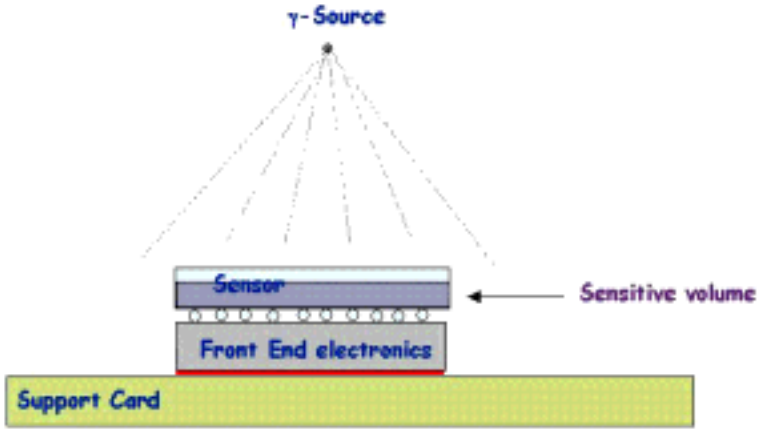

Figure 18: The setup for laboratory measurements of depletion voltage of pixel sensors bump bonded to electronics.

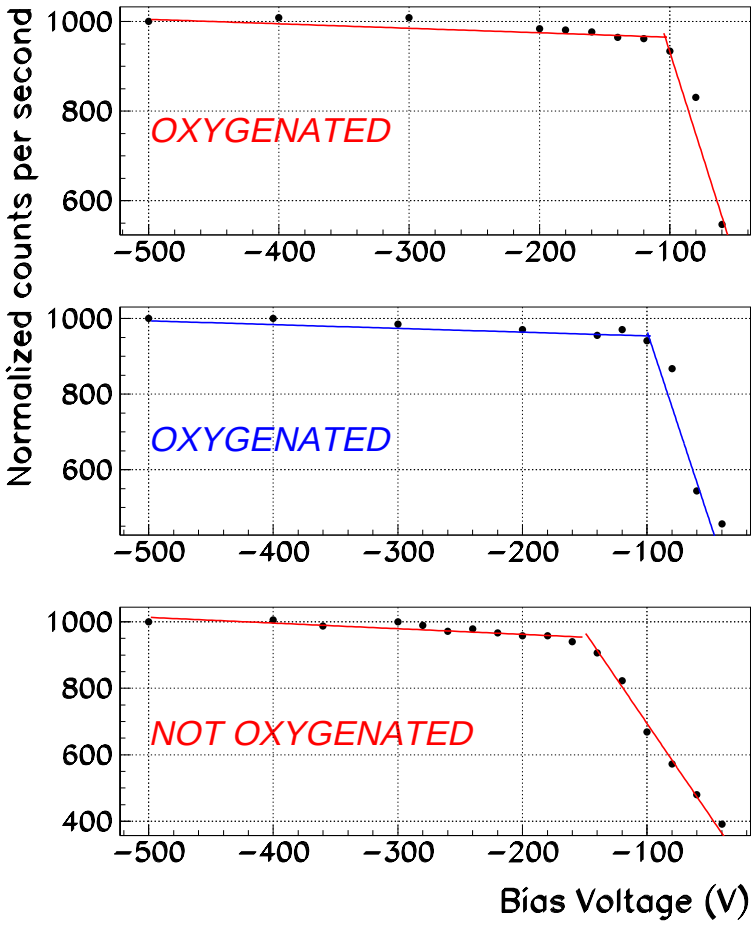

Figure 19: The interaction rate versus bias voltage for three pixel sensors irradiated to $3.0 \times 10^{14}/\mathrm{cm}^2$. The upper two use oxygenated silicon while the lower uses standard.

of this function, and the intersection point of the lines is taken as an estimate of the depletion voltage. We refer to this as the plateau voltage.

For irradiated sensors, the details of the flip-chipping process must be monitored carefully, as the readout chip is connected to the sensor after the sensor has been irradiated. The heat involved accelerates the effect of the radiation damage in the sensor. Figure 19 shows the hitbus frequency versus bias voltage for interactions produced with an ^{241}Am source in three sensors with the same temperature history. Two of the sensors were fabricated with oxygenated silicon while the third used standard silicon. All three were irradiated to the same fluence, $3.0 \times 10^{14}/\mathrm{cm}^2$. The oxygenated sensors have very similar interaction rate characteristics, showing a plateau voltage of about 100 V. The non-oxygenated sensor has a higher plateau voltage, about 150 V.

Figure 20 shows the hitbus frequency versus bias voltage for interactions produced with an ^{241}Am source in three oxygenated sensors irradiated to different fluences. The temperature history for the three sensors is the same. The plateau voltages obtained are 150 V, 180 V, 280 V for fluences of $3.0 \times 10^{14}/\mathrm{cm}^2$, $5 \times 10^{14}/\mathrm{cm}^2$ and $1.1 \times 10^{15}/\mathrm{cm}^2$, respectively. The measured values are consistent with predictions using damage parameters in a model [6] that considers the received particle flux and the temperature history from

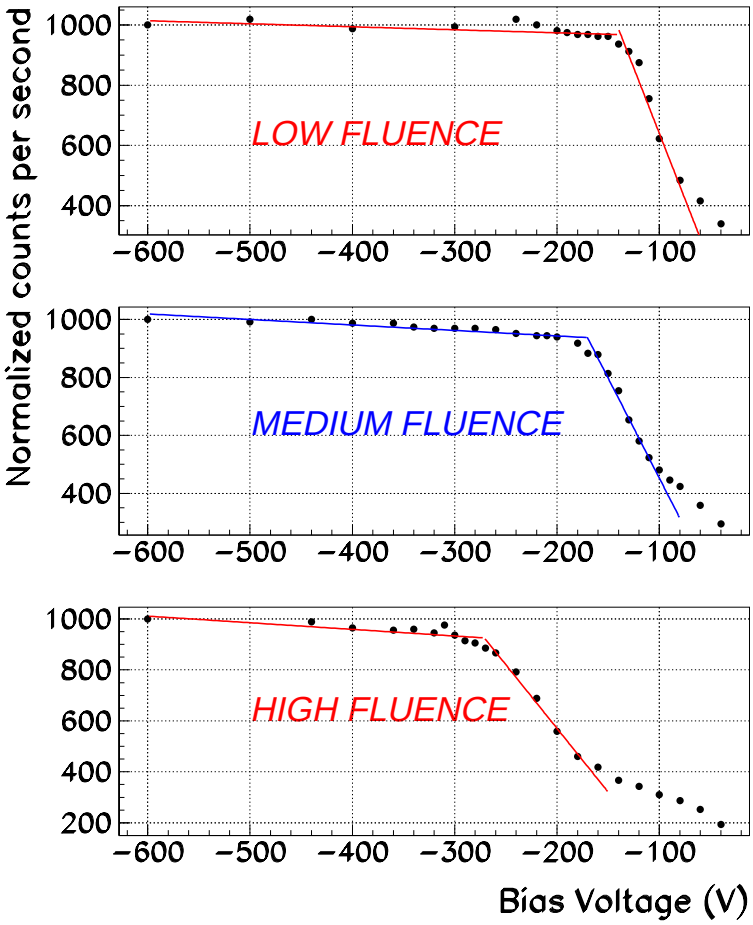

Figure 20: The interaction rate versus bias voltage for pixel sensors fabricated with oxygenated silicon and irradiated to $3.0 \times 10^{14}/\mathrm{cm}^2$ (upper), $5 \times 10^{14}/\mathrm{cm}^2$ (middle), and $1.1 \times 10^{15}/\mathrm{cm}^2$ (lower). The plateau voltage obtained by the fit is shown for each plot.

irradiation to the time of measurement.

The depletion depth has also been studied in test beam experiments at CERN using the method of inclined tracks [2]. Data were taken with a particle beam incident on the sensor at angles of 20° and 30° with respect to the normal to the pixel plane. The maximum depth of the track segment subtended by the hit pixels was measured at various bias voltages. The results are summarized in Table 4. In some cases [7] only lower limits on depletion depths could be obtained. Table 4 shows that oxygenated sensors have larger depletion depths than non-oxygenated sensors irradiated to the same fluence and operated at the same bias voltage. For example, after a fluence of $10^{15}/\mathrm{cm}^2$, a sensor made with oxygenated substrate and operated at 400 V has the same depletion depth as one made with standard substrate operated at 600 V. Furthermore, after a fluence of $0.5 \times 10^{15}/\mathrm{cm}^2$, a 250$\mu$m thick sensor made with oxygenated substrate is almost fully depleted at 250 V, while a non-oxygenated sensor requires 400 V to attain a depth of 250μm.

Fluence [n/cm^2]	Oxygenated	Thickness [μm]	Bias Voltage [V]	Depletion Depth [μm]
0.5×10^{15}	no	280	400	252 ± 10
0.5×10^{15}	no	280	200	147 ± 7
0.5×10^{15}	yes	250	400	$> 242 \pm 8$
0.5×10^{15}	yes	250	250	$> 230 \pm 14$
0.5×10^{15}	yes	250	200	$> 184 \pm 13$
1.0×10^{15}	no	280	600	203 ± 9
1.0×10^{15}	no	280	300	111 ± 10
1.0×10^{15}	yes	250	600	$> 227 \pm 8$
1.0×10^{15}	yes	250	430	$> 225 \pm 14$
1.0×10^{15}	yes	250	400	$> 201 \pm 12$

Table 4: Depletion depth of irradiated pixel sensors as measured in a test beam.

5 Conclusions

Prototype sensors for the ATLAS silicon pixel detector have been electrically characterized. The current and voltage characteristics, charge collection efficiencies, and resolutions have been examined. Devices were fabricated on oxygenated and standard detector-grade silicon wafers. Results are presented from prototypes which examine p-stop and standard and moderated p-spray isolation for a variety of geometrical options. The response of the devices to fluences relevant to LHC operation is examined. The final design selected for ATLAS uses moderated p-spray isolation and the SMD bias grid on oxygenated wafers of thickness 250μm. The pixel cells have dimensions $50\mu\text{m} \times 400\mu\text{m}$, Si_3N_4 passivation, and $\langle 111 \rangle$ crystal orientation. Additional detailed geometrical choices have also been described.

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