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THE ATLAS SILICON PIXEL SENSORS

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ABSTRACT

Prototype sensors for the ATLAS silicon pixel detector have been developed. The design of the sensors is guided by the need to operate them in the severe LHC radiation environment at up to several hundred volts while maintaining a good signal-to-noise ratio, small cell size, and minimal multiple scattering. The ability to be operated under full bias for electrical characterization prior to attachment of the readout integrated circuit electronics is also desired.

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1 Introduction

The ATLAS Collaboration at the Large Hadron Collider (LHC) is now in the process of developing silicon pixel sensors for use in the pixel detector[1]. The sensors must have properties consistent with the detection of a wide range of physics signals[2] while functioning in the challenging environment of the LHC. Performance requirements on the detector as a whole include excellent pattern recognition in a high multiplicity environment, excellent transverse impact parameter resolution and very good three-dimensional vertexing capability, and excellent b-tagging and b-triggering capabilities. These general requirements lead to sensor-specific requirements including small cell size (the exact value of which is set by the electronics design), radiation tolerance (to permit placement very close to the beam), and minimum material (consistent with acceptable assembly yield and safe operation). The ability to be operated under full bias for electrical characterization prior to attachment of the readout integrated circuit electronics is also a desired design feature.

The development program for the pixel sensors includes design of First Prototypes, Second Prototypes, and test structures that are associated with each generation of prototypes and that explore alternatives to the principal prototype designs. This paper describes the First Prototypes and their test structures.

2 Radiation Tolerance Requirements

Table 1 summarizes the total fluence expected for each barrel layer and disk of the pixel system during the ten-year operation time of ATLAS. The sensor characteristics that are most sensitive to radiation are the effective doping concentration, the leakage current, and the charge collection efficiency. The increase in acceptor-like defects leads to an inversion of the conduction type from n to p and subsequently to an increase in the depletion voltage with time. The radiation-induced leakage current results in an increase in noise and power consumption unless the detectors are cooled. Conditions at the location of the innermost layer, or "B Layer," are sufficiently harsh as to necessitate replacement of this layer midway through the experiment.

3 The Sensor Concept

The ATLAS pixel sensors have n-type implants in n-type substrate, a feature that allows them to be operated partially depleted. Such operation might be necessary if the full depletion voltage becomes excessively large after substrate type inversion caused by the high radiation fluence at the LHC. Each First Prototype wafer (see Figure 1) includes two full-size sensors known as Tile 1 and Tile 2 (in Figure 1, Tile 2 is labelled "md") and additional test structures. Most of the additional structures are designed to be read out by a single front-end chip; consequently, these are called single-chip devices. Figure 2 illustrates the general tile concept. Each tile contains 328×144 pixel cells of size $50\mu\text{m} \times 400\mu\text{m}$. These will be connected to 16 front-end chips and will cover a sensitive area of 16.4mm $\times$ 60.4mm. Between chip boundaries, the sensor cells are either elongated from $400\mu\text{m}$ to $600\mu\text{m}$ or are connected to adjacent cells by metal lines (see Figure 3). While the production sensors will have thickness $250\mu\text{m}$ ($200\mu\text{m}$ for the B Layer), the First Prototypes are nominally $300\mu\text{m}$ thick. The ATLAS pixel detector has 1.4×10^8 pixel channels and hence requires 2228 identical tiles. The outer dimensions of the production tiles will depend upon the module concept. The prototype tiles were designed to allow examination of several options, most notably two options concerning the module geometry

Table 1: Maximum predicted annual fluence and integrated ten-year fluence of pixel detector elements. The annual fluence assumes a luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$ and 100 days of operation. The total fluence assumes a linear increase in the luminosity from $10^{33}\text{cm}^{-2}\text{s}^{-1}$ to $10^{34}\text{cm}^{-2}\text{s}^{-1}$ during the first three years. The calculations use the value of $\sigma_{\text{pp inel}} = 80$ mb for the proton-proton inelastic cross section. The detailed pattern of the predicted fluence throughout the pixel detector region can be found in Figure 4-1 of Reference [1].

	r [cm]	z [cm]	Annual Fluence $[\times 10^{13}\text{cm}^{-2}]$	Total Fluence $[\times 10^{14}\text{cm}^{-2}]$
B Layer	4.3	0	34.8	27.84
Layer 1	10.1	0	8.3	6.64
Layer 2	13.2	0	5.0	4.00
Disk 1	12.6	49.5	4.9	3.92
Disk 2	12.6	62.0	4.7	3.76
Disk 3	12.6	67.0	4.7	3.76
Disk 4	12.6	84.0	4.6	3.68
Disk 5	12.6	92.0	4.5	3.60

and two options concerning the n-side isolation (see Section 4.1). Tile 1 has dimensions 18.4mm × 62.4mm and Tile 2, dimensions 21.4mm × 67.8mm.

Pixel implants are connected to front-end electronics by using bump bonding and flip chip technology. The size of the gap between the sensor's n-side and the electronics is determined by the bump height, which is less than 20μm and depends upon the vendor. The smallness of this gap could lead to damage to the electronics through a spark if adequate protection is not provided. For that reason, the entire region of the sensor's n-side external to the active area is covered by an n^+ implant that is grounded externally. A controlled potential drop toward the cut edge on the p-side is achieved by a multiple guard ring structure[3]. This structure consists of 22 rings with a pitch that increases from 20μm to 50μm outward. For protection, the contact holes in the dielectric between the back side diode and the metal lie only in the edge region. The metal on the p-side above each pixel has an aperture of dimensions 30μm × 100μm to allow the pixel to be stimulated by laser light during testing. The bond pads are 18μm diameter circles with circular passivation openings of diameter 12μm. The dielectric layers use $SiO_2 + Si_3N_4$.

4 Details of the Design

4.1 n-side Isolation

Devices that use n^+ implants in an n-type substrate require the inclusion of a structure to maintain high resistance between neighboring cells in the presence of the oxide charge-induced electron accumulation layer at the silicon–silicon dioxide interface. The First Prototypes examined two isolation technologies: p-stop[4] and p-spray[5]. In the case of the p-stop technique, a high dose p-type implant surrounds each n-type region. The p-spray technology involves application of a medium-dose p-type implant to the whole n-side; some regions of the spray are then overcompensated by the n-type pixel implants themselves. Each of the two tiles (and its associated test structures) on a wafer incorporated one of the isolation technologies; p-stop devices were separated from p-spray ones by a low precision mask.

4.2 The p-stop Devices, Including Tile 1

Figure 4 shows the geometry in a corner of Tile 1. Tile 1 uses p-stops of the "atoll"[6] configuration, in which each n-type implant is surrounded by its own p-stop. The gap between the n^+ and p^+ implants was chosen to be 6μm to minimize the inter-implant potential. To conform to the 50μm pitch, the other dimensions were chosen to be: 5μm p-stop width, 5μm gap between neighboring p-stops, and 23μm width of the n-implant itself. An additional p-implant frame surrounds every group of pixels that will be read out by a pair of front-end chips—this feature is intended to further interrupt the accumulation layer and guarantee localization of any problems.

The inner guard ring that surrounds the active region consists of a metallized 86.5μm wide n^+ implant. Its distance from the outermost pixel implant is identical to the inter-pixel separation. Beyond this guard ring is a 10μm wide unimplanted region, then a 10μm wide p^+-implanted ring, then a second 10μm wide unimplanted region. The region beyond this is implanted with n^+-type material and is grounded externally as discussed above.

Each First Prototype wafer contains, in addition to the tiles, three single-chip devices with all the features of Tile 1. These are referred to as ST1 devices. Other single-chip devices were also included to test various p-stop geometries. These include two devices with common p-stops, one with a common p-stop and p-spray, one that examines eight different combinations of atoll and combined p-stop geometries, and one that includes bricking (see Section 4.6).

4.3 The p-spray Devices, Including Tile 2

Figure 5 shows the geometry of Tile 2. Tile 2 and related test structures utilize p-spray. In the First Prototypes, Tile 2 pixel cells had 13μm wide n^+ implants that were surrounded by 6μm wide floating n^+ rings.[1)] During operation, the floating ring is charged by the detector's dark current, and the electrostatic drift field is focused on the pixel implant.

Each wafer contains three single chip sensors with all the features of Tile 2. These are known as ST2 devices. Also included is one with a simpler design known as SSG. The SSG, which eventually evolved into the design that forms the baseline for the production sensors, has a 37μm wide n^+ implant and a gap of 13μm between adjacent pixels. This is the same size gap as is used between the floating n^+ rings in the ST2 design. The floating n^+ rings are not present in the SSG design, and the bias grid (see Section 4.4) is implemented in a simplified form, as is shown in Figure 6. An n^+ implanted line runs perpendicular to the pixel cells between alternate columns. When biased, it contacts every pixel implant by punchthrough.

Each wafer also includes three p-spray devices whose dimensions are optimized to minimize cross talk and one that evaluates several implant geometries and bricking patterns.

On the basis of results presented in Section 6, p-spray was ultimately chosen as the isolation technology for the ATLAS pixel detector.

4.4 The Bias Grid

It is anticipated that quality assurance of the production sensors will include measurement of leakage current versus bias voltage ("I-V") for each tile. This measurement

[1)] In a revision of the design, the floating rings were eliminated and the implants enlarged.

requires that the entire sensor be biased uniformly beyond full depletion. To facilitate uniform application of the potential to every pixel cell, a structure known as the bias grid is integrated into the p-spray devices. Figure 7 shows a detail of it. A bus line from the inner guard ring runs between every other pair of columns and is connected to a small n^+-implant dot near each pixel. Application of voltage to any point in the grid of bus lines (e.g., through a probe needle at the inner guard ring) causes every pixel to be biased to the same potential by punchthrough from its neighboring dot. Once the sensor has been bump bonded to its front-end chip, the pixels are biased via the electronics and the grid becomes inoperative. It does hold any pixels that are unconnected to the electronics (e.g., due to a bonding failure) at a potential close to ground. In the First Prototypes, the bias grid occupies 0.8% of the total sensitive area of the sensor.

4.5 Double-metal

One-third of the prototypes were fabricated with a double-metal process. The second metal is used for signal routing in regions not directly accessible to readout chips, in some bricked regions, and as bus lines in the insensitive area along the side of the array. The bus lines are arranged in the same way as are those in Figure 3 but in this case are in the second metal, rather than the first metal, layer. The second metal bus lines were placed within the region accessed by one read-out chip and on the side opposite to that which uses single metal; this placement facilitates a comparison of the two routing layers' effects upon capacitance and cross coupling.

4.6 Bricking

Bricking refers to pixel cells that are offset in neighboring rows by one-half of the pixel length. Bricking was included in several of the single chip structures (see for example Figure 8) to determine its value in improving the z-resolution of tracks with double hits and in reducing the cross talk by distribution of capacitance. Including bricking in the ATLAS design requires some modification to the shape of the bias grid. A significant design challenge is posed by the requirement that the bricked arrays have the same bump pad pattern as do the unbricked arrays, so that both can be tested with the same front-end electronics. Section 6.5 compares the measured properties of bricked and unbricked sensors.

5 Sensor Specifications

Table 2 summarizes the requirements that were placed upon the First Prototype sensors. The p-spray implantation dose is adjusted to the saturation value of the oxide charge in order to achieve an optimal compromise between low fields and good isolation. While no requirements were placed upon the devices' radiation tolerance for acceptance from the manufacturers, tests of the maximum operating voltage, average leakage current per pixel, and total leakage current after irradiation by 10^{15} p/cm^2 were conducted. The results of those tests are presented below.

6 Performance of the Prototypes

6.1 The Wafers

Twenty-six First Prototype wafers were delivered for testing: 10 single-metal and 6 double-metal from CiS (Centrum für intelligente Sensorik), Germany, and 7 single-

Table 2: Specifications of the First Prototype sensor wafers.

Property	Specification
Uniformity of wafer thickness	10μm
Mask alignment	$\leq 2\mu$m
Initial depletion voltage (for a 300μm wafer)	50–150 V
Initial operating voltage	> 200V
Initial leakage current (at V_{depl})	< 100 nA/cm^2
n^+-implant dose	$> 10^{14}$cm^{-2}
p-stop implant dose	$> 10^{13}$cm^{-2}
p-spray implant dose	$(3.0 \pm 0.5) \times 10^{12}$cm^{-2}
back side p-implant dose	$> 10^{14}$cm^{-2}
implant depth after processing	$> 1\mu$m

metal and 3 double-metal from Seiko, Japan. Some of the properties of these wafers are summarized in Table 3.

Table 3: Properties of the First Prototype sensor wafers.

Property	CiS	Seiko
Thickness	280 μm	300 μm
Crystal orientation	$\langle 111 \rangle$	$\langle 100 \rangle$
Depletion voltage	105 V	45 V
Effective dopant concentration	1.7×10^{12}cm^{-3}	6.6×10^{11}cm^{-3}
Flat band voltage	4.5 V	1.5 V
Sheet resistances:		
p-side	105 Ω/square	129 Ω/square
n-side: n^+-implants	110 Ω/square	171 Ω/square
n-side: p-stops	1.3 kΩ/square	0.6 kΩ/square
p-spray implant dose	2.6×10^{12}cm^{-2}	3.2×10^{12}cm^{-2}
Electron mobility near p-spray surface	67 cm^2/Vs	356 cm^2/Vs

6.2 Electrostatic Characterization

The leakage current of every tile and single-chip device was measured as a function of applied bias voltage, since I-V characteristics are a useful means for detecting fabrication defects. Figure 9 shows the setup for I-V measurements. Two probe needles are placed on the p-side, one on the active area and one at the wafer edge or device scribe line. The contact to the edge or scribe line is shorted to the n-side. Prior to full depletion, the pixels are shorted and are consequently all at the same potential. They become isolated once the applied voltage exceeds the depletion voltage. At voltages above V_{depl}, each pixel's current crosses by thermionic emission to the nearest n^+ implant between it and the bias structure or guard ring. The voltage drop between neighboring pixels depends upon the contact geometry, the current level, and the p-side voltage. In devices with bias grids, the number of gaps between each pixel and the bias structure is three, so all pixels have the

same potential. In devices without bias grids, the potential of each pixel depends upon its distance from the guard ring.

I-V measurements were initially made on the unbumped, undiced wafers, then subsequently after each step required for connecting the sensors to their front-end chips, and finally after all assembly was completed. All measurements were made in clean environments. Measurements on fully assembled devices were performed with analog and digital ground connected but power off in order to ensure reproducible temperature conditions. No step in the assembly process produced a change in a device's I-V characteristic that is associated with damage.

Figures 10–13 show the I-V characteristics of all of the tiles that were delivered. Figures 14–15 histogram the breakdown voltages of the Tile 1-like and Tile 2-like single chip devices. The breakdown voltage is defined as the voltage associated with the intersection point between a straight line fitted to the curve below the current rise and a straight line fitted to the curve in the region where the current is rising.

Devices with p-stops appear to show a more homogeneous behavior than do p-spray devices. The homogeneity is, however, an artifact introduced by the potential gradient across the device. The I-V curves of the tiles with bias grids are more directly interpretable due to the uniformity of the potential across all pixels. This becomes evident when the I-V measurements are redone after flip chip assembly, at which time the potential gradient is no longer present on the p-stop devices.

Devices with p-stops generally show a rise in the current at about 200 V for the CiS devices and 160 V for the Seiko devices. The current rise is also present in the associated single-chip devices. The p-spray devices show a similar pattern, with the current rise typically occurring at 200 V for the CiS devices and between 110 V and 140 V for the Seiko devices. The tiles can be classified into three groups by their I-V characteristics: Group 1 includes devices that break down at or below full depletion. These are likely to have a mechanical defect. Group 2 includes devices that can be operated above full depletion but that show a slow (but acceptable) current rise above full depletion. The origin of this current rise is not understood. Group 3 includes devices that can be operated at voltages above full depletion without evidence of the current rise found in Group 2.

6.3 Radiation Tests

To investigate the behavior of the prototypes after radiation doses comparable to those expected at the LHC, one wafer from each manufacturer was diced and its single-chip devices irradiated. Irradiations were performed using a 300 MeV pion beam at the PSI Laboratory, Switzerland, and a 55 MeV proton beam at Lawrence Berkeley National Laboratory (LBNL) in the U.S.A. Three Tile 1-like single chip devices and three Tile 2-like single chip devices each received a fluence equivalent to 2.4×10^{14} n_{eq} cm^{-2}, where n_{eq} represents a particle with the non-ionizing energy loss of a 1 MeV neutron. Two Tile 1-like single chip devices and two Tile 2-like single chip devices each received a fluence of 1.1×10^{15} n_{eq} cm^{-2}. The irradiations were performed at room temperature, and no bias was applied to the sensors during irradation. I-V measurements were subsequently made at various temperatures below $-10°C$ and normalized to $-10°C$ according to the equation

$$I(T) \propto (kT)^2 e^{-E/2kT},$$

where $E = 1.21$ eV, T is absolute temperature, and k is Boltzmann's constant. There is agreement among results from the pion and proton irradiations, and among results from

devices by the different manufacturers. Example plots from CiS devices irradiated at the PSI are used here to illustrate the results.

The I-V characteristics of some irradiated single-chip devices are shown in Figures 16 (for p-stop) and 17 (for p-spray). The irradiated p-stop devices break down at about 200 V while the p-spray devices withstand voltages up to at least 500 V without evidence of breakdown. The measured currents are consistent with those expected purely from bulk damage.

Figures 18 and 19 show the results of inter-pixel resistance measurements of irradiated p-stop and p-spray devices. Around zero volts an ohmic behavior can be observed that corresponds to a resistance of 8.9 MΩ for the p-spray device and 26 MΩ for the p-stop device. These values are sufficient for reliable operation of the devices even after a high irradiation dose. The measurements were made at room temperature without application of bias voltage and so are considered to be conservative estimates of the values that would be obtained for biased (depleted) sensors.

6.4 Pixel Cross Coupling

Several sensor cell geometries were studied using assemblies of single chip devices connected to electronics chips[1] via the bump bonding and flip-chip technology. Each assembly includes 1/16 of the number of pixel cells that appear in a module (an assembled tile); this is 2880 active pixels, each with amplifying electronics. The assemblies utilize two different versions of the prototype front-end electronics chip, called FE-A/C and FE-B. They were characterized in the laboratory with test pulses and radioactive sources and in high energy test beams (see below).

We define cross coupling as the fraction of the charge deposited in one pixel cell but observed in an adjacent cell due to the inter-pixel capacitance. The cross coupling leads to a cross talk hit only if it is above the threshold set by the discriminator. The amount of cross coupling associated with a given configuration of sensor cell and front-end electronics cell depends on the sensor cell design (mostly via the backplane and inter-pixel capacitances) and on the preamplifier circuit's response behavior and time characteristics. Therefore the absolute measured value of the cross coupling depends on the specific circuitry of the front-end and on its operational settings, including its feedback current, preamplifier speed, and discriminator speed. We summarize here results that are common to both front end chips and that are specifically related to the pixel sensor design.

In the central region of the detector, cross coupling between nearest neighbors dominates other contributions. The typical measured values are about 5% or less. The cross coupling of Tile 2 cells is about half that of Tile 1 cells. At the boundary of the pixel array, where pixel columns have cells of length 600μm rather than 400μm, the higher inter-pixel (and consequently total) capacitance causes the measured cross coupling to be about 20% larger than in the interior. In the rows near the sensor array edge, some of the pixels are connected as pairs (see Section 3 and Figure 3) in order to retain sensitivity to tracks in the region not directly covered by electronics. The extra metal lines associated with these pixel cells induce additional capacitance. Measurements of cross coupling in this region show that the direct cross coupling between neighboring pixel cells is about 5–10%. This number can increase by as much as a factor of two when pixels are connected by metal lines.

6.5 Test Beam Studies

Several single chip assemblies were studied in a 180 GeV pion beam at CERN by using a beam telescope composed of four silicon microstrip detector pairs. A detailed description of all the results of the studies can be found elsewhere[7]; here only results that are particularly relevant to the sensor design are reported.

The ability of the electronics to record time over threshold made it possible to measure the charge collected by the pixels. The charge collected by the pixels was studied as a function of the point of impact of traversing particles relative to a pair of pixel cells. Figures 20 and 21 show the average charge collected as a function of positions x and y, where the coordinate axes are parallel to the short (50μm) and long (400μm) edges of the pixels, respectively, and are centered (in x) at the center of a single pixel and (in y) between two adjacent pixels.

For hits not at the pixel center, the signal is shared between several pixels. The sum of the pixel measurements is given. The electronics threshold was set at 2000 electrons during these measurements.

Regions with reduced charge collection were observed for some designs; these could be explained by specific design features. These regions are located at the center of the plots in y or at the edges of the pixels in both x and y.

For the Tile 2 design, charge loss was observed at all edges of the pixel. A possible explanation of this is that the n^+ implant ring that surrounds the main pixel implant (and which was introduced to minimize inter-pixel capacitance) did not float as it should, due to the presence of a current path not evident in the two-dimensional simulations used to optimize the design. It consequently collected signal charge of which part was then lost due to capacitive coupling to parasitic nodes (e.g., the bias grid).[2)] At the end of each Tile 2 pixel that is directly adjacent to the bias grid, two charge loss effects combine: the capacitive effect described above and a direct loss to the implanted bias dot. In this region a relatively large amount of charge loss is visible, extending approximately $\pm 50\mu$m into the pixel region in the y direction; this loss profile corresponds roughly to the geometry of the bias structure.

The first charge loss effect is absent from the SSG design, which has no n^+ implant ring. Results for this design show only a small charge collection inefficiency at alternate gaps, corresponding to the presence of the bias grid, which includes an n^+ implantation line. A new design which minimizes the size of the implanted region is being tested.

Tile 1 and related single chip sensors show only a small charge collection inefficiency on all sides of each pixel. The small gap between the individual p-stop rings acts (due to electron accumulation) like a small n^+ region.

The bricked design was tested with a single chip assembly in the test beam to verify that its resolution is as expected. This sensor has 400μm long pixels; those in adjacent columns are displaced by 200μm in the long direction. For a non-bricked design, the residuals along the long dimension of the pixel with respect to the track incidence point form a flat distribution extending from -200μm to $+200\mu$m with an rms mean value of 115μm. For a bricked design one expects the same behavior for single-hit clusters, while for clusters of two or more hits the residuals should have a flat distribution from -100μm to $+100\mu$m with an rms mean value of 58μm. The overall resolution depends upon the fraction of clusters with two or more hits. The resolution of the bricked sensor was measured for angles between 0 and 30°. The fraction of clusters with two or more hits

[2)] A study using three-dimensional simulation is in progress to better understand this.

varied from 46% at 0° to 98% at 30°. The resolution as a function of the track incidence angle is shown in Figure 22. No variation in the x-direction resolution was observed relative to the non-bricked design.

7 Summary and Conclusions

The features and performance of the first ATLAS pixel sensor prototypes have been presented. These prototypes were fabricated with n-type implants in an n-type substrate to allow them to be operated partially depleted if necessary. The prototypes performed well after irradiation to fluences appropriate to the LHC environment. P-spray was selected over p-stops as the n-side isolation technology because of its superior response to radiation and because it allows implementation of a bias grid that facilitates testing. The design of the bias grid has been iterated for optimal charge collection. The observed level of cross coupling is acceptable with the discriminator thresholds expected to be used in operation.

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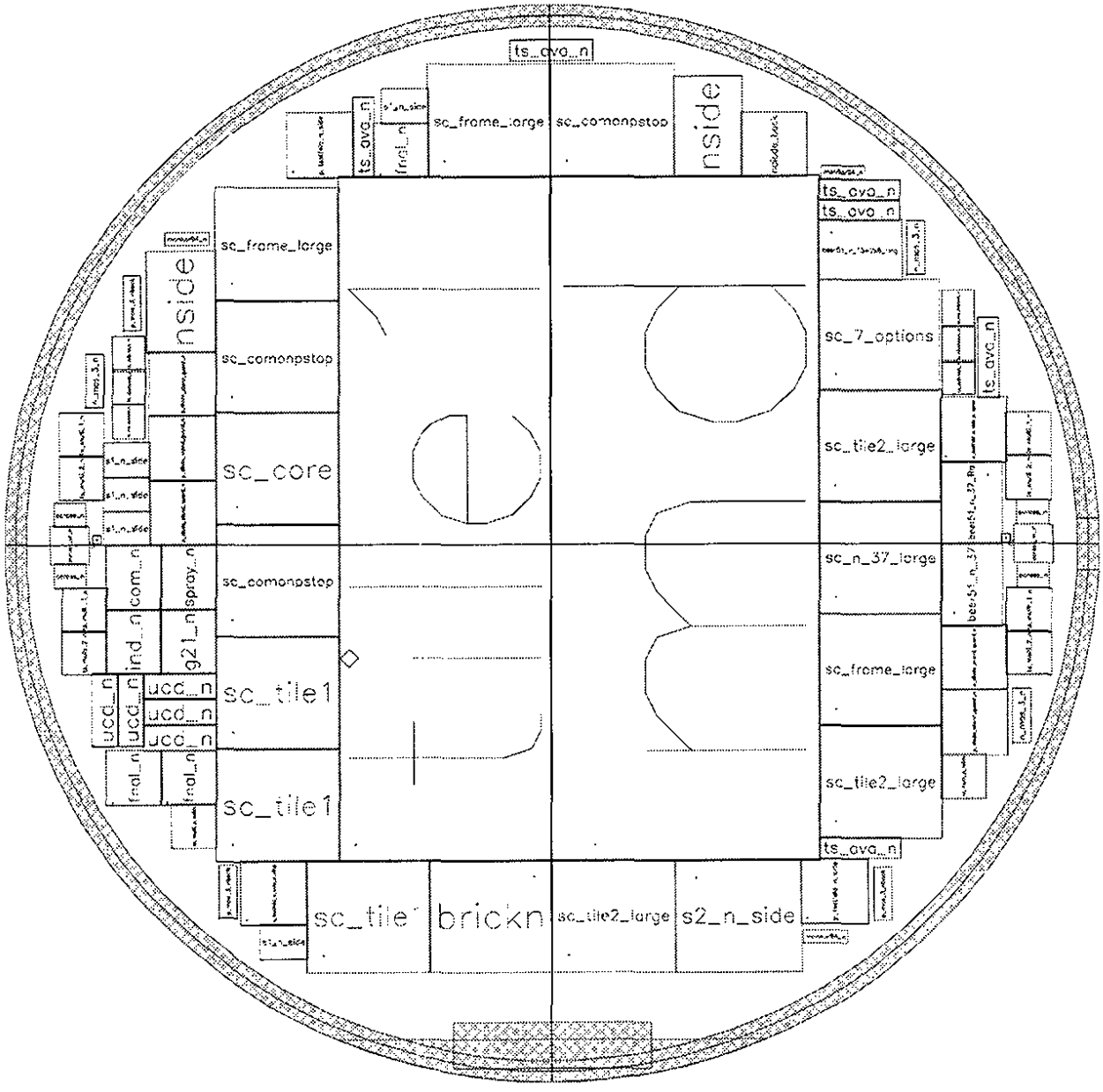

Figure 1: The first ATLAS pixel sensor prototype wafer.

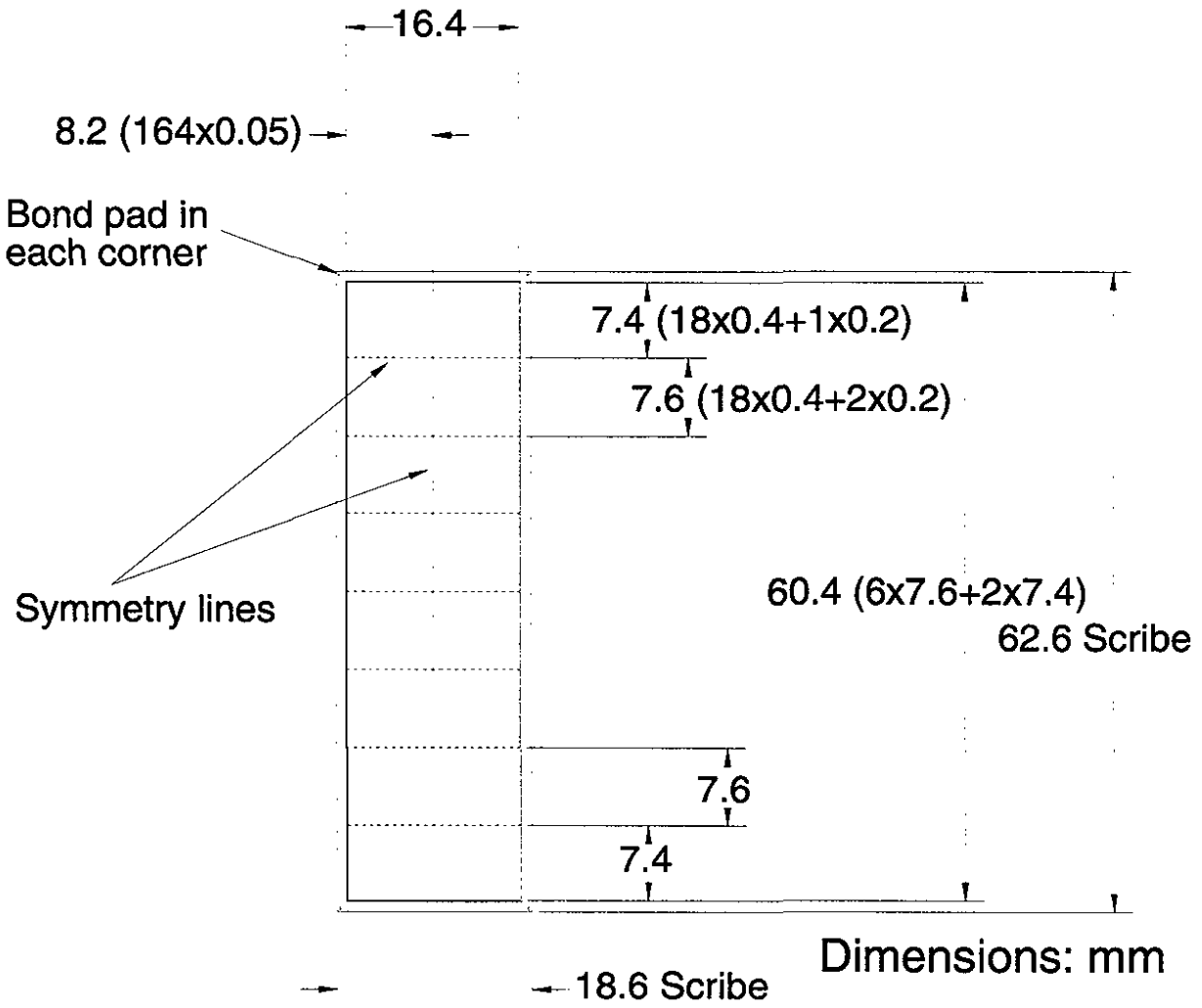

Figure 2: The tile concept.

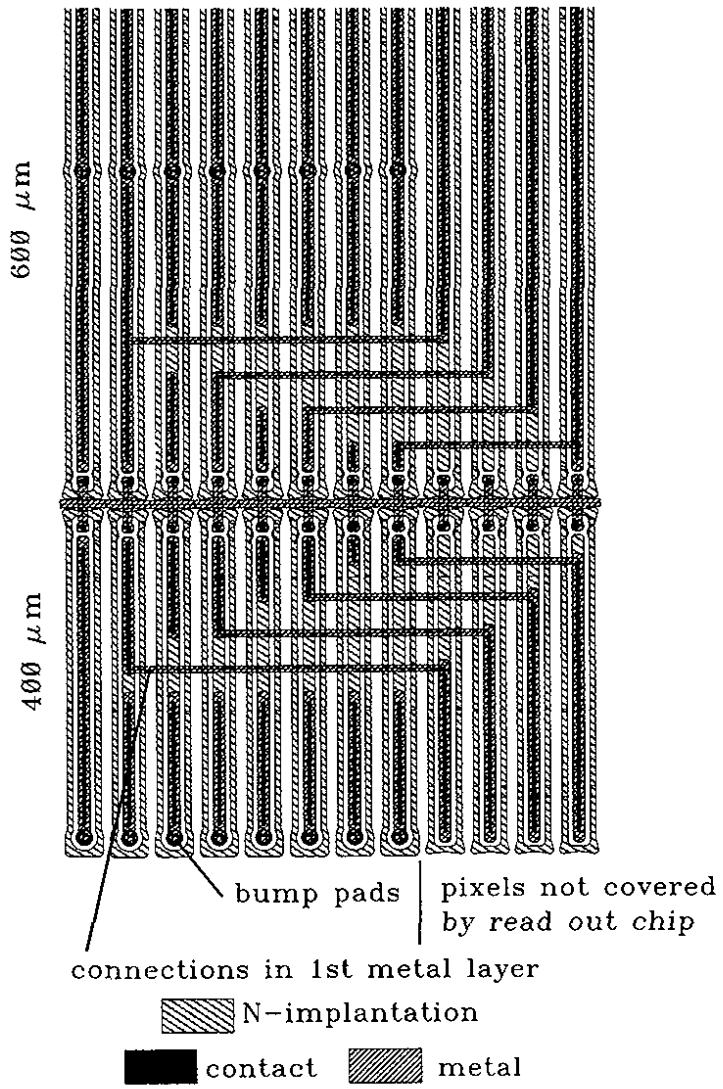

Figure 3: Detail of the Tile 2 design showing first metal traces that route signals from implants at the edges of their units to the preamplifers above neighboring implants.

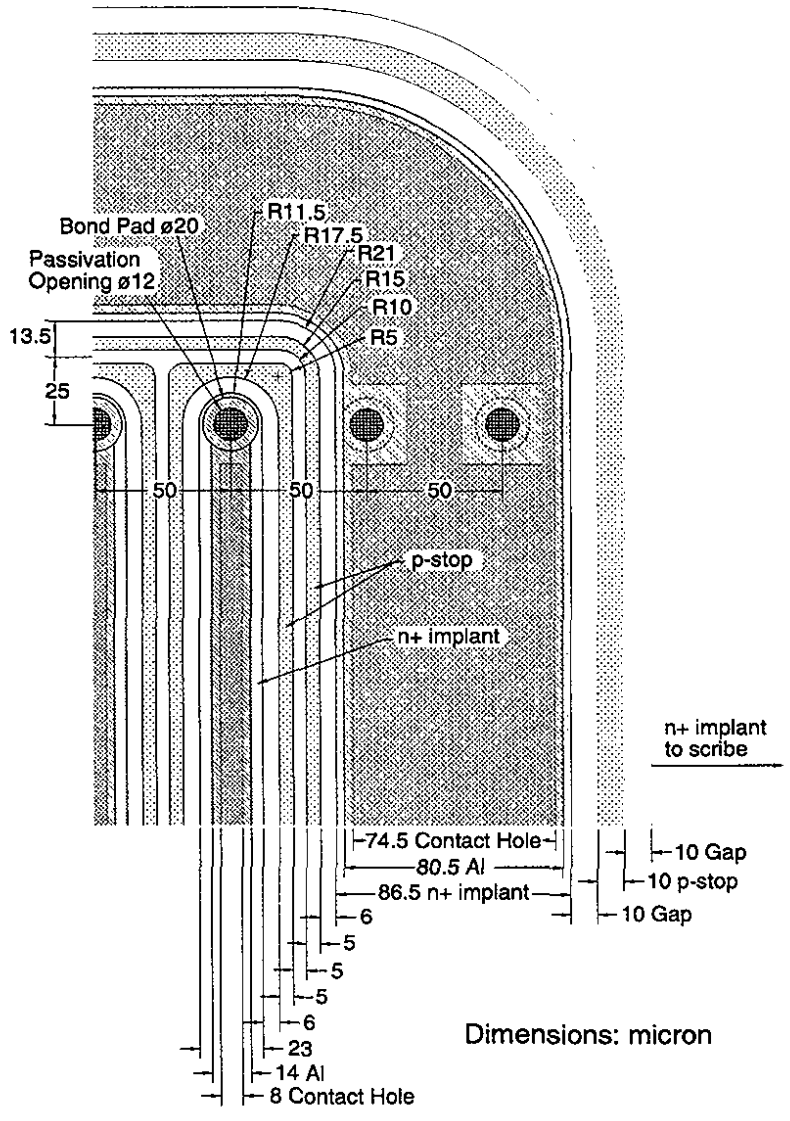

Figure 4: Detail of Tile 1 showing the corner of the n-side guard ring and the isolation implants.

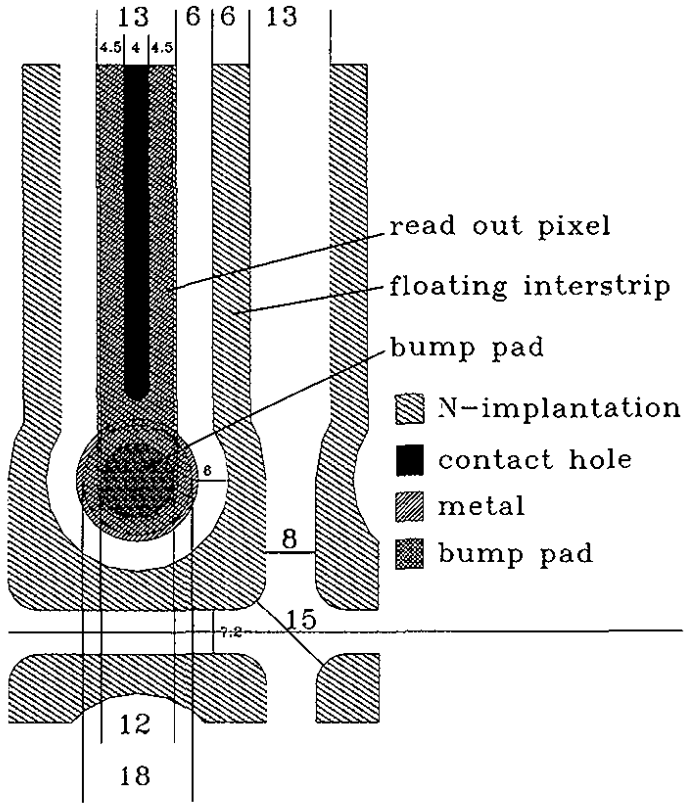

Figure 5: Portion of a pixel cell in Tile 2.

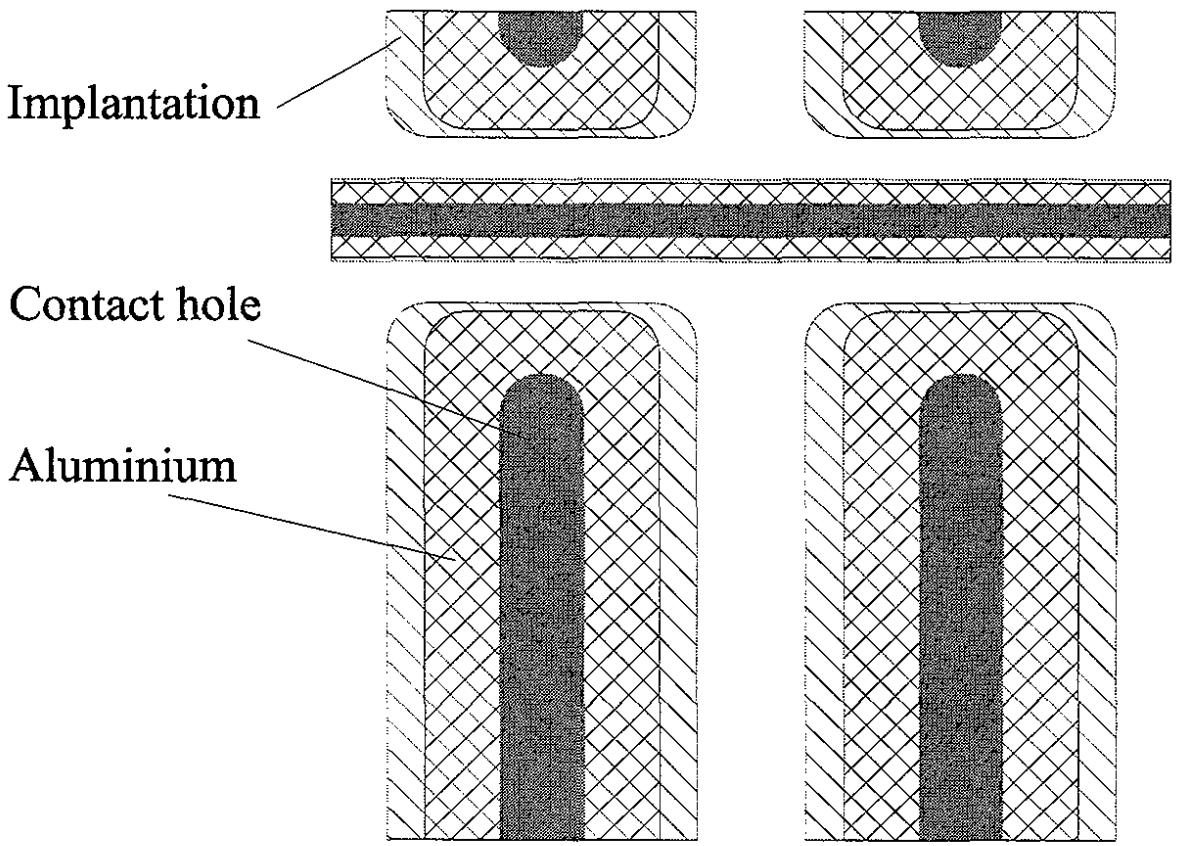

Figure 6: A section of the SSG single-chip sensor showing several adjacent pixels. The horizontal line represents a segment of the bias grid.

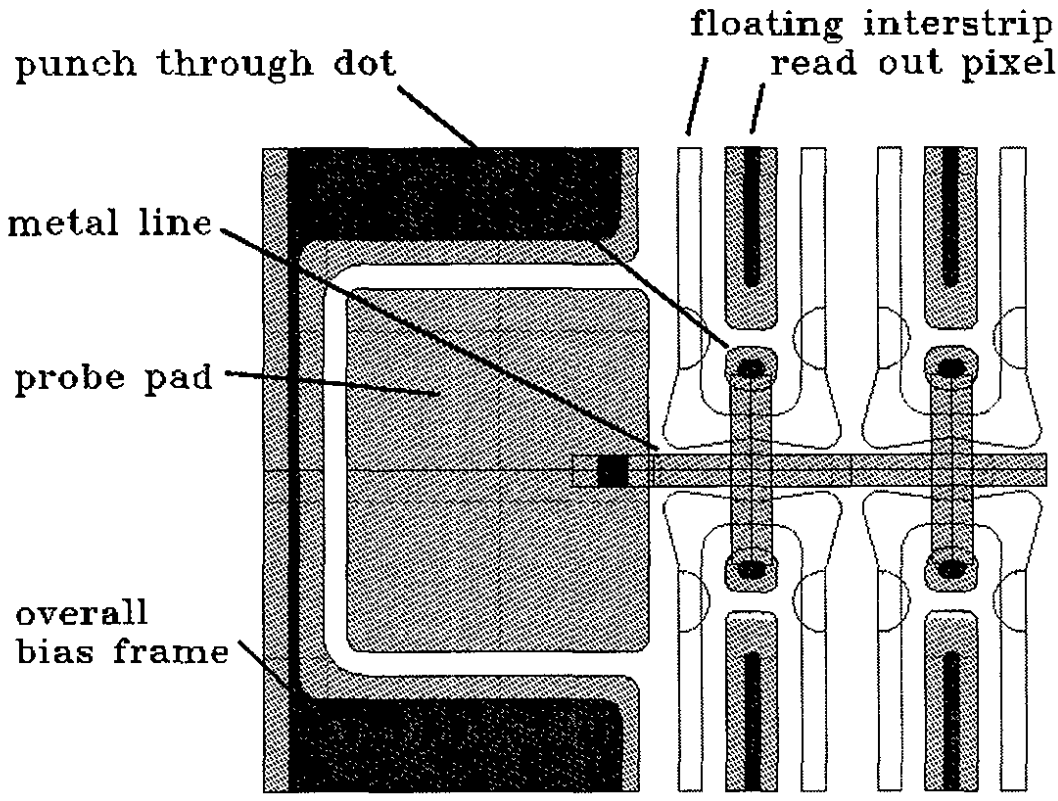

Figure 7: A section of the bias grid.

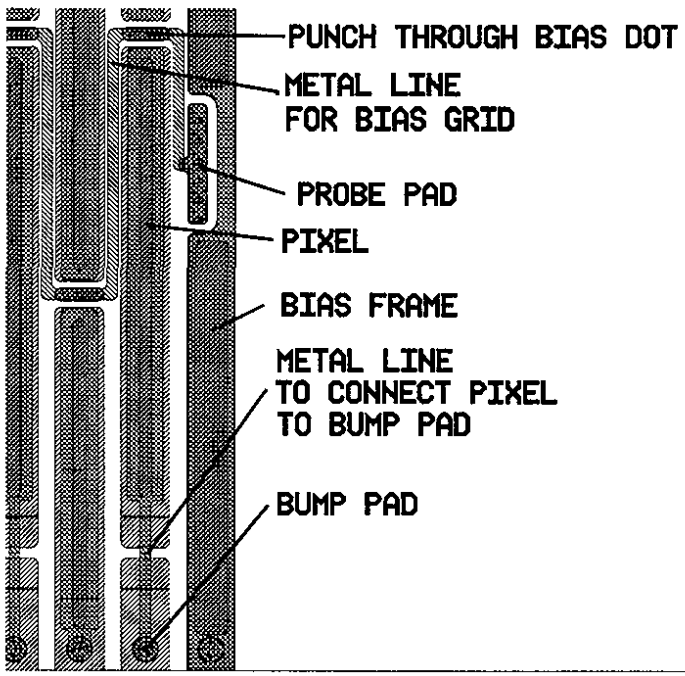

Figure 8: A section of the bricking pattern used in one of the single chip sensors.

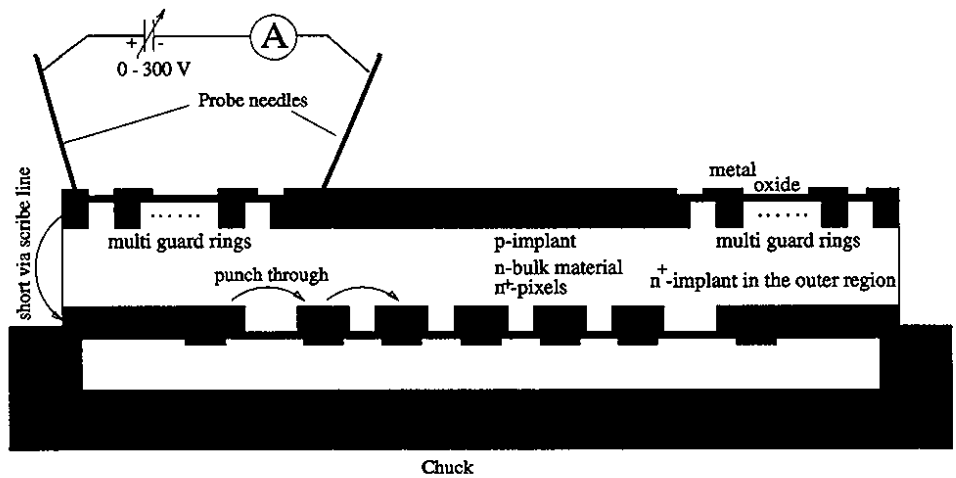

Figure 9: The setup for measurements of leakage current versus applied bias voltage (I-V) curves.

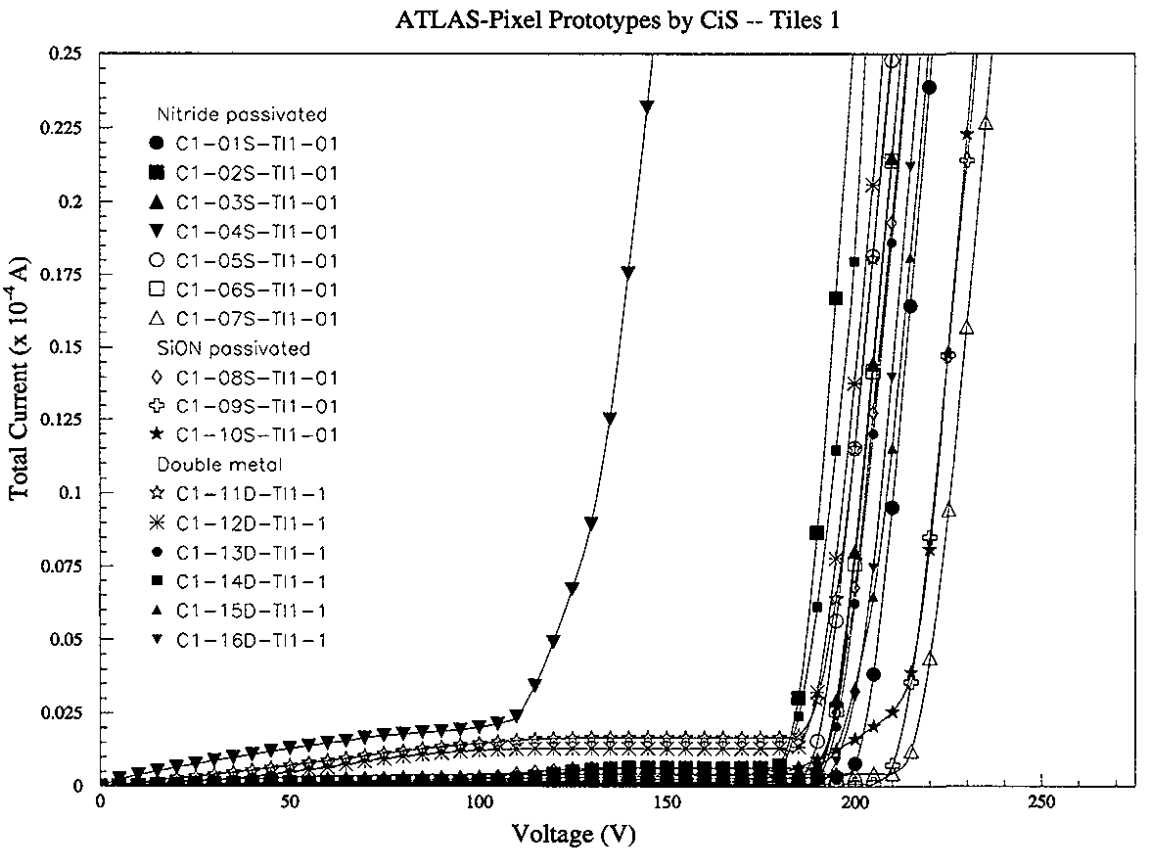

Figure 10: I-V curves measured at room temperature for the Tile 1 sensors fabricated by CiS.

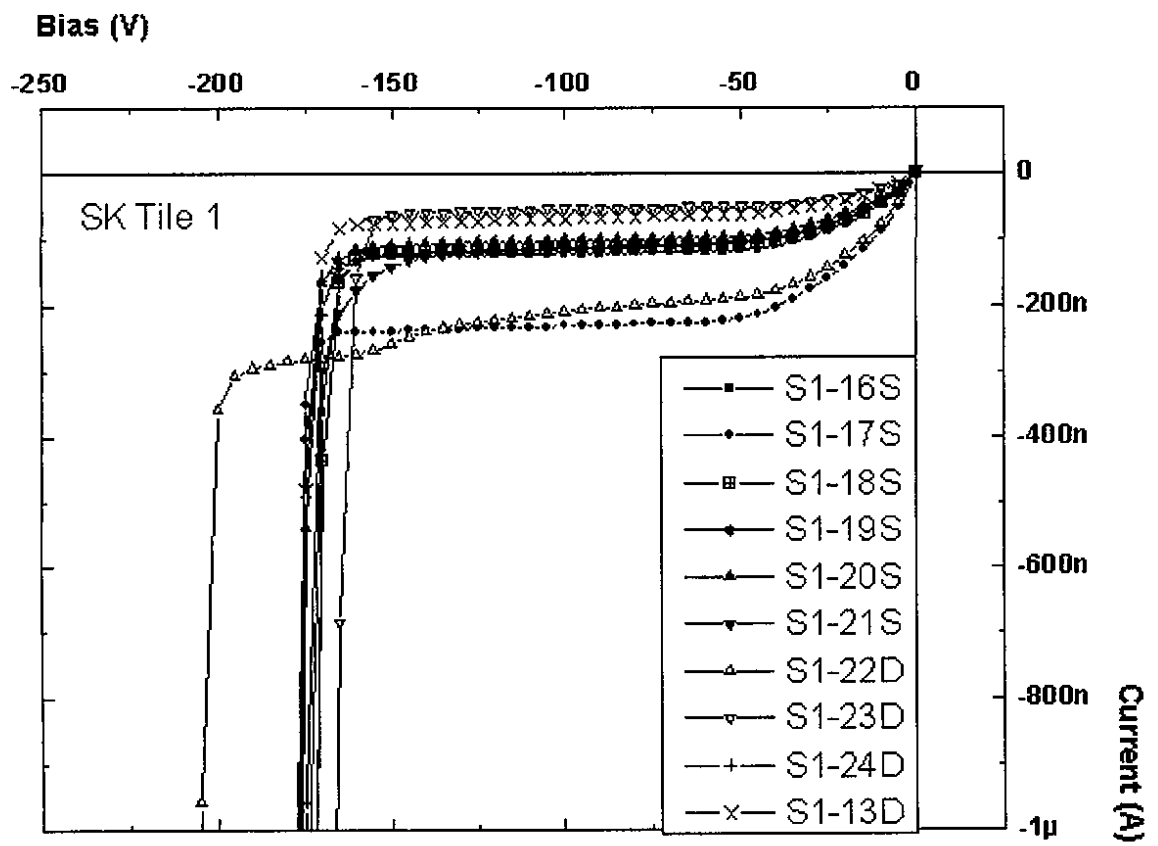

Figure 11: I-V curves measured at room temperature for the Tile 1 sensors fabricated by Seiko.

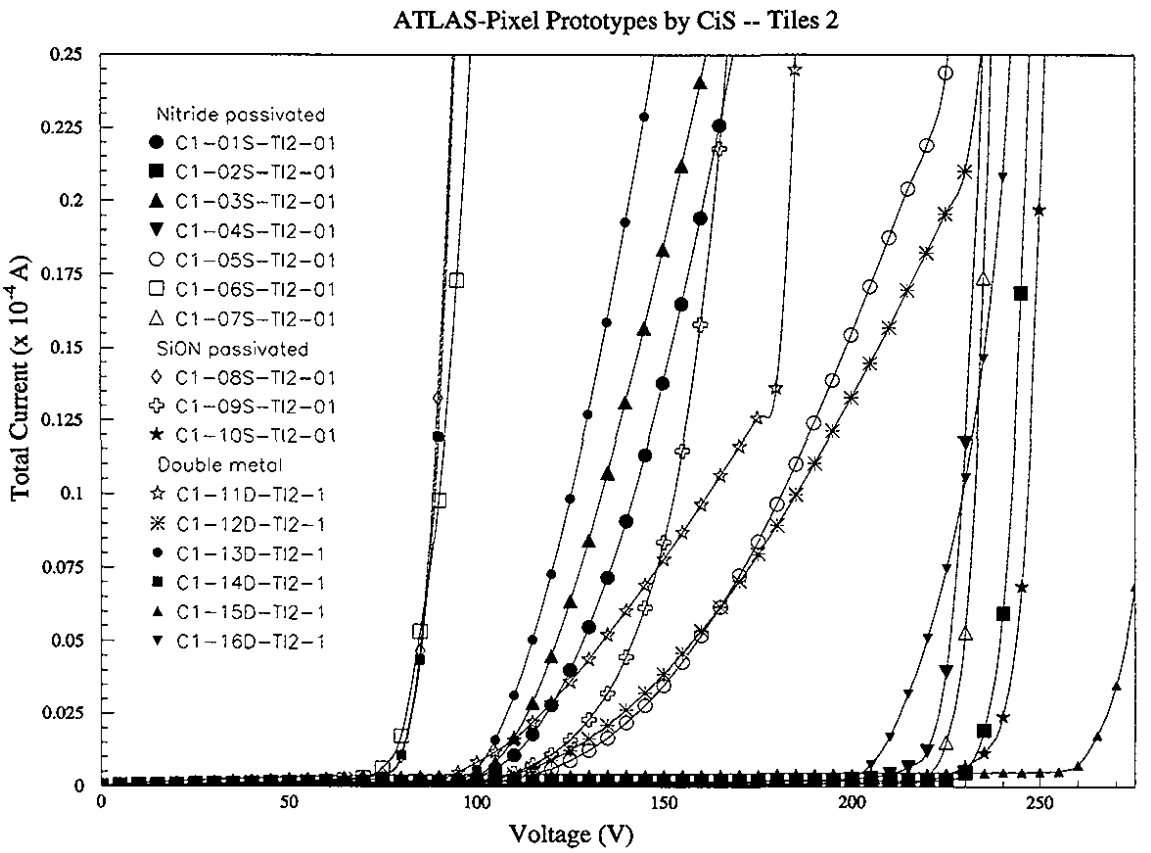

Figure 12: I-V curves measured at room temperature for the Tile 2 sensors fabricated by CiS.

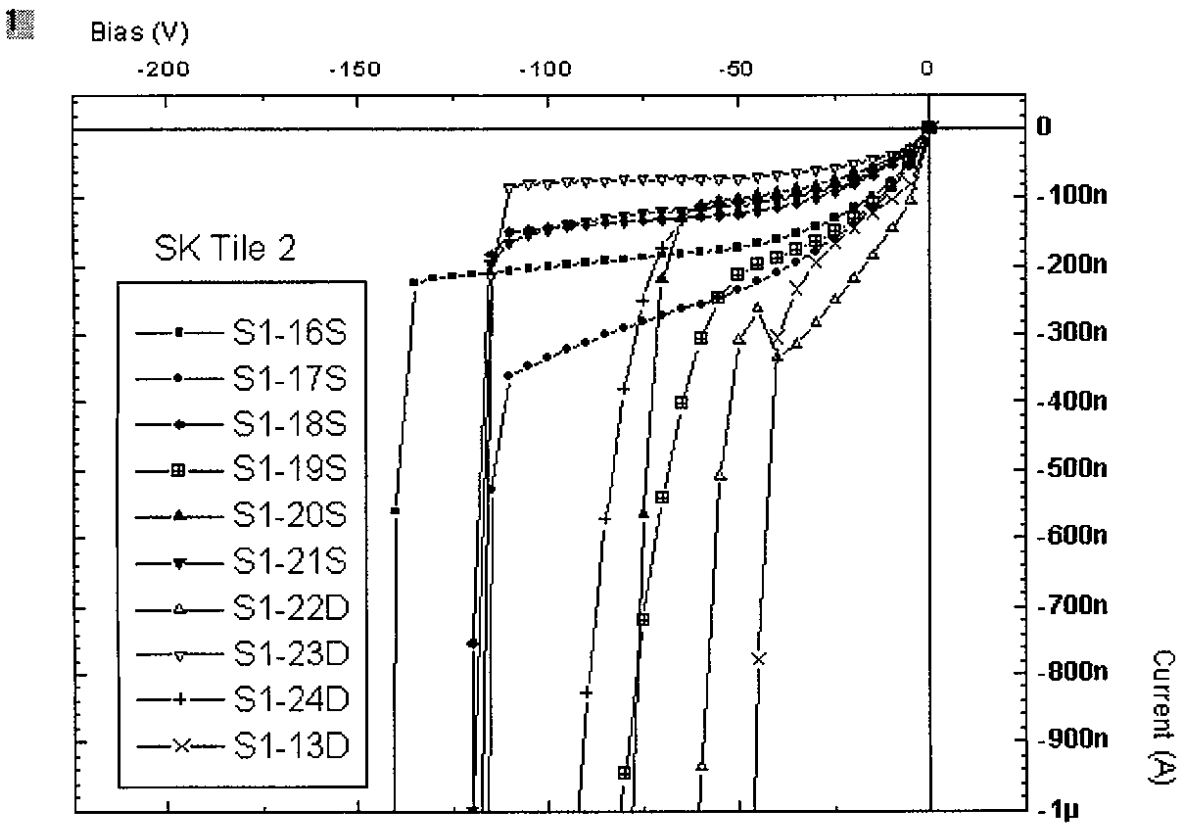

Figure 13: I-V curves measured at room temperature for the Tile 2 sensors fabricated by Seiko.

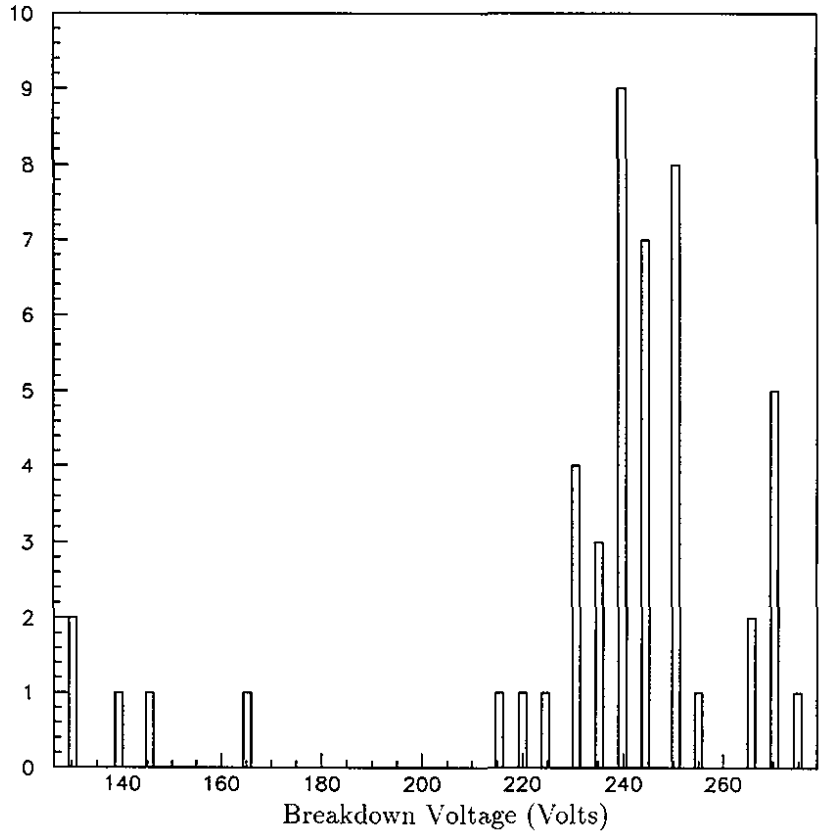

Figure 14: Breakdown voltages of the Tile 1-like single chip sensors fabricated by CiS and Seiko.

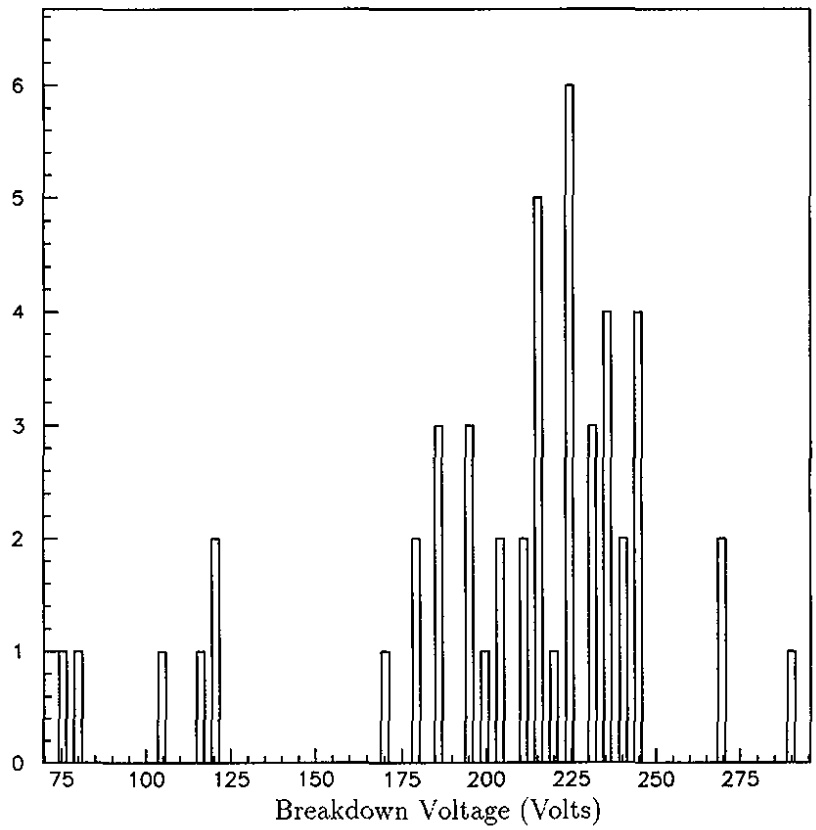

Figure 15: Breakdown voltages of the Tile 2-like single chip sensors fabricated by CiS and Seiko.

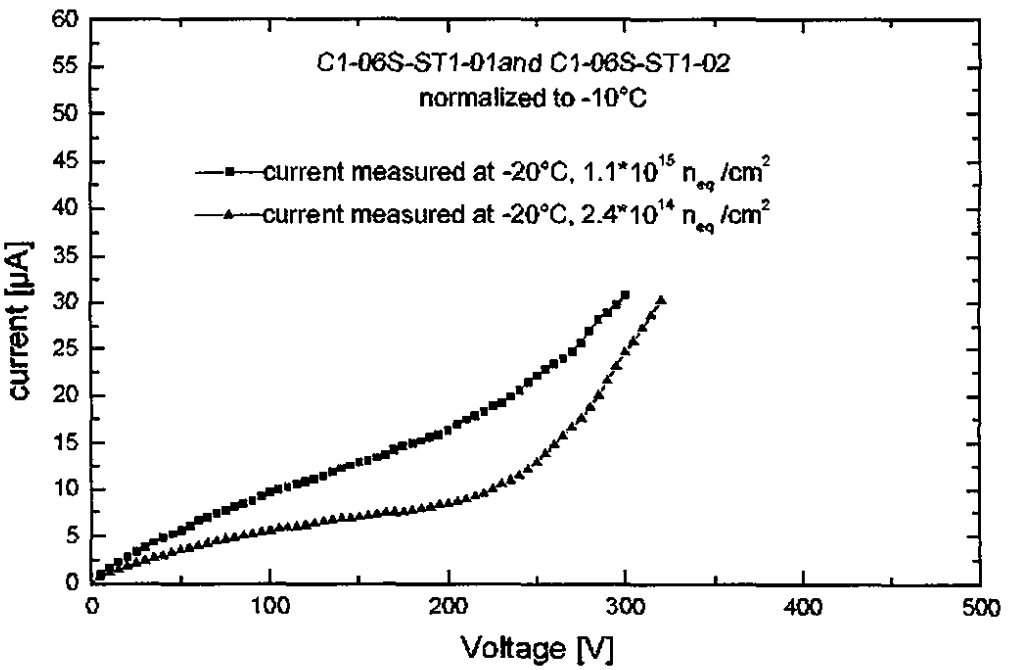

Figure 16: I-V characteristics of two irradiated single-chip sensors with p-stops. The upper curve is for a device that received 1.1×10^{15} n_{eq} cm^{-2}. The lower curve is for a device that received 2.4×10^{14} n_{eq} cm^{-2}. Both measurements are normalized to $-10°C$.

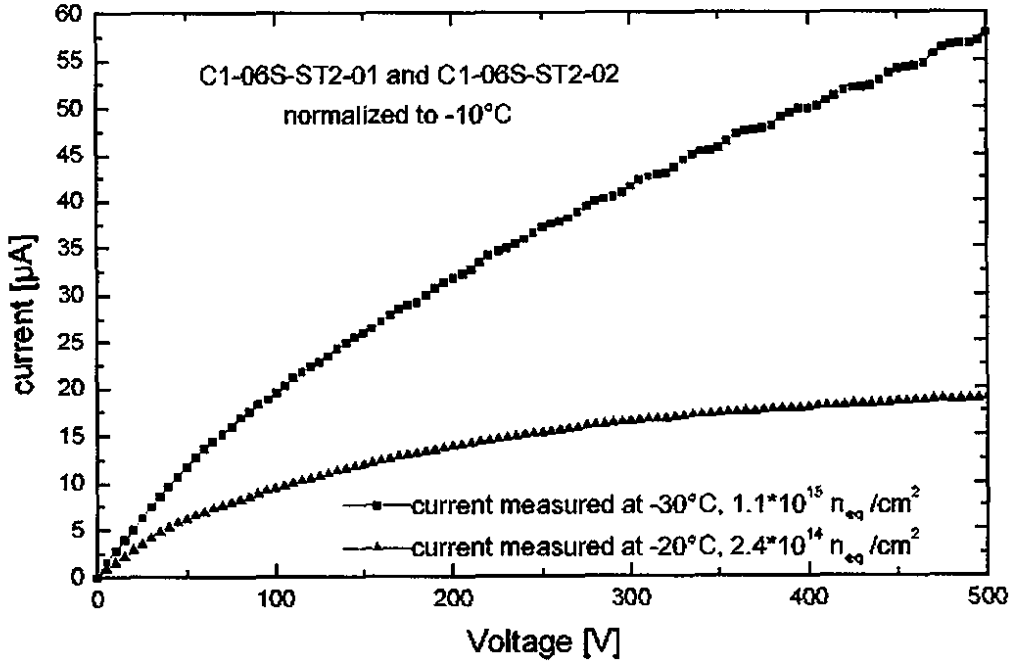

Figure 17: I-V characteristics of two irradiated single-chip sensors with p-spray. The upper curve is for a device that received 1.1×10^{15} n_{eq} cm^{-2}. The lower curve is for a device that received 2.4×10^{14} n_{eq} cm^{-2}. Both measurements are normalized to $-10°C$.

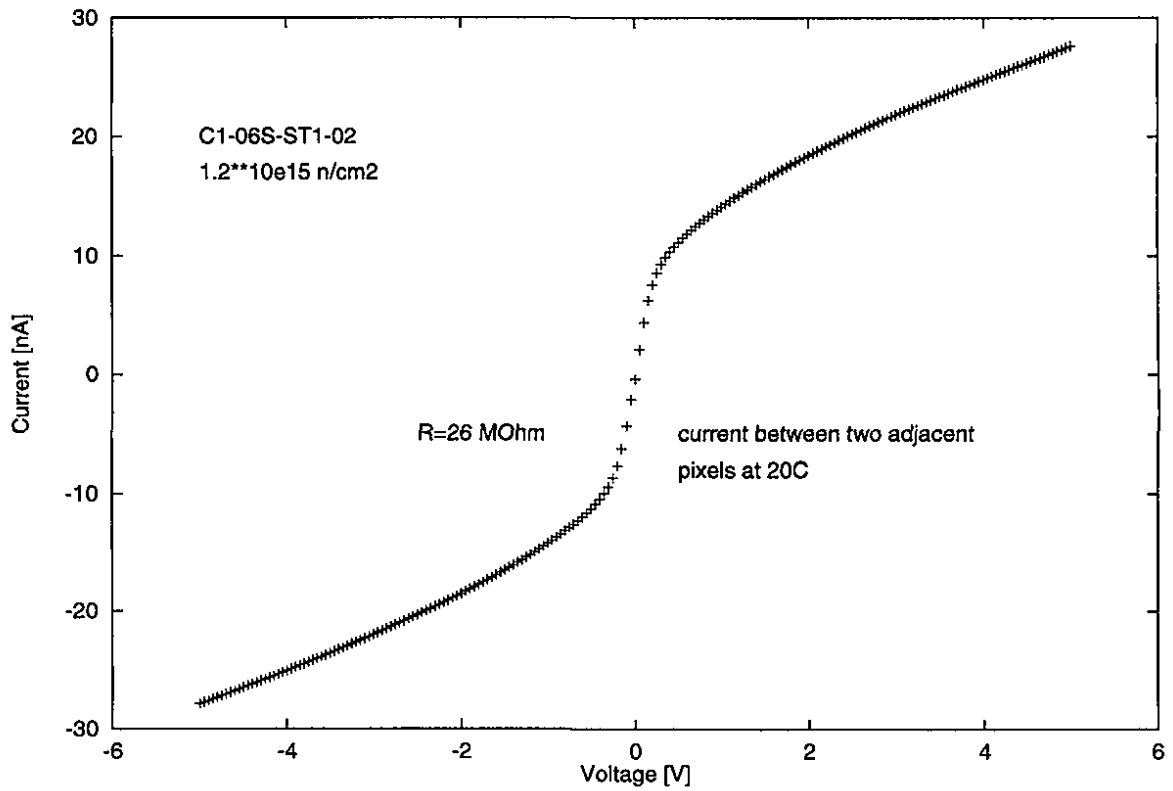

Figure 18: The leakage current between two adjacent pixels in a highly irradiated single-chip device with p-stop isolation, as a function of the potential difference between them. The slope of this curve gives the inter-pixel resistance. The measurement was made at room temperature without p-side bias.

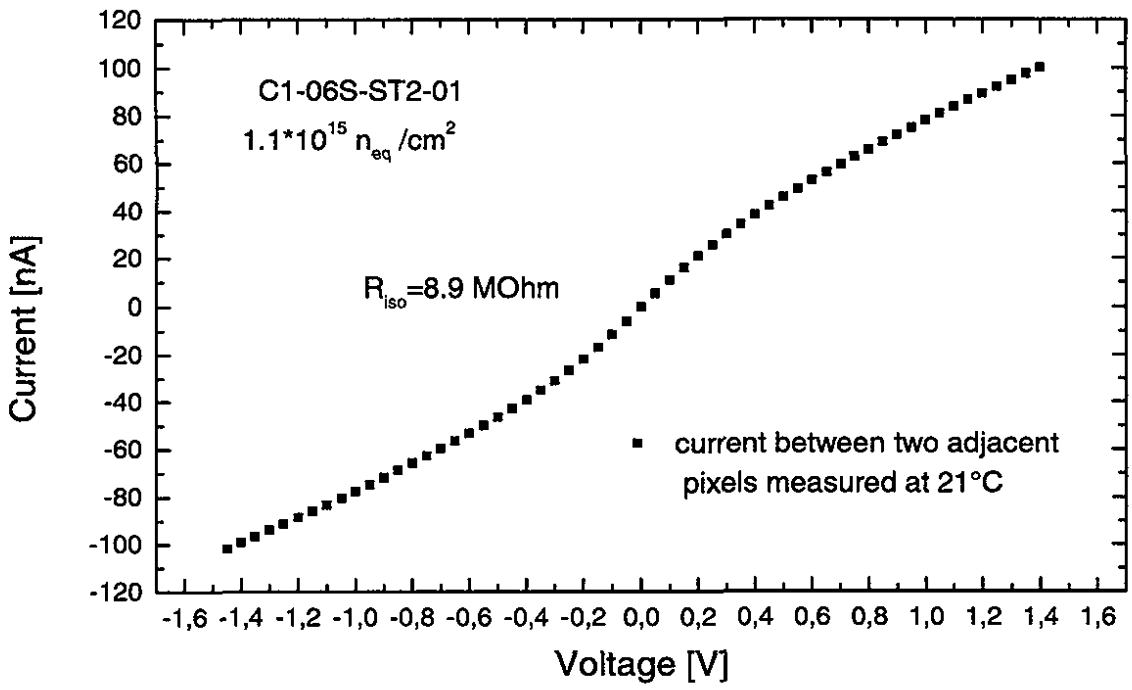

Figure 19: The leakage current between two adjacent pixels in a highly irradiated single-chip device with p-spray isolation, as a function of the potential difference between them. The slope of this curve gives the inter-pixel resistance. The measurement was made at room temperature without p-side bias.

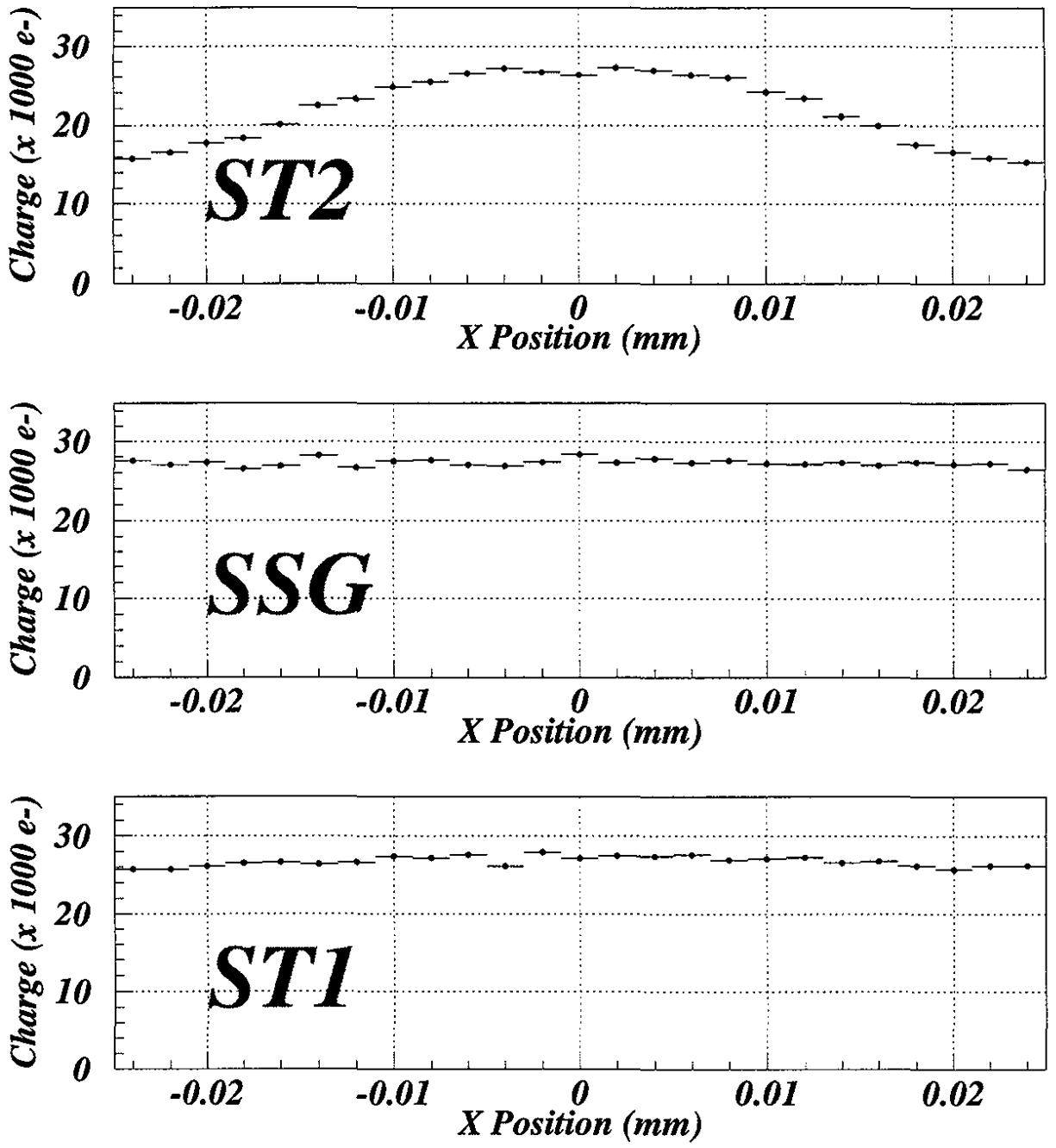

Figure 20: The average collected charge as a function of the position within a pixel cell of short dimension 50μm for Tile 2 (ST2), Tile 1 (ST1), and SSG sensors. The total charge of the clusters is shown in units of thousands of electrons.

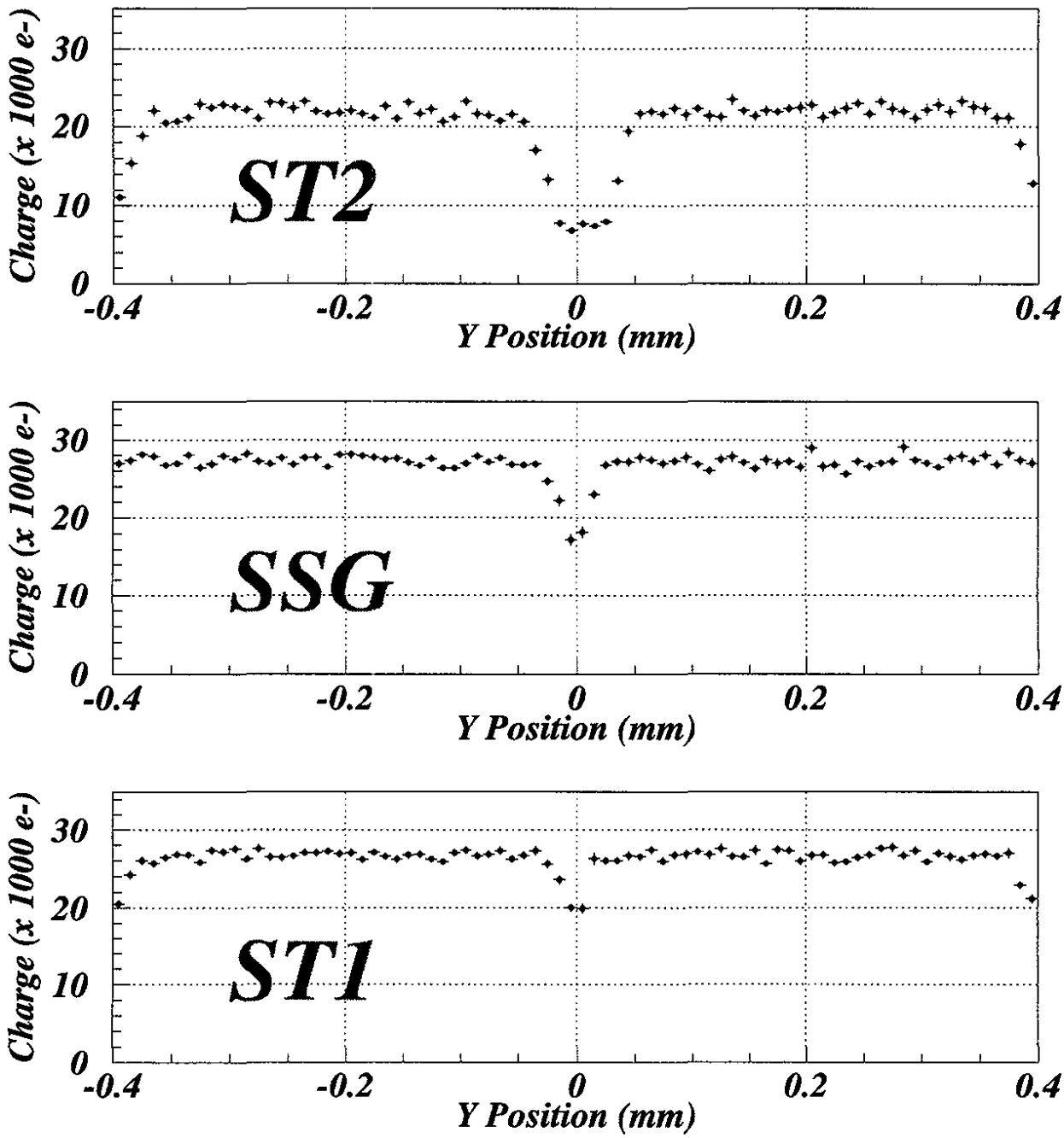

Figure 21: The average collected charge as a function of position relative to a pair of pixel cells of long dimension $2 \times 400\mu$m for Tile 2 (ST2), Tile 1 (ST1), and SSG sensors. The total charge of the clusters is shown in units of thousands of electrons.

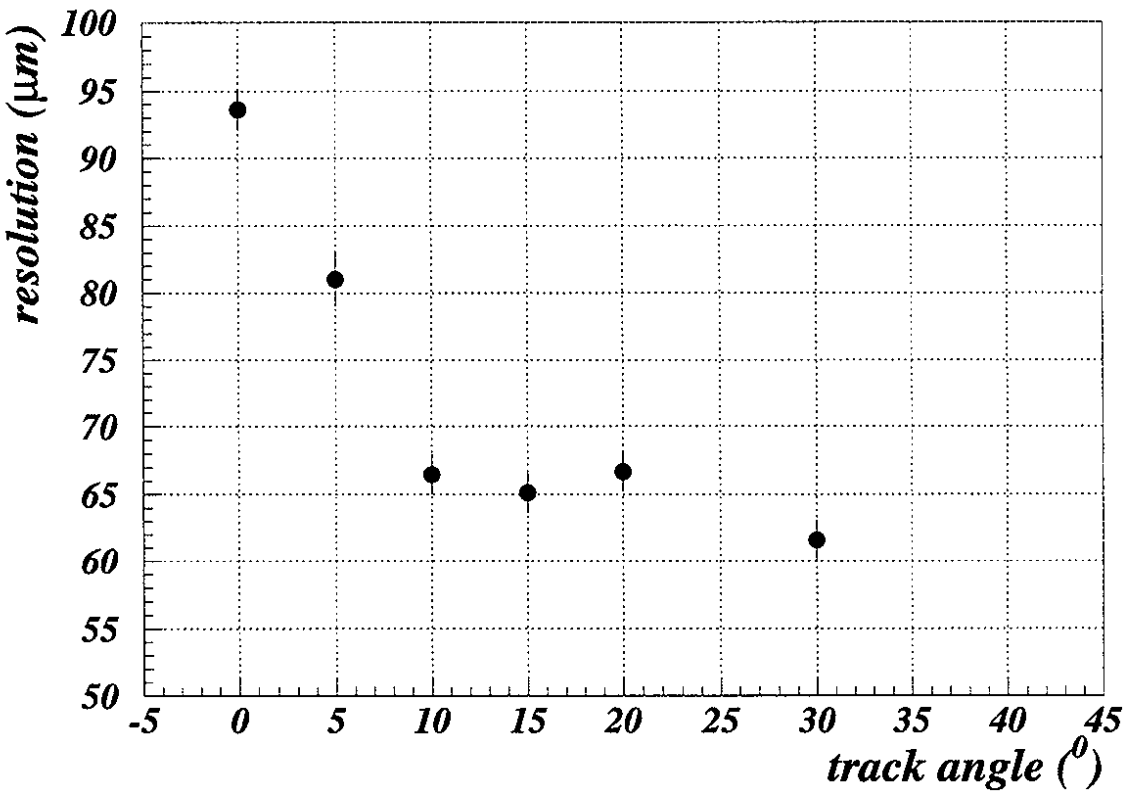

Figure 22: Resolution in the long dimension of the bricked pixel sensor as a function of the track angle with respect to the normal to the sensor.

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[7] The ATLAS Pixel Collaboration, "Beam Test Results on Silicon Pixel Detectors for the ATLAS Experiment," to be submitted to *Nucl. Instr. and Meth.*