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A Charge Injection System for the TileCal CAEN ADCs

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Abstract

We present a summary of the design, operation and performance of the Charge Injection System (CIS) developed and used in the TileCal testbeam to calibrate the CAEN ADCs.

1 Introduction

We report here on the design of the CIS for use in calibrating standard gated ADC systems. In particular the CIS was first used in the April, 1996, combined Liquid Argon-TileCal testbeam run in H8A at CERN for ATLAS. The TileCal calorimeters were readout with 12-bit CAEN ADC's with high and low gains, the gain factor being about 7.5.

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We have built 220 channels of CIS which was originally intended to replace the existing Precision Pulse Generator (PPG) system. The CIS allows us to inject known charges between 0 and 1000 pC into any combination of ADC channels. The charge and channel selection is programmable through VME and can be varied at each pulse if desired. Thus the CIS can be used to calibrate attenuation in long cables, measure gain and linearity of the ADC channels, and to test trigger systems.

2 CIS Overview

In Figure 1 we show a general block diagram of the layout of the CIS as used in the April, 1996, testbeam run. There are three basic components to the system:

1. A VME-based Controller
2. A CAMAC Crate-based CIS Controller
3. A CAMAC Crate-based CIS Module

Near the calorimeter, the cables from the calorimeter are routed into the inputs of the **CIS Modules**. In the case of the testbeam, the calorimeter signals are routed first into the Cs integrator boxes, then into the inputs of the CIS Modules as shown. The CIS Modules reside in a CAMAC crate and are controlled by the **CIS CAMAC Controller**. The outputs of the CIS Modules connect directly to the ADC inputs. In the testbeam this connection was made through 40 m of RG58 cable. Communication between the CIS Crate Controller and the **CIS VME Controller** is done through 40 m of a 50-conductor twisted-pair cable. The VME Controller generates the trigger pulse used to dump the charge stored in each of the enabled CIS channels and after a programmable delay, generates a pulse which triggers the ADC gating system.

The CIS Crate Controller uses a 16-bit DAC to set the voltage to each of the CIS Modules, where each CIS channel uses 100 pf, 1% capacitors to store the charge. Before every CIS pulse, the VME Controller can tell the

CIS crate what the DAC setting is and which CIS channels to enable. The VME Controller then generates or passes a trigger pulse to discharge the capacitors into the CIS outputs.

In Section 3.1 we will describe the VME Controller. Section 3.2 will discuss the CIS Crate Controller and Section 3.3 will discuss the design of the CIS Modules. In Sections 4.1 and 4.2.3 we will present the results obtained on the CIS operation. Finally in Sections 4.2.1 through 4.2.3 we document the software as it exists at the TileCal testbeam.

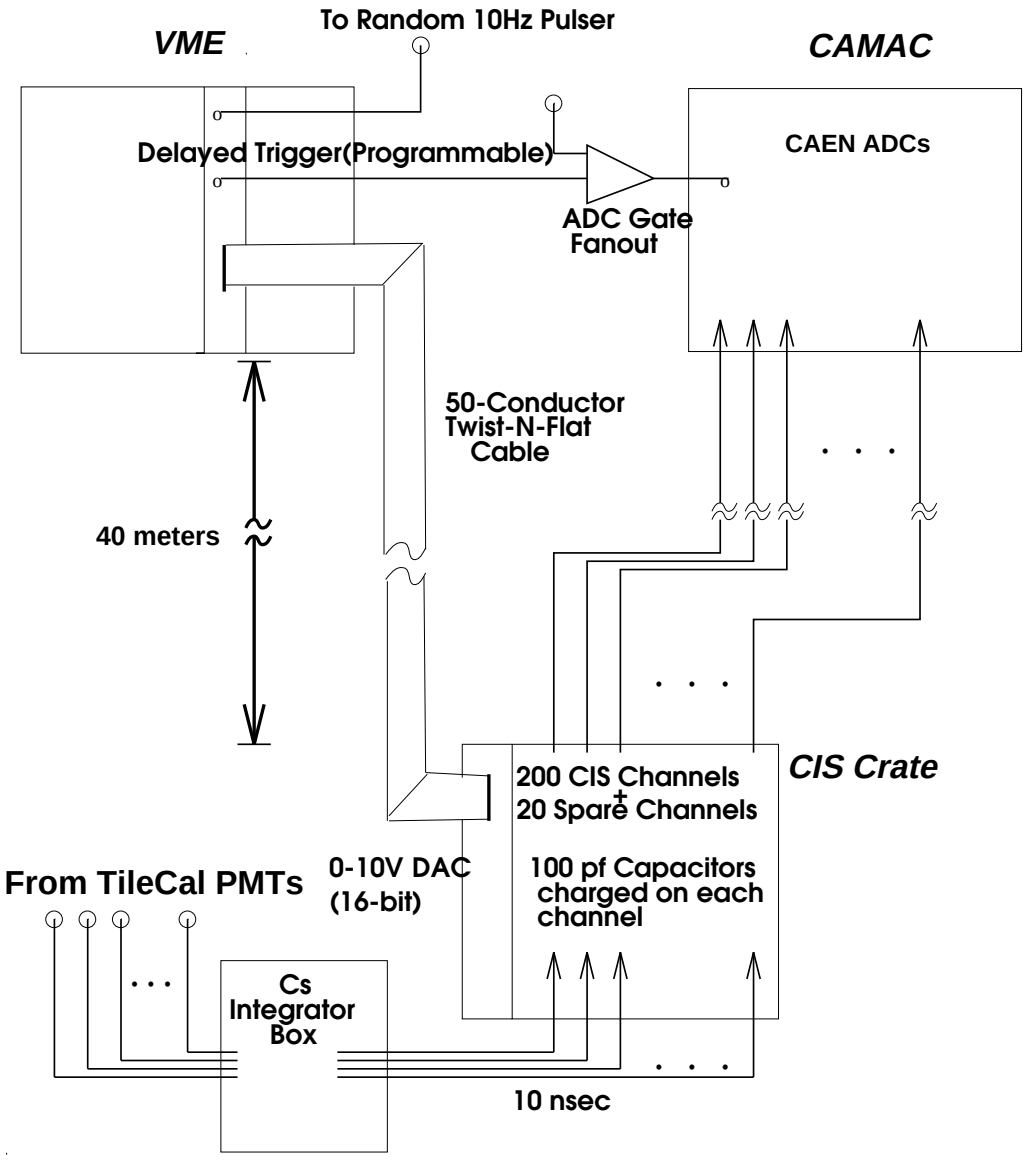
Charge Injection System -- Block Diagram
To Random 10Hz Pulser
VME
CAMAC
Delayed Trigger(Programmable)
CAEN ADCs
ADC Gate
Fanout
50-Conductor
Twist-N-Flat
Cable
40 meters
CIS Crate
200 CIS Channels
+
20 Spare Channels
From TileCal PMTs
0-10V DAC
(16-bit)
100 pf Capacitors
charged on each
channel
Cs
Integrator
Box
10 nsec

Figure 1:

3 Electronics Detail

3.1 CIS VME Controller

In Fig. 2 we show a functional block diagram of the VME controller. Besides incorporating logic to decode VME addressing, the Controller's function is the following:

- Generate triggers to the CIS crate to discharge the capacitors,
- Generate a delayed pulse to gate the ADCs,
- Send the DAC voltage setting to the CIS Crate Controller,
- Send the pattern of which CIS channels to enable or disable.

Communication with VME is through either A32/D32 or A24/D16, jumper selectable. Communication with the CIS crate is through a 50-conductor twisted pair cable. Communication to the fast electronics is through three input LEMO connectors.

The trigger is selected in either of four ways: external NIM trigger, internal 100 Hz oscillator, VME written trigger, and trigger off. Furthermore, the trigger is enabled *only* if there is a NIM true level at the CALFLAG LEMO input or if the CALFLAG latch is set directly from VME to enable the triggers. The latter was the mode of operation in the testbeam. A NIM level at the VETO input will also veto output triggers. Furthermore, a 100 ns pulse will be outputted the GATE OUT LEMO after a programmed delay time. This delay is 300 nsec fixed + 0-128 nsec programmed. This delay accommodates the trigger pulse going out and the injected charge returning to the ADCs on 40 m of cable.

Writing 10-bit words at 23 VME addresses permit the enabling of individual CIS channels. If a bit is set in the 10-bit word, that CIS channel will be enabled for calibration. If the bit is not set, then the channel will bypass the charge injector completely.

The charge to be injected is set by sending 2 bytes to the CIS Crate Controller's 16-bit DAC: the low byte is sent first, and at the receipt of the

second byte, the data is latched into the DAC.

The VME address is defined always with the following protocol:

- VME Address Space: A31-A1
- DIP Switch Space: A31-A9
- A1=0 Always
- Jumper F23 sets address - data mode:
  - A=32 bits of address - 32 bits of data
  - B=24 bits of address - 16 bits of data

Table 1 gives the VME address space and the appropriate functions to be performed. Figures 3 through 8 show construction schematics of the CIS VME Controller.

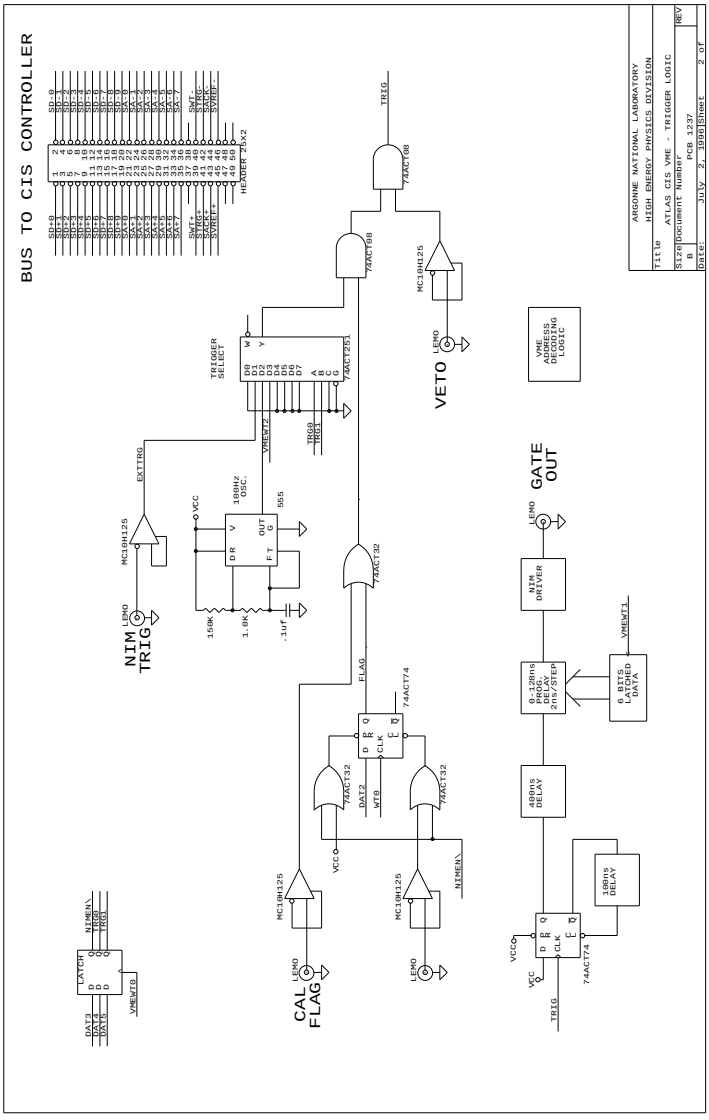

Figure 2: Functional diagram of VME Controller.

Table 1: VME Address and Commands

Address	Bits	Data	Function
\$000	0	1/0	Set/Unset Start Of Run latch
	1	1/0	Set/Unset Start Of Burst latch
	2	1/0	Set/Unset Calibration Flag latch
	3	1/0	Set/Unset NIM Disable latch
	4-5	0	Select No trigger
		1	Select external NIM trigger pulse
		2	Select 100 Hz internal oscillator
		3	Select VME trigger pulse
\$004	0-5		Read/Write Gate Delay (2ns/step)
\$008			Write VME Trigger Pulse
\$104	0-9	1/0 in bit	Enable/Disable CIS Channel CAMAC slot 1
\$108			Enable/Disable CIS Channel CAMAC slot 2
\$10C			Enable/Disable CIS Channel CAMAC slot 3
\$110			Enable/Disable CIS Channel CAMAC slot 4
\$114			Enable/Disable CIS Channel CAMAC slot 5
\$118			Enable/Disable CIS Channel CAMAC slot 6
\$11C			Enable/Disable CIS Channel CAMAC slot 7
\$120			Enable/Disable CIS Channel CAMAC slot 8
\$124			Enable/Disable CIS Channel CAMAC slot 9
\$128			Enable/Disable CIS Channel CAMAC slot 10
\$12C			Enable/Disable CIS Channel CAMAC slot 11
\$130			Enable/Disable CIS Channel CAMAC slot 12
\$134			Enable/Disable CIS Channel CAMAC slot 13
\$138			Enable/Disable CIS Channel CAMAC slot 14
\$13C			Enable/Disable CIS Channel CAMAC slot 15
\$140			Enable/Disable CIS Channel CAMAC slot 16
\$144			Enable/Disable CIS Channel CAMAC slot 17
\$148			Enable/Disable CIS Channel CAMAC slot 18
\$14C			Enable/Disable CIS Channel CAMAC slot 19
\$150			Enable/Disable CIS Channel CAMAC slot 20
\$154			Enable/Disable CIS Channel CAMAC slot 21
\$158			Enable/Disable CIS Channel CAMAC slot 22
\$15C			Enable/Disable CIS Channel CAMAC slot 23
\$180	0-7		Write DAC Voltage low byte into setup latch
\$184	0-7		Write DAC Voltage high byte and set DAC

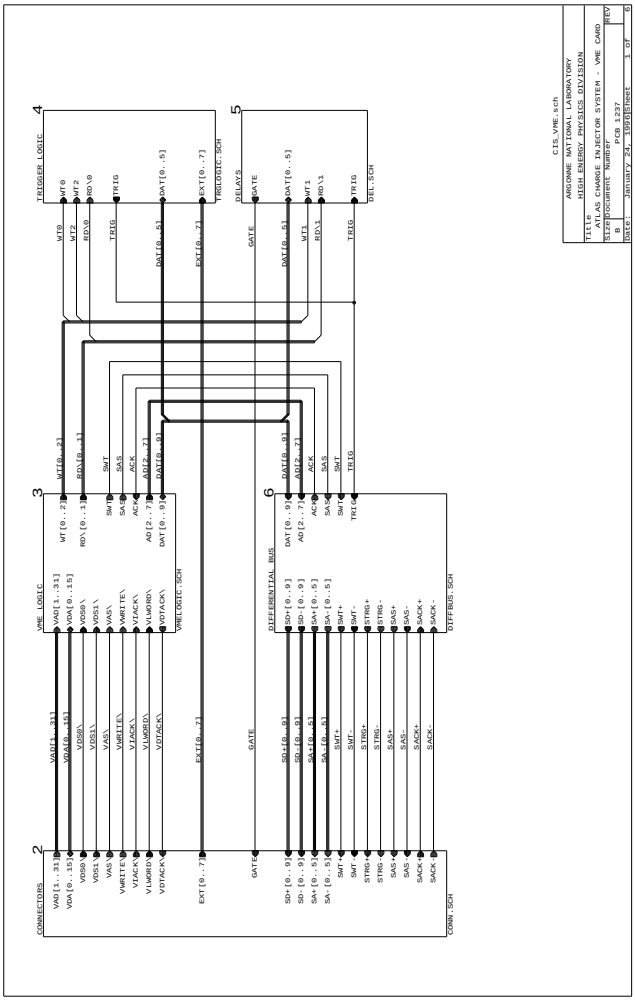

Figure 3: Root layout of VME board.

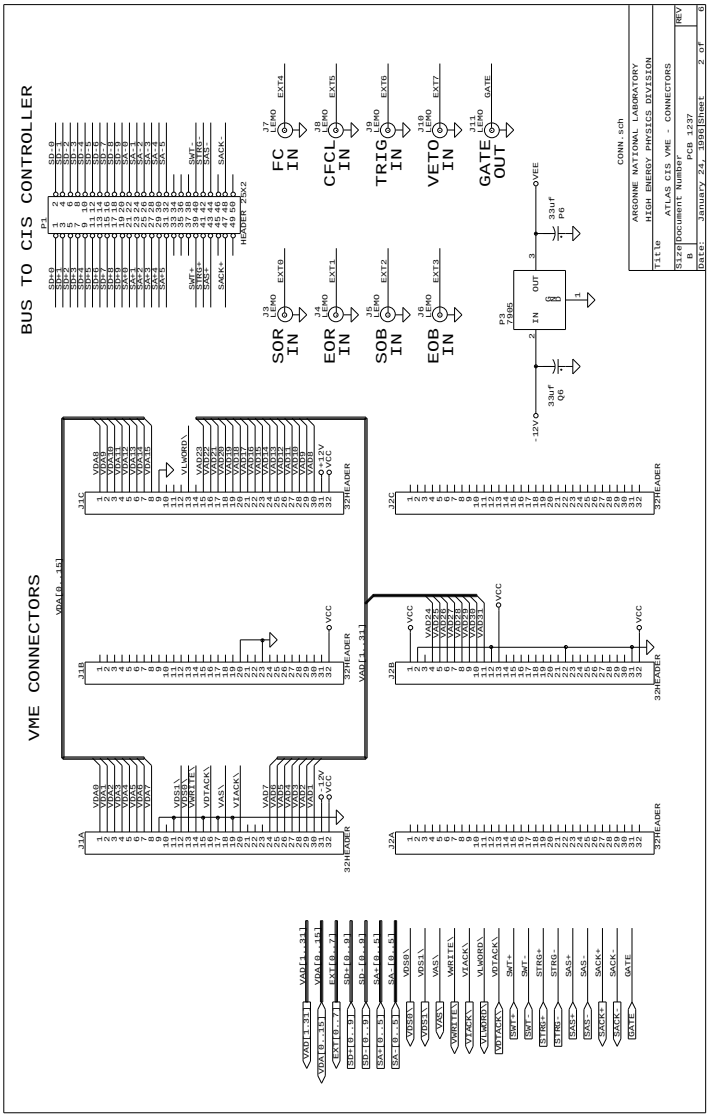

Figure 4: Connectors of VME board.

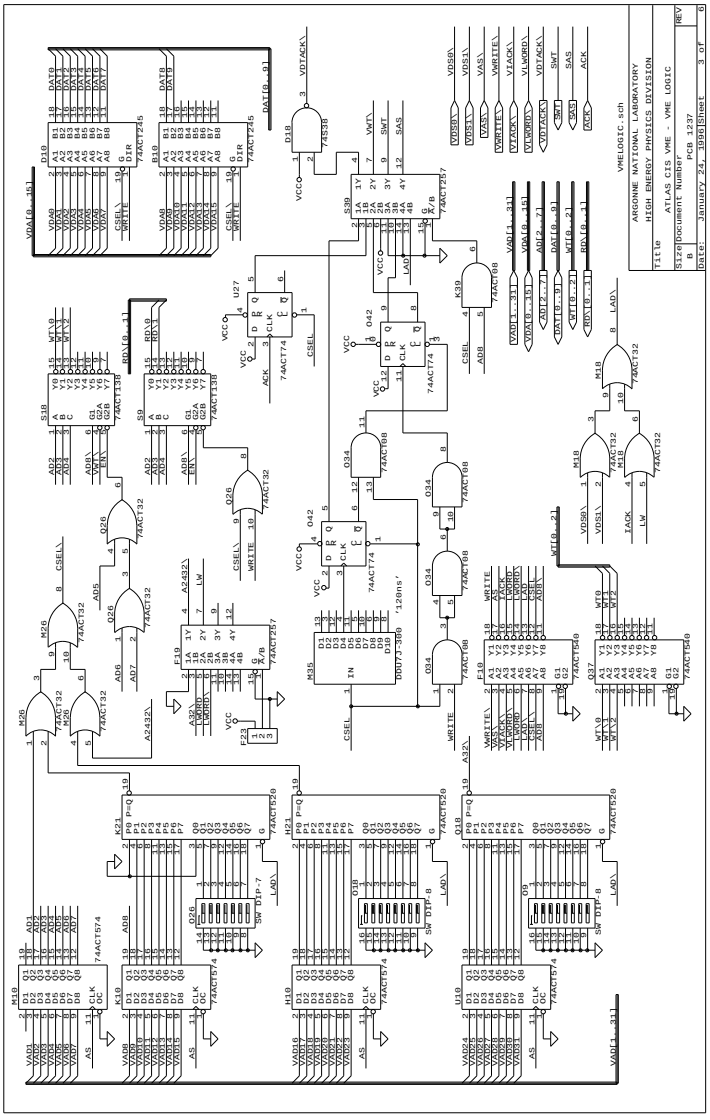

Figure 5: Schematic of VME decoding logic.

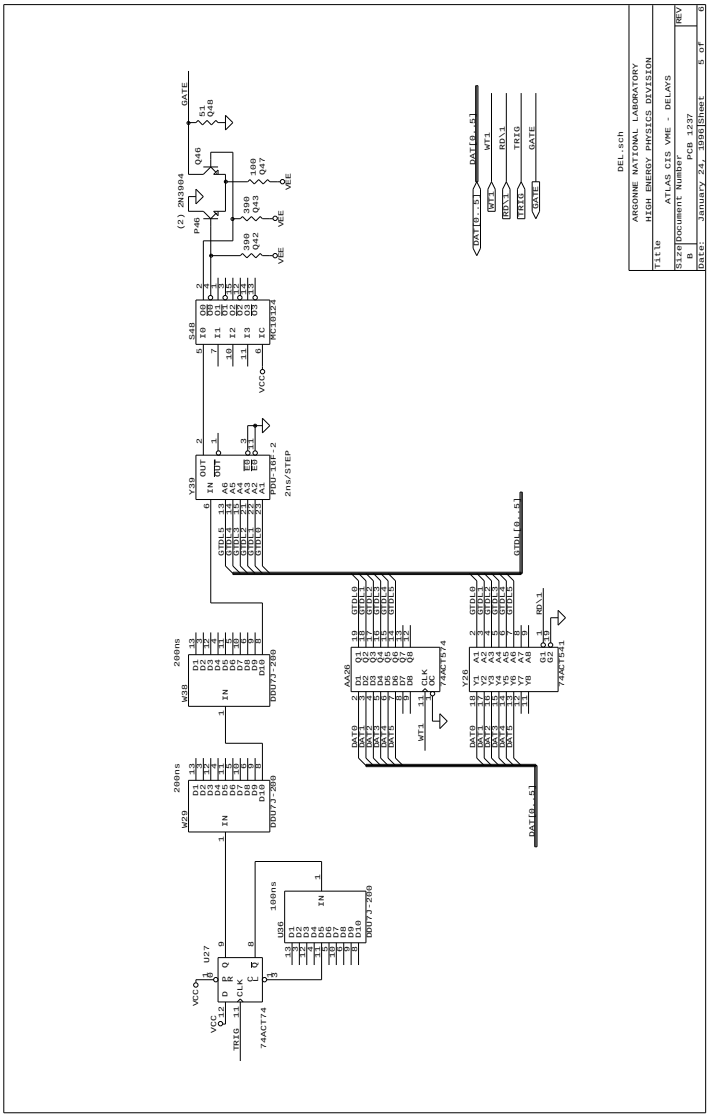

Figure 6: Schematic of Gate Delay in VME module.

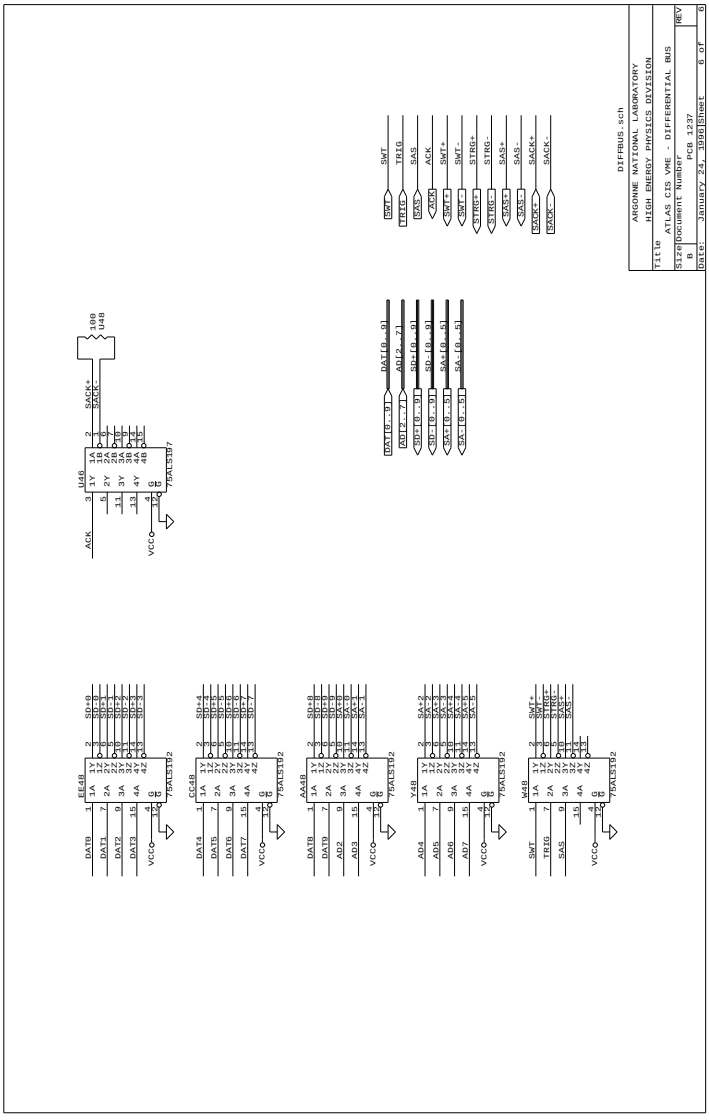

Figure 7: Schematic of VME-CIS bus signals.

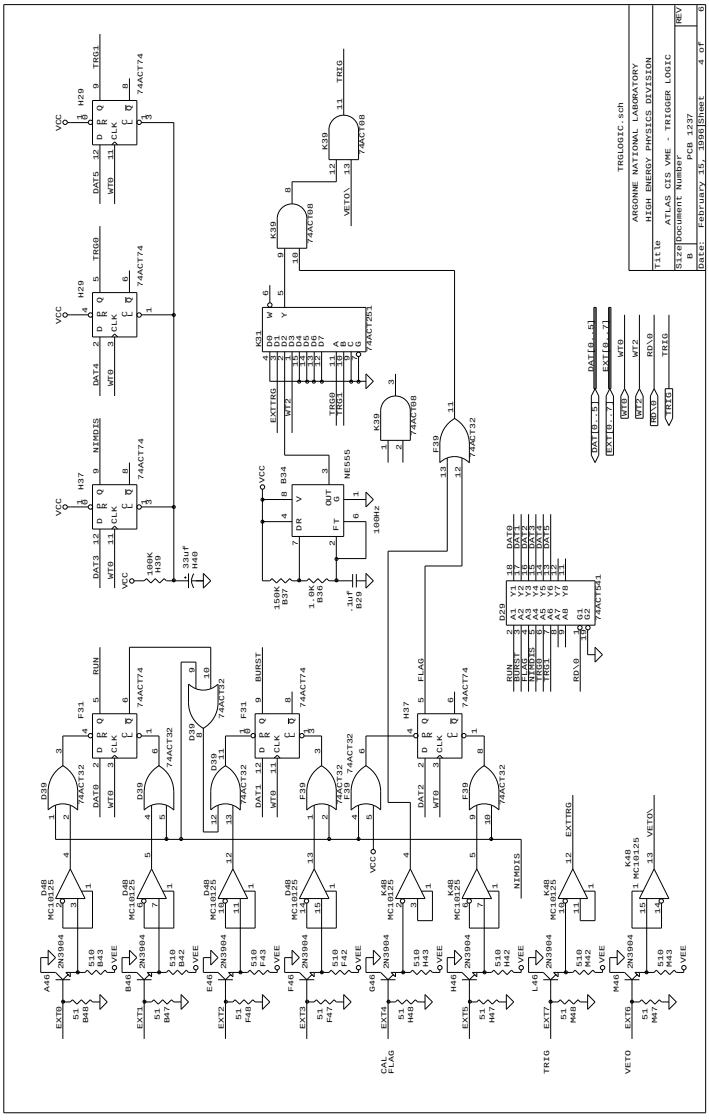

Figure 8: Schematic of triggering and enabling circuitry in VME module.

3.2 CIS Crate Controller

In Fig. 9 we show a functional block diagram of the CIS Crate Controller. The Crate Controller's function consists of at least the following:

- Receive and decode the commands from VME on the 50-conductor cable,
- Set the internal 16-bit DAC and supply the reference voltage at the V_{ref} connector,
- Write to the CIS modules to enable or disable particular channels,
- Send a trigger pulse on the S2 line to discharge the capacitors.

The Crate Controller contains the single 16-bit DAC for the entire crate and the DAC voltage is outputted the rear panel on a dedicated coax to minimize noise pickup. The reference voltage is then daisy-chained to all CIS Modules. There is a trimpot at the rear to adjust the zero of the DAC. This offset was adjusted using digitizations with LeCroy 2249W ADCs and the outputs of CIS Modules. Using an average for all 220 channels, the offset was set such that the pedestal measured with CIS channels disabled, and using a random pulser gating the ADCs, was the same as that measured with CIS channels enabled and $V_{ref} = 0$. The original difference was about 0.25pC. There is a full scale adjustment, and using an accurate voltmeter, this was set to 10.000 Volts.

The 23 VME addresses correspond to slots 1-23 in the CAMAC crate. The Crate Controller may write to a given slot a 10-bit word, enabling or disabling the respective CIS channel. Data is strobed to the CIS Modules with a write strobe (WT) on the S1 line. An empty slot addressed in CAMAC will not return an acknowledgement on the Q line, and the Controller will signal this to the VME which then will result in a VME bus error condition. Similarly, if the address of the DAC is not decoded properly - due to bad cable, power off, etc. - the Controller will signal an error and this too will result in a VME bus error. The generation of bus errors can be eliminated by wiring the write strobe directly to the ACK line.

Figures 10 through 13 show construction schematics of the CIS Crate Controller.

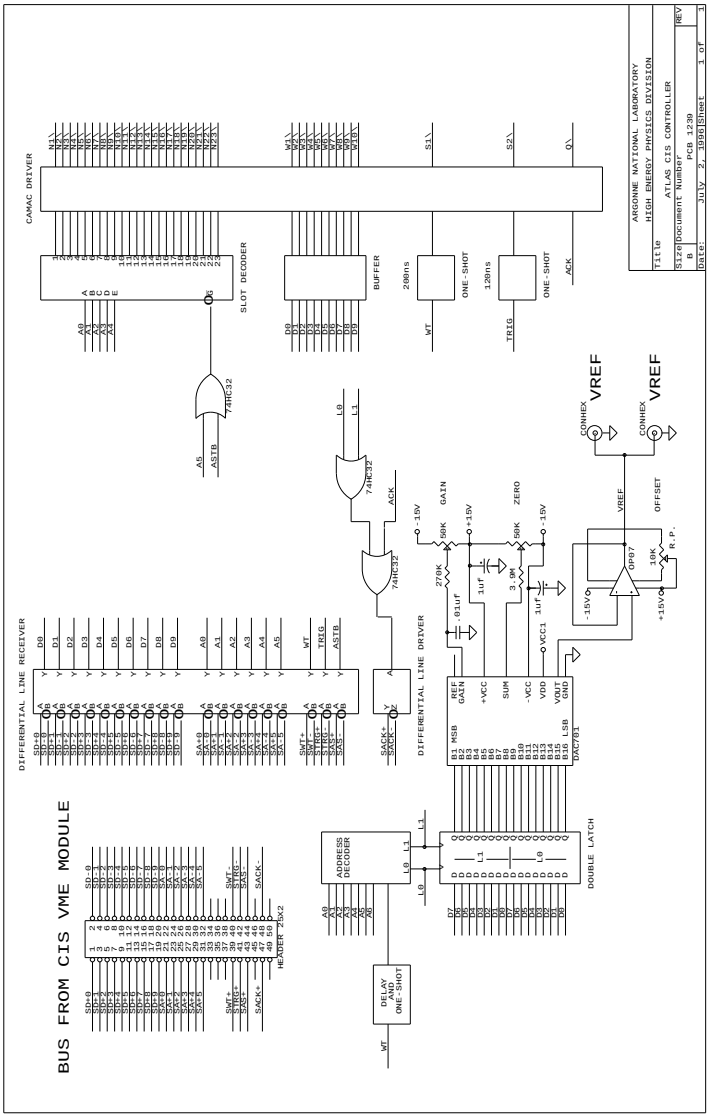

Figure 9: Functional diagram of CIS Crate Controller.

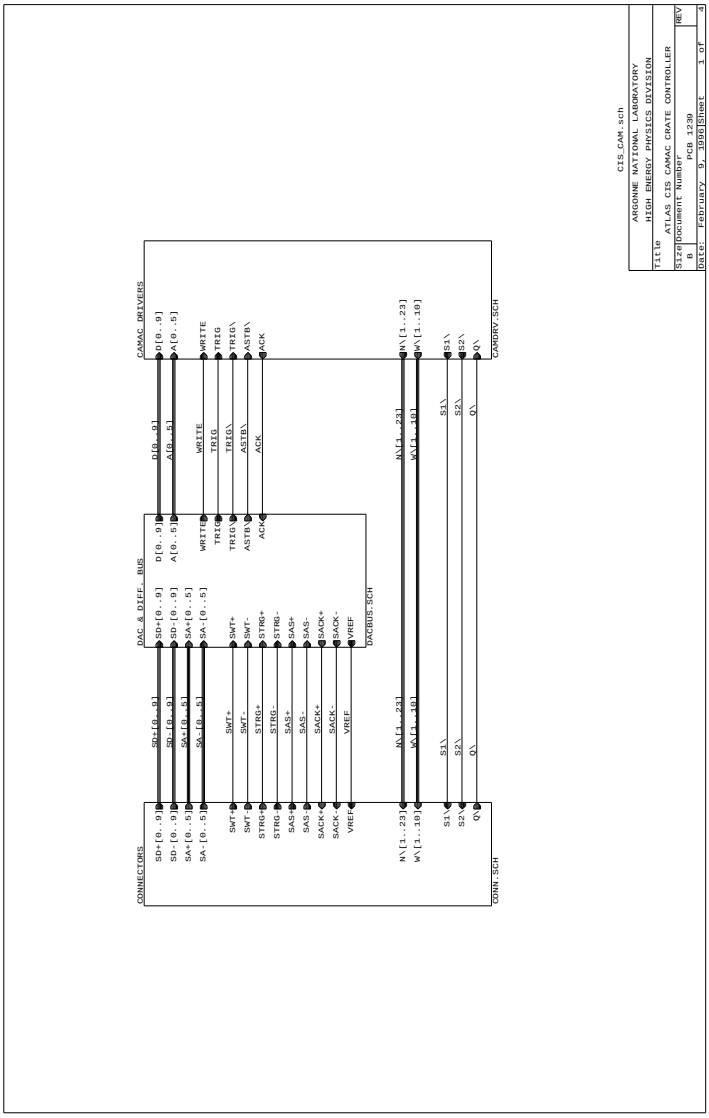

Figure 10: Root layout of CIS Crate Controller.

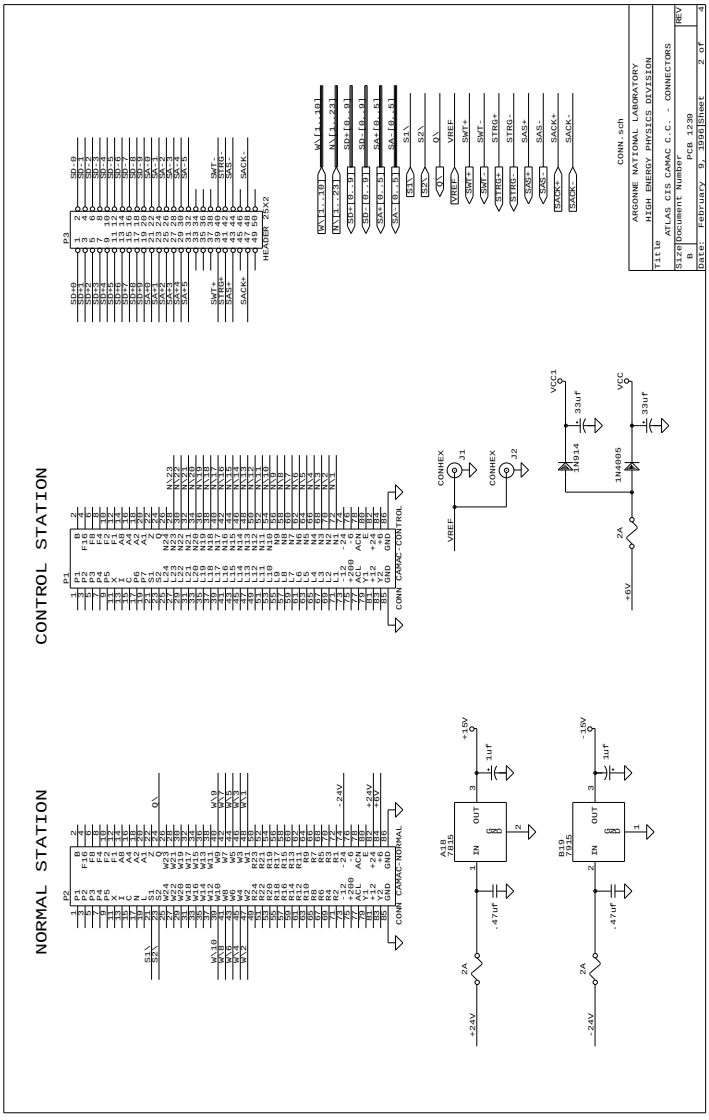

Figure 11: Front panel and back panel connectors of CIS Crate Controller.

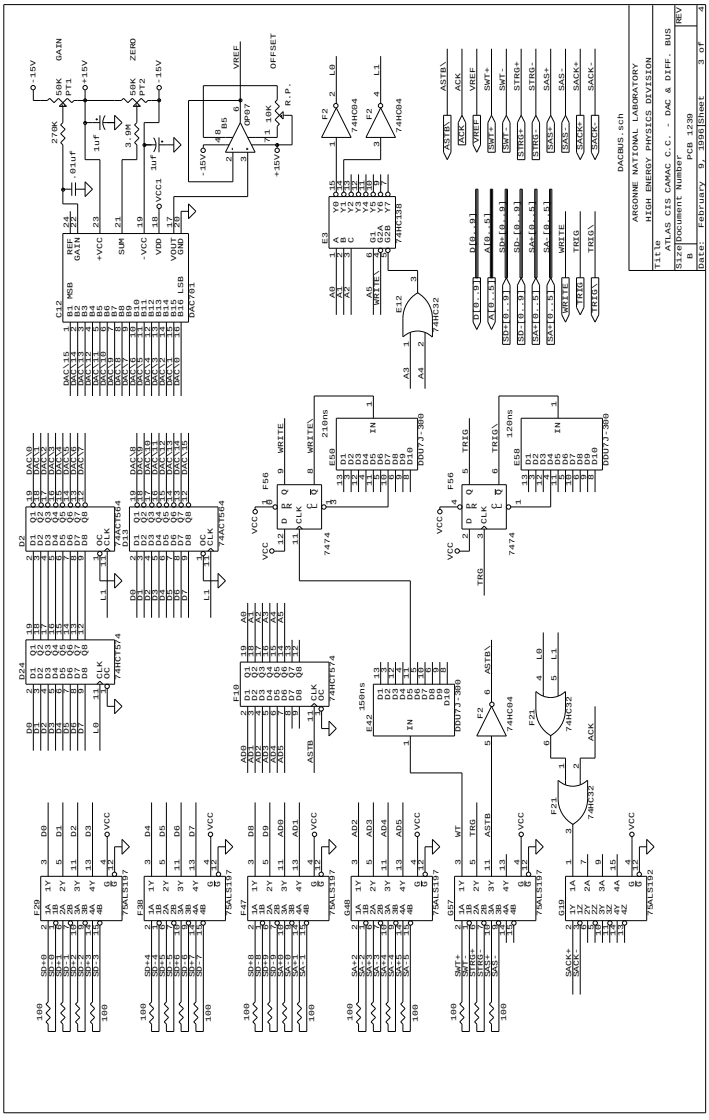

Figure 12: Schematic of the VME-CIS bus signals and the DAC logic.

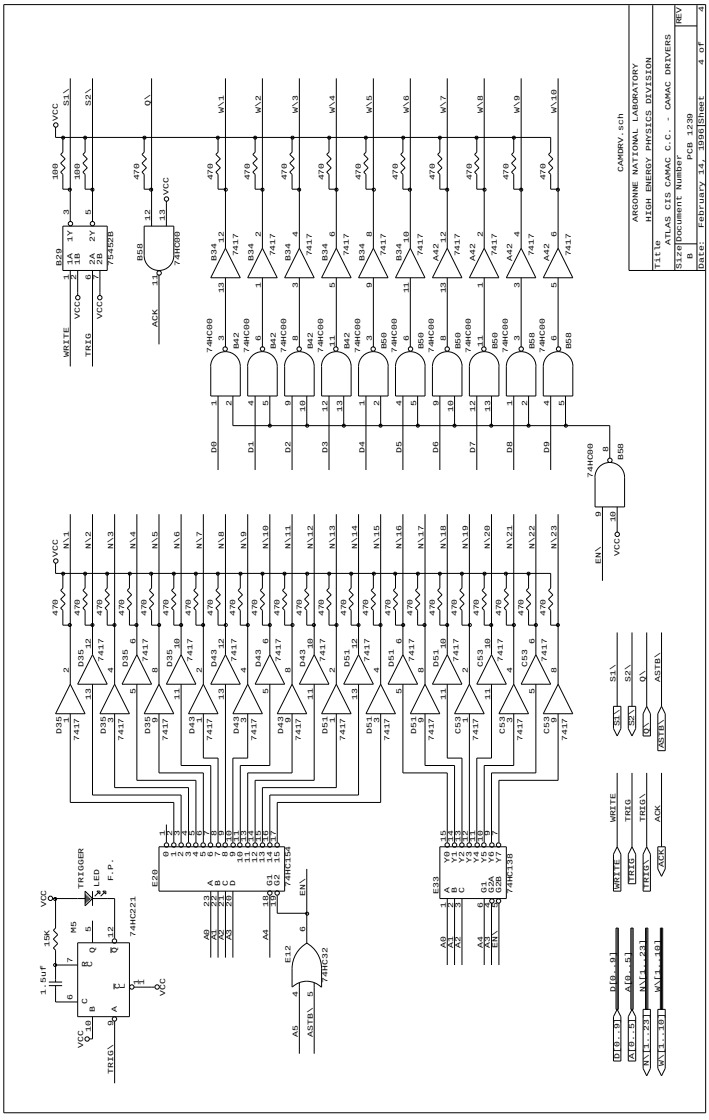

Figure 13: Schematic of the CIS Controller - CIS Module signal drivers.

3.3 CIS Module

In Fig. 14 we show a diagram of the CIS Module. The CIS Module allows the connection of the ADC input directly to either the phototube, disconnecting the charge injection circuit, or to the charge injection circuit, disconnecting the phototube. The change of states are accomplished with Form-A mercury-wetted relays. In the power off state the relays are set such that the CIS Module's inputs (from the phototubes) are connected to the CIS Module's outputs (to the ADCs). The charge injection circuit consists of a 100 pf capacitor charged to the V_{ref} voltage through a $150k\Omega$ resistor. Closing of a solid state switch on each channel quickly dumps the charge into the ADC output connector. The layout of the boards pays special attention to maintain a 50Ω impedance through the relays. The rise time of the charge pulse is $<$ 10 nsec.

Each CIS Module contains 10 channels and each channel is independently connected to its solid state switch. If the appropriate bit is set to connect the charge injection circuit to the ADC output connector, only then will the trigger pulse from the controller dump that channel's charge. If disconnected from the charge injection circuit, that channel will not be triggered, thus reducing cross talk between channels. A further reduction in crosstalk is made by delaying the falling edge of the triggering pulse outside the ADC gate. The pulse from S2 is therefore widened to $1\mu sec$ on each CIS Module. The cross talk is seen the strongest on neighboring channels at the level of about 0.05%. However even at some layout-specific channels, the cross talk can also get as high as 0.05%.

Figure 15 shows a layout of the parts for a CIS Module.

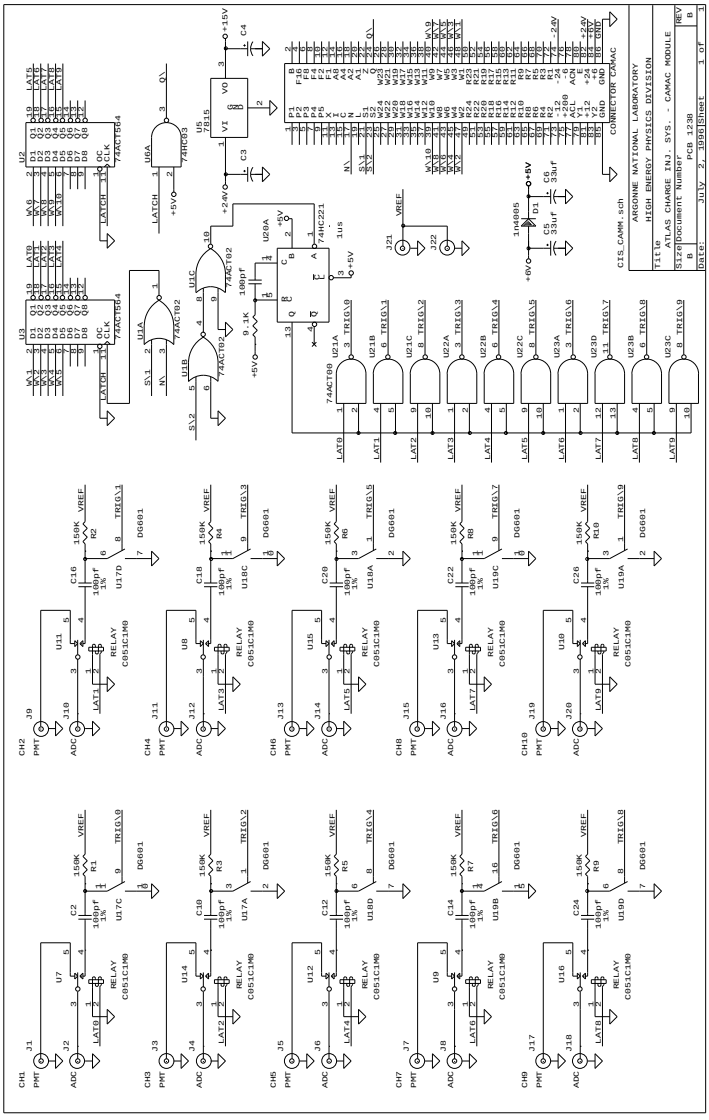

Figure 14: The CIS Module schematic.

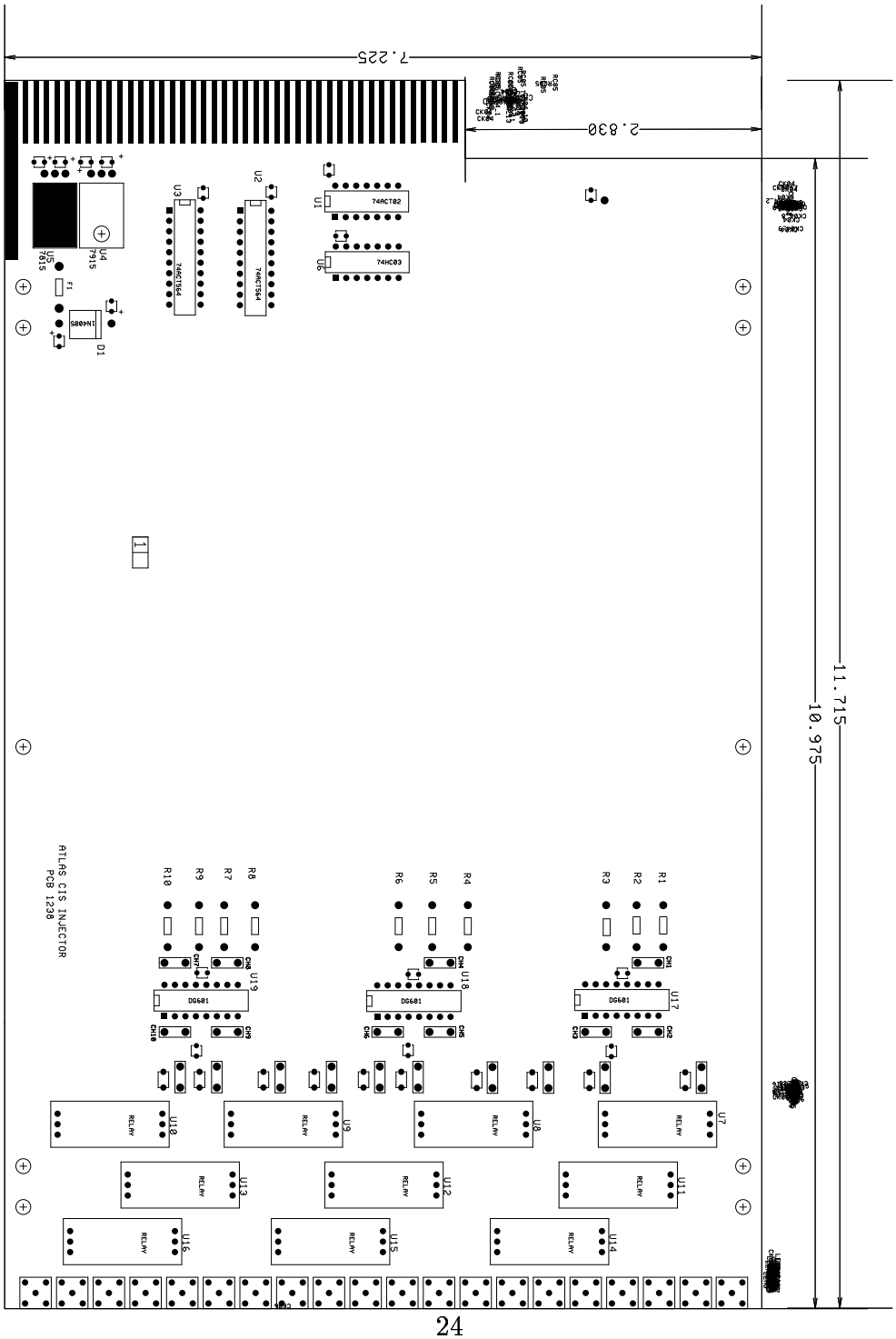

Figure 15: Component layout in the CIS Module.

4 CIS Operational Results

4.1 Bench Measurements

All CIS channels were measured using a Lecroy 2249W ADC. The outputs of 10 channels of a CIS Module were fed into the 2249W and the gate for the ADC was 150 nsec wide, triggered either by the CIS VME Module, or for pedestal measurements, a pulse generator. For each module three measurements were made: pedestal with no CIS channels enabled, DAC=0.0 Volts with each of the 10 channels individually enabled, and DAC=4.60 Volts also with each of the 10 channels individually enabled. To correct for channel-channel variation in the ADC, each of the 10 ADC channels had charge injected from one CIS channel and then all 10 channels were normalized to channel number 1. These corrections were $< 1\%$.

Pedestal and DAC=0 were compared, and for all but two CIS channels the DAC=0 signal was no more than 0.25 pC above pedestal. The two anomalies had $<$ 1pC above pedestal, and it was never learned what caused those effects.

With individual channels pulsed at a fixed DAC voltage, both uniformity and crosstalk was measured. As mentioned above in Sect. 3.3 crosstalk was never more than 0.05% from any given channel firing. In Fig. 16 we show the uniformity of the CIS channels, reflected as the capacitance of the charged capacitors. We calculate the corrected charge from the ADCs, and adjusted (offline) the value of V_{ref} to obtain a mean capacitance of 100 pf for all the 220 channels as shown in the figure. The tolerance is 1% as expected, but with an RMS of the distribution of 0.44%.

Using a Lecroy QVt we measured the loss associated with a long cable on the output of a CIS channel. With a charge injected into the cable of about 500 pC, we measure an 8.06% loss after the addition of 200 nsec of RG58 cable.

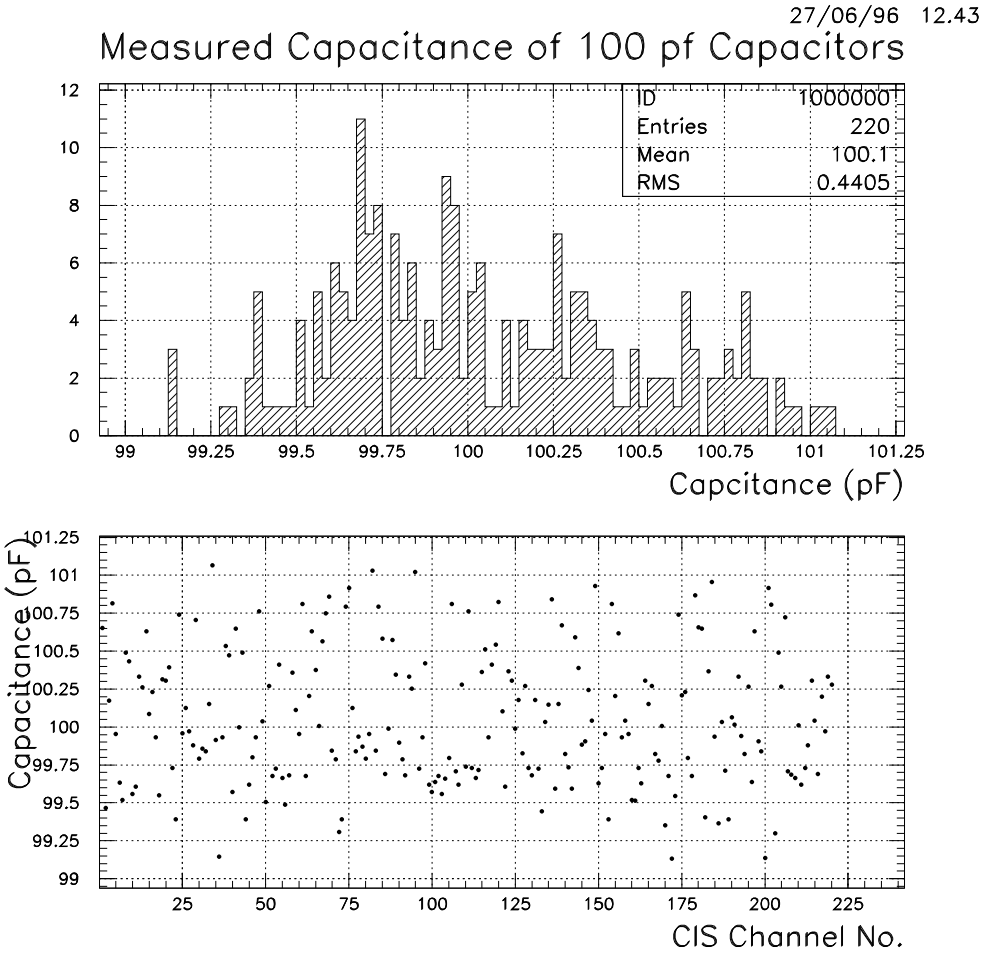

Figure 16: The resolved capacitance in each of the CIS Modules. The capacitance was derived from the pulse height measured in a Lecroy 2249W ADC and the applied voltage on the capacitors from the DAC. The tolerance on the capacitors was specified as 1%.

4.2 Software

4.2.1 DAQ

The online data acquisition system communicates with the Run Control to pass initial parameters to the CIS routine running on the RAID (rd34fe01) to read CAMAC and VME. The acquisition program can be found on the testbeam HP (hpea06) under the **tiledaq** account in directory **/users/tiledaq/development/sources/ticaldaq**. The main routines are called **usercal.c** and **tical_vme.c** and the variable declarations are in the respective include file. In the run control setup, the user specifies the initial DAC setting, DAC_0,in counts $(< 65,535)$, the number of DAC steps to be taken, N_{step}, a pattern in which channels are to be simultaneously pulsed and the number of pulses to record at each DAC for each pattern. A pattern is specified as a single number, and this number denotes the distance between channels simultaneously firing. For example, pattern=2 means every other channel is pulsed simultaneously. The calibration routine ranges through the DAC values according to the following algorithm:

$$DAC = \frac{DAC_0 + \frac{65535 - DAC_0}{N_{step}} \cdot (step - 1)}{8 * 0.60}$$

for $DAC \leq 65535/8$, and

$$DAC = 65535/8 + \frac{1 - \frac{1}{8}}{1 - 0.60} \cdot \left[DAC_0 + \frac{65535 - DAC_0}{N_{step}} \cdot (step - 1) \right]$$

for $DAC > 65535/8$.

Thus, a scan through the N_{step} points produces a bilinear DAC output in order to do a fine scan for the high gain channels, and a coarser scan for the low gain channels. The numbers 1/8 and 0.60 are parameters in the program.

A typical calibration run specifies 30 DAC steps, a pattern pulsing every 4th channel, an initial DAC setting of 6000, and 5 pulses/pattern/DAC setting.

4.2.2 Utilities

On the RAID there exists a utility program which allows one to setup the CIS system according to the parameters defined in Table 1. Under the **tilecal** account, in directory **/usr/people/tilecal/cis** are the files which make **cismain**, which allows one to simply enter the parameters. There is a script file , **set_slot**, which allows one to set enable or disable all channels, or to selectively enable a particular channel. The script uses the utility vme_loop. The base address of the CIS VME Module was set to DFF00000 for the April, 1996, run.

4.2.3 Monitor

The monitor program consists of a two step process. The first process is to run the CIS calibration from the Run Control and the second process is the analysis and fitting of the data with a PAW kumac.

The calibration monitor runs on the RAID (rd34fe01) and can be accessed on the testbeam HP (hpea06). The program can be found under the **tiledaq** account in directory **/users/tiledaq/development/sources/ticalib**. The main fortran routine is called **ticalib_cis.f** and the variable declarations are in the respective include file. **ticalib_cis** runs automatically after the Run Control starts the CIS calibration. For every DAC setting, the monitor program calculates the mean ADC and RMS for each amplified and nonamplified ADC channel. NTUPLE 1013 is written to **/hpea06/users/tilecal/ticalib/cis_nnnnn.hbook**, where nnnnn is the run number, and contains

1. the ADC module number
2. the ADC channel in the module
3. the step number
4. the number of events per step
5. the mean of the nonamplified value

6. the RMS of the nonamplified value
7. the mean of the amplified value
8. the RMS of the amplified value
9. the DAC setting in counts

The database **cabl.calo** is used for the relationship between ADC channels and pulsed calorimeter channels.

After a calibration run which takes a few minutes, the analysis of the NTUPLE is straightforward. In the **tilecal** account in directory **/users/tilecal/ticalib** **plot_cis.kumac** automatically reads in the NTUPLE, fits the amplified and non-amplified ADC values to the input charge with a quadratic:

$$Q = A_0 + A_1 \cdot ADC + A_2 \cdot ADC^2 \tag{1}$$

where $Q = DAC \cdot 1000/65535$ in pC. These coefficients are then stored in **/users/tilecal/ticalib/cis_nnnnn.coeff** for each ADC channel.

The final results of a CIS calibration are shown in Figs. 17 through 20. A sample of the fits for some ADC channels are shown in Fig. 21 for the high gain channels and Fig. 22 for the low gain channels. These results are not corrected for the 8.06% loss in the cable discussed in Section 4.1.

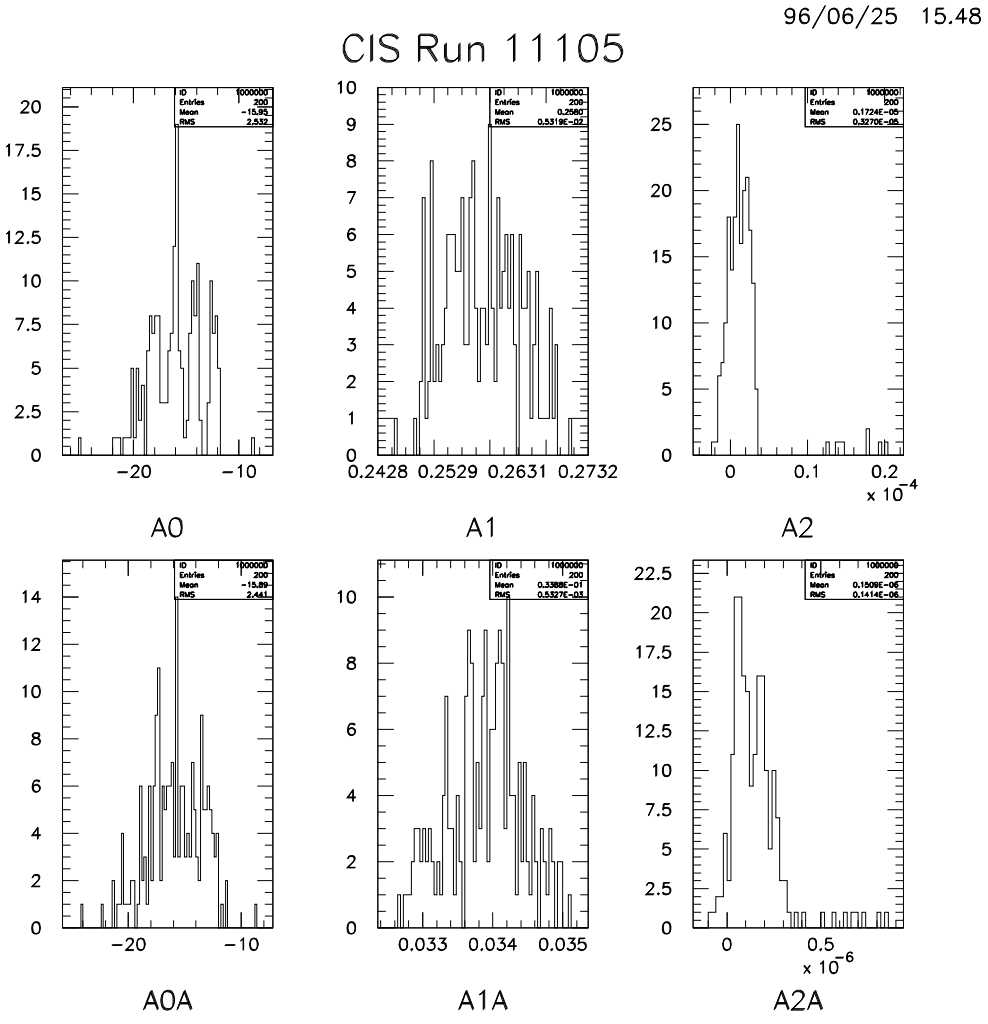

Figure 17: The distribution of the three coefficients of the fit for the non-amplified channels (A0,A1,A2) and the amplified channels (A0A,A1A,A2A).

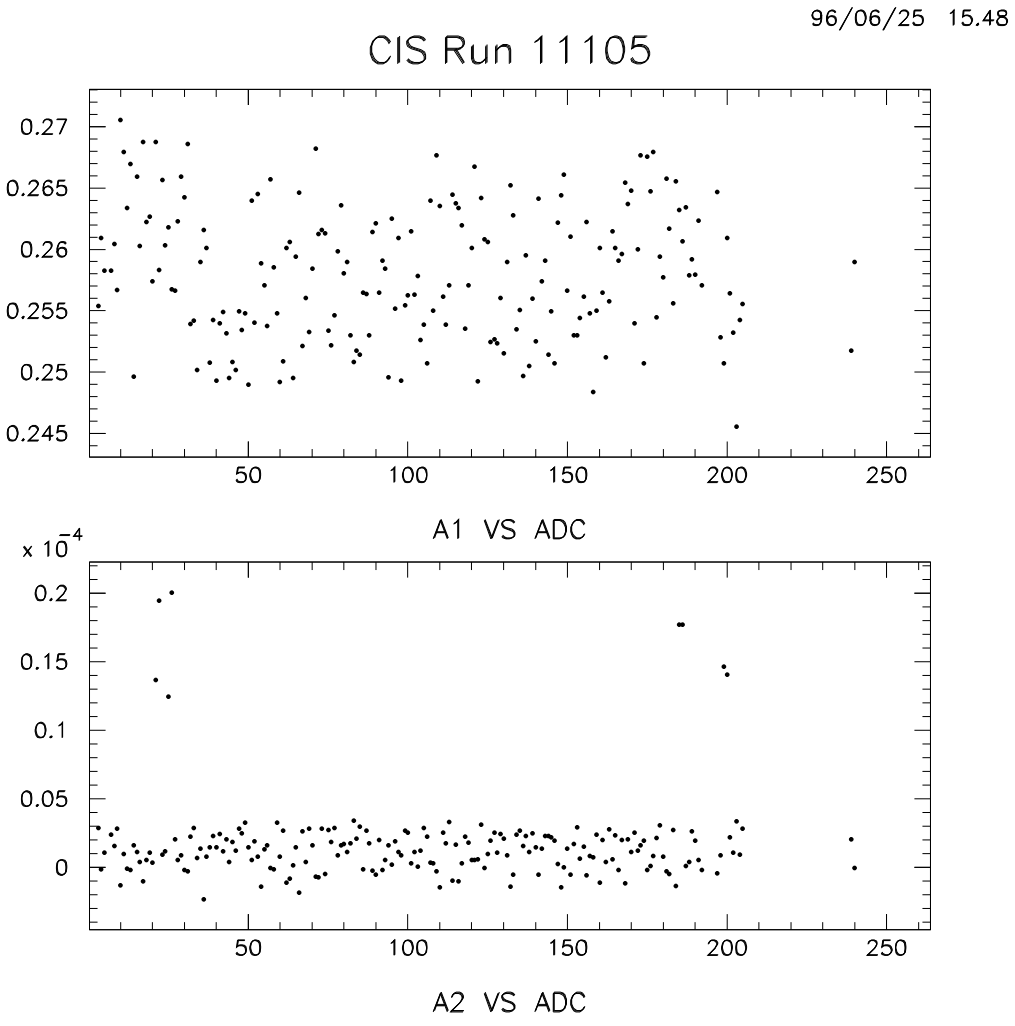

Figure 18: The linear and quadratic terms of the fit for the non-amplified channels *vs* each ADC channel number.

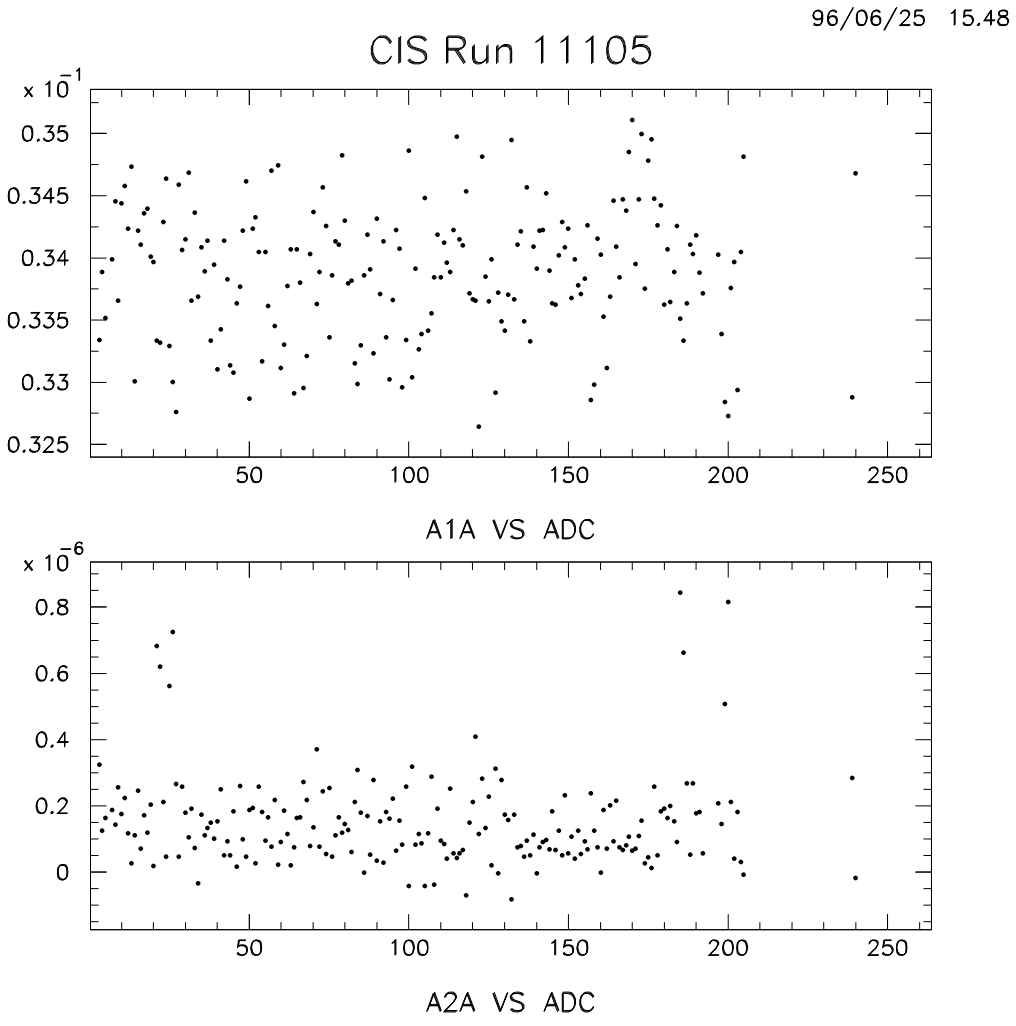

Figure 19: The linear and quadratic terms of the fit for the amplified channels *vs* each ADC channel number.

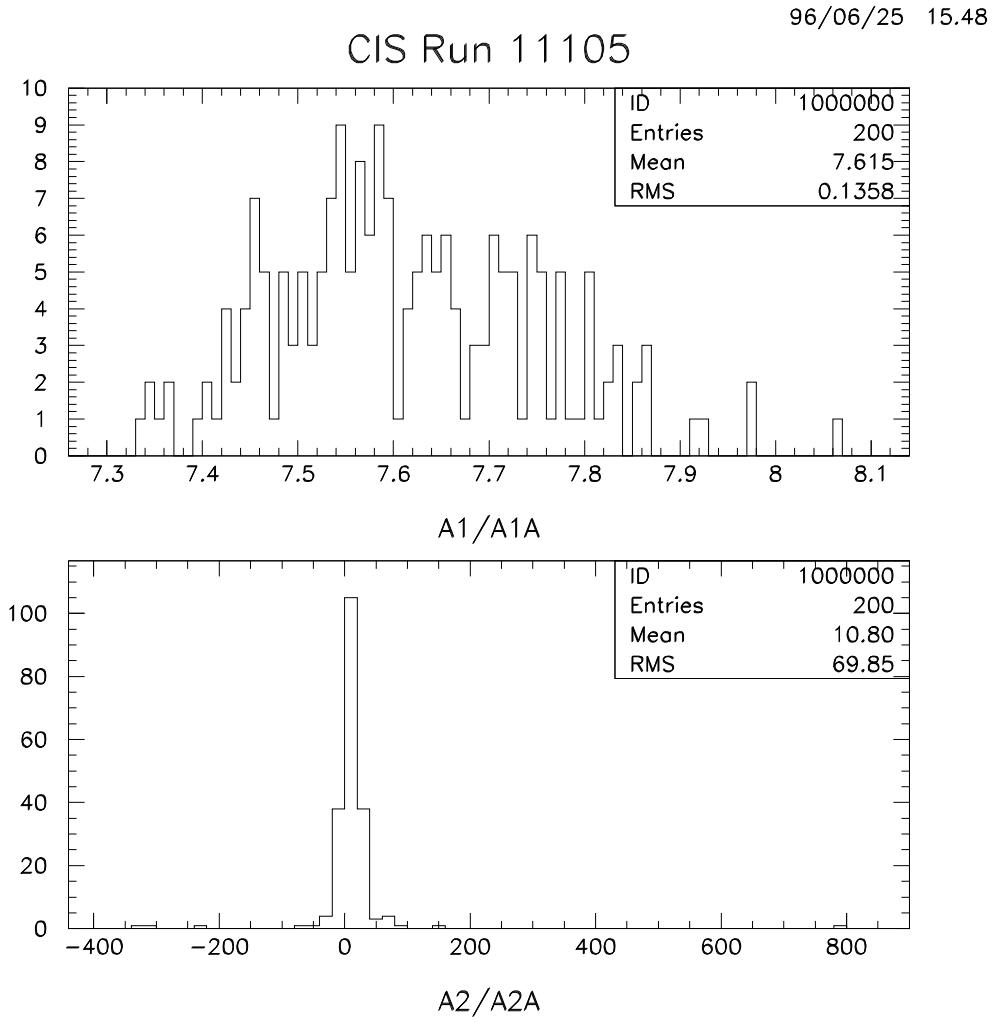

Figure 20: The ratio of non-amplified to amplified slopes (A1 and A1A) and the ratio nonamplified to amplified quadratic terms (A2 and A2A) for all the ADCs connected to the 1m modules.

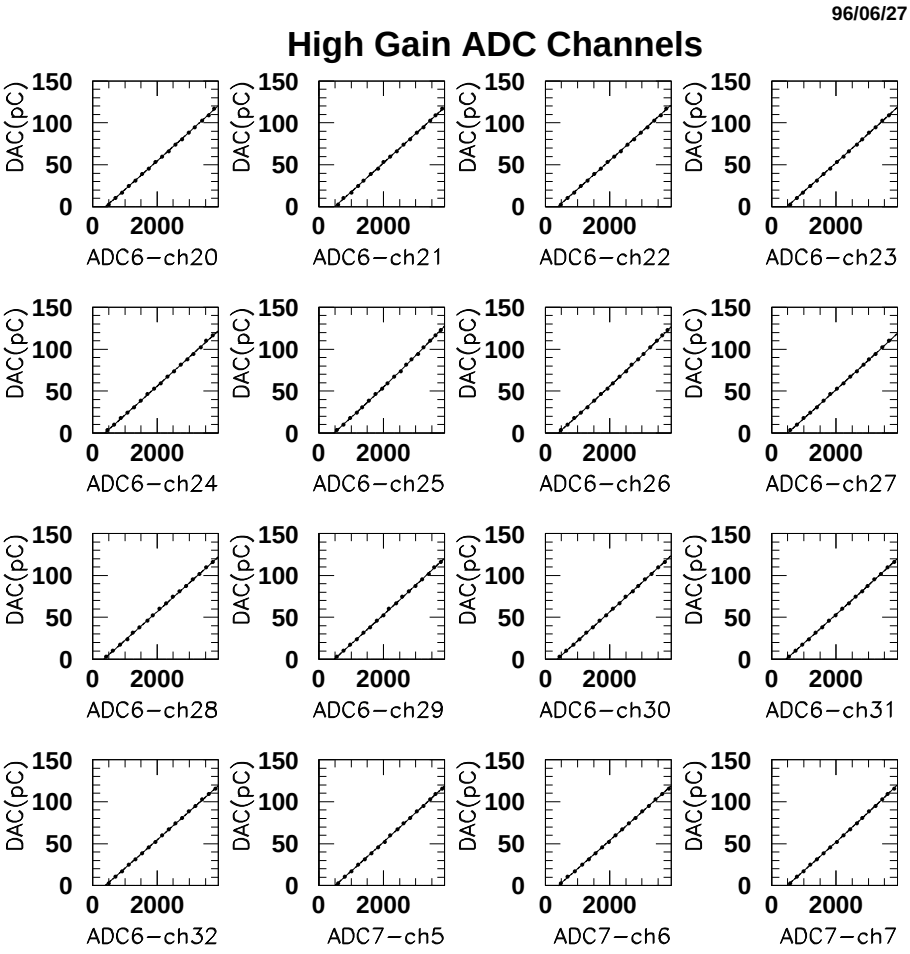

Figure 21: The injected charge *vs* the ADC value for a sampling of the high gain CAEN ADC channels. The fit is a quadratic to the data.

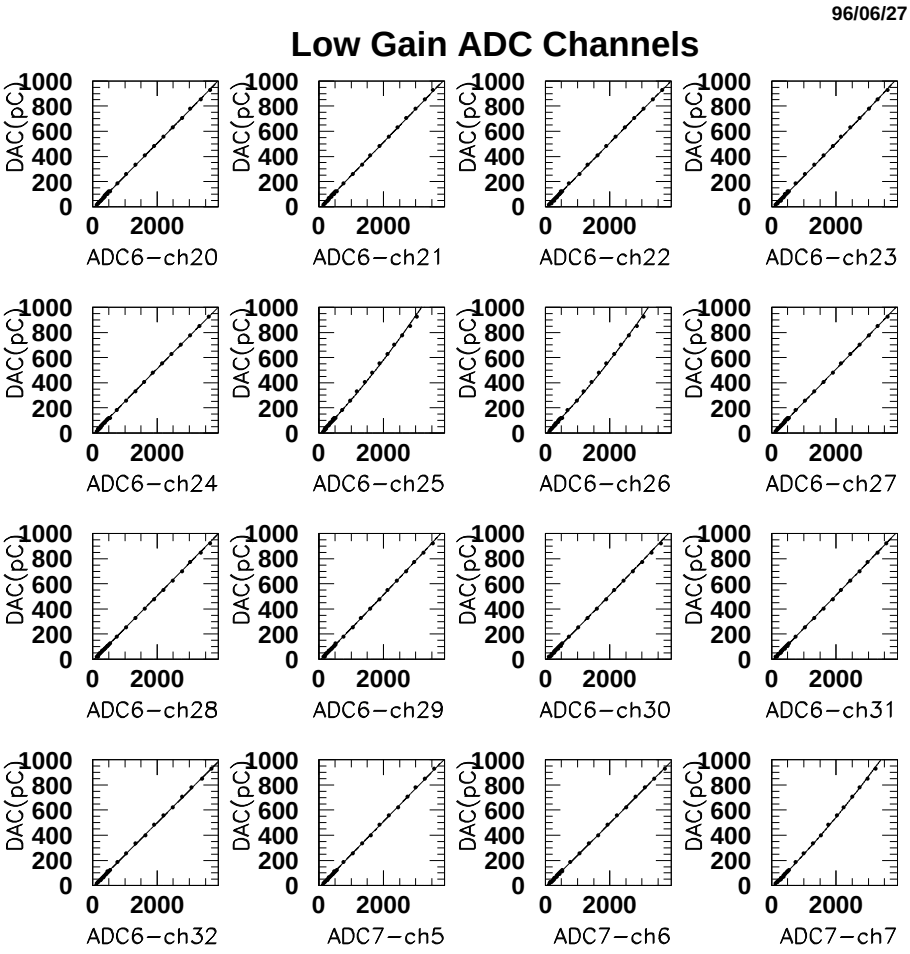

Figure 22: The injected charge *vs* the ADC value for a sampling of the low gain CAEN ADC channels. The fit is a quadratic to the data.