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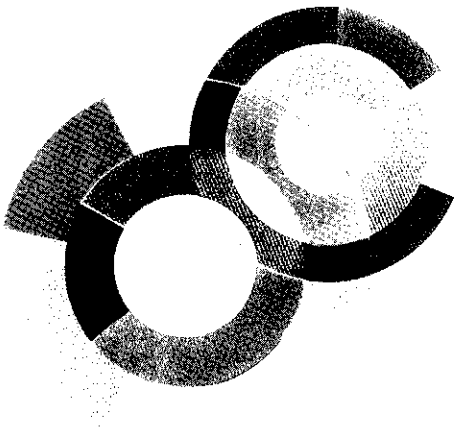

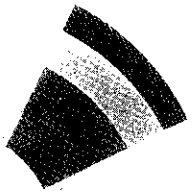

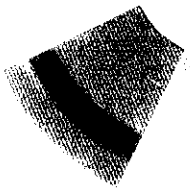

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# SFE16, A LOW NOISE FRONT-END INTEGRATED CIRCUIT DEDICATED TO THE READ-OUT OF LARGE MICROMEGAS DETECTORS

**E. Delagnes, P. Abbon, Y. Bedfer, J.C. Faivre, F. Kunne, A. Magnon, S. Platchkov, P. Rebourgeard, D. Thers**

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# SFE16, a Low Noise Front-End Integrated Circuit Dedicated to the Read-out of Large Micromegas Detectors.

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*Abstract*

A front-end BiCMOS ASIC was specially developed for the Micromegas detectors to be used in the Small Angle Tracker of the COMPASS experiment at CERN. Each of the 16 channels of this integrated circuit contains a low noise preamplifier with a 100 ns peaking time filter and a discriminator driving a low-level differential digital buffer. The design of the preamplifier and the choice of the shaping have been tuned to the detector signal shape in order to allow the operation of Micromegas even for very low multiplication gain values. Noise measurements show an equivalent noise charge of less than 1500 e- rms for a detector capacitance of 40pF. The measured performances of this ASIC associated or not with the detector are fully described in this paper.

## I. INTRODUCTION

The Small Angle Tracker (S.A.T.) of the CERN COMPASS experiment [1] will consist of at least twelve planes of 40cm*40cm 347 µm pitch Micromegas detectors [2] resulting in a total number of 14000 channels to be read. Although the central regions of the detector are inactivated, the particle flux can reach up to 100 kHz per detector strip. This high flux excludes the use of pre-existing low noise integrated circuits with a microsecond scale recovery time. Even if, at low flux, Micromegas can operate with a gain up to $10^5$, at higher flux its gain value is severely limited by the onset of discharges, phenomena common to all micro-pattern gaseous detector [4] generating deadtime and inefficiency. In the Compass experiment the detector gain will be set in the 1500-6000 range, to limit the probability of sparks to less than one in a 2s spill of the S.P.S. In order to reach a good overall detection efficiency using such modest detector gains, a low noise front-end electronics becomes then mandatory. This noise constraint together with the ballistic deficit due to the duration of the signal delivered by the detector are incompatible with the use of fast shaping preamplifier, used previously [3]. The SFE16 full custom ASIC has been developed to answer to this specific need.

## II. SYSTEM AND CHIP DESIGN

### A. Detector Read-out Architecture.

The read-out architecture of the whole COMPASS experiment has been standardized to reduce both the development effort and the cost for each sub-detector electronics. This read-out architecture shown on Fig. 1 is based on the use of the F1 chip [6] developed by Freiburg University for the specific COMPASS experiment needs. This chip includes an 8-channel multi-hit time to digital converter, level 1 buffers, a de-sparsification system, and the event formatting electronics.

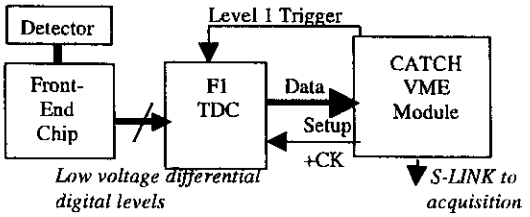


Fig. 1 : Simplified read-out architecture of the COMPASS SAT detector.

The front-end chips, realizing the Micromegas signal preamplification, shaping, and discrimination, will be implemented on daughter boards directly mounted on the detector. In order to limit multiple scattering, the rest of electronics will be located outside the detector acceptance. The Front-End Boards will be connected to the F1 board through 70cm long, differential cables.

### B. Detector Signal and choice of the shaping.

The signal induced on a Micromegas strip by the interaction of a minimum ionizing particle is the sum of a fast electron signal and of a slower ion signal. The duration (d) of the ion signal, which represents 80% of the total charge, depends on the gas and is typically of 105ns for Argon-isobutane mixture, which was the reference gas for the electronics design .

The total charge available on detector strips for a minimum ionizing particle can be calculated by :

$$Q = Qp * G \quad (1)$$

where Qp is the number of primary electrons created on the drift region and G is the mean gain of the multiplication region. Qp follows a Landau distribution which parameters depend on the gas used (for Argon based mixtures, the most probable value of Qp is 15 and its mean value is 32). The Landau distribution is slightly widened by the distribution of the gain. For this reason, the front end electronics dynamic range will have to treat incoming charges from few fC up to 100fC, for the highest detector gains expected.

As the detector does not deliver the charge instantaneously, its signal after integration and shaping will suffer from a ballistic deficit DBAL [5]. It is defined as the ratio of the peak amplitude of the shaped signal due to a charge delivered during a d duration, over that due to the same charge delivered

instantaneously. This effect is illustrated on Fig. 2, for a typical detector signal shaped by two filters with different time constants.

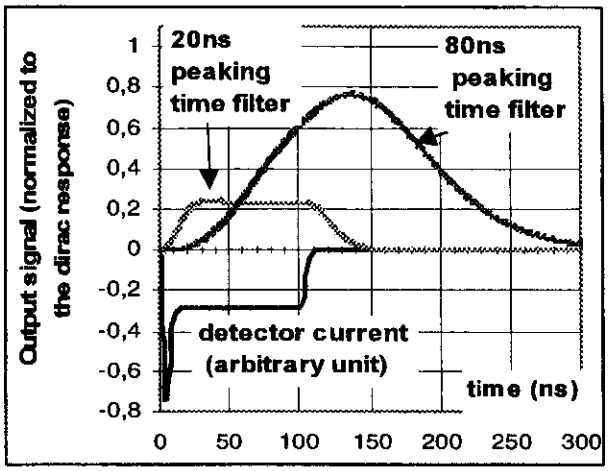


Fig. 2: Effect of the ballistic deficit for a typical detector signal.

The Equivalent Noise Charge (ENC) has been calculated for a detector capacitance Cd=40pF and an optimized PMOS input preamplifier [4] biased with a 2mA current (choice driven by power consumption constraints).

The Signal over Noise ratio (S/N) is then given by :

$$S/N = Qp * G * DBAL(tp,d) / ENC(tp,d) \qquad (2)$$

where tp is the peaking time of the 4th order semi-gaussian filter used for this study.

The occupancy time measured at 5% of the shaped signal (Tocc) has also been calculated as a function of both tp and d.

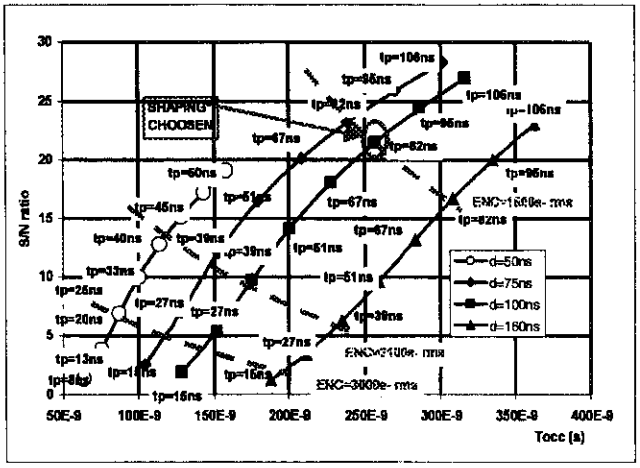


Fig. 3: S/N ratio vs Tocc for 4 different values of d. (G=3000, Qp=15 ).

S/N is plotted versus Tocc for different values of tp and d. on Fig. 3. This figure. shows that, assuming d=105ns, Qp=15 (Ar + isobutane) and G=3000, tp must be at least larger than 80 ns to reach a 20 S/N, necessary to achieve a 99% efficiency. For this value, Tocc is then equal to 250ns. It will results in an occupancy of in the order of 2.5%/strip at the highest expected flux of 100 kHz/strip. A tp value of 85ns will be taken as a basis for our design. The Fig. 3 also shows that for fastest detector signals obtained with other gas mixtures the S/N ratio will be higher.

Assuming a threshold set to 6000 electrons, corresponding to 4 sigmas of the rms noise, the frequency of noise hits per strip (Fn) has been simulated using the transient noise analysis available in the Eldo simulator [6] The value of 1kHz obtained for Fn remains small compared to the maximum counting rate due to particles.

## *C. Signal Treatment options.*

Previous tests and simulations have shown that with a 347µm pitch Micromegas [3], a binary read-out is sufficient to achieve the required spatial resolution of 100µm. To allow a correct particle tracking, and to limit the number of random events, the maximum width of the timing distribution has to be smaller than 100ns. As the detector jitter itself can reach a peak to peak value of 60ns, this requirement is obviously not compatible with the time walk of a leading edge discrimination for a signal shaped with a 85ns peaking time. The time walk due to the electronics can be drastically reduced by encoding both the leading and the trailing edges, as allowed by the F1 chip. In this Both Edge Discrimination treatment, the signal timing is calculated using a weighted linear combination of the two edges timing. The weights of the two edges may be extracted either from a signal typical shape, or from the calibration data.

Moreover, the duration between the two edges, called Time Over Threshold (TOT), represents a logarithmic compression of the amplitude and can be used as an analog information to improve the spatial resolution as shown in section III

## *D SFE16 Chip Description.*

The SFE16, fabricated in the AMS BiCMOS 0.8µm technology, has been designed to match these signal treatment options. It includes 16 front-end channels and some service blocs. To minimize the amount of material located in the detector acceptance, it is packaged in a 100 pins, 0.5mm pitch, TQFP plastic package. It uses +/- 2.5V power supply voltages.

As shown on Fig. 4, each channel consists of:

- an input protection

The chip inputs have to be protected against the detector discharges. The input protection is made of four diodes and does not use any serie resistor which would be an undesirable source of noise.

- a Charge Sensitive Preamplifier (C.S.A.)

Its open loop structure uses the classical operational transconductance amplifier structure with folded cascod. Its input PMOS transistor, biased with a 2mA current has been optimized for a 40pF detector capacitance. The feedback capacitance value is 0.5pF. The preamplifier input impedance

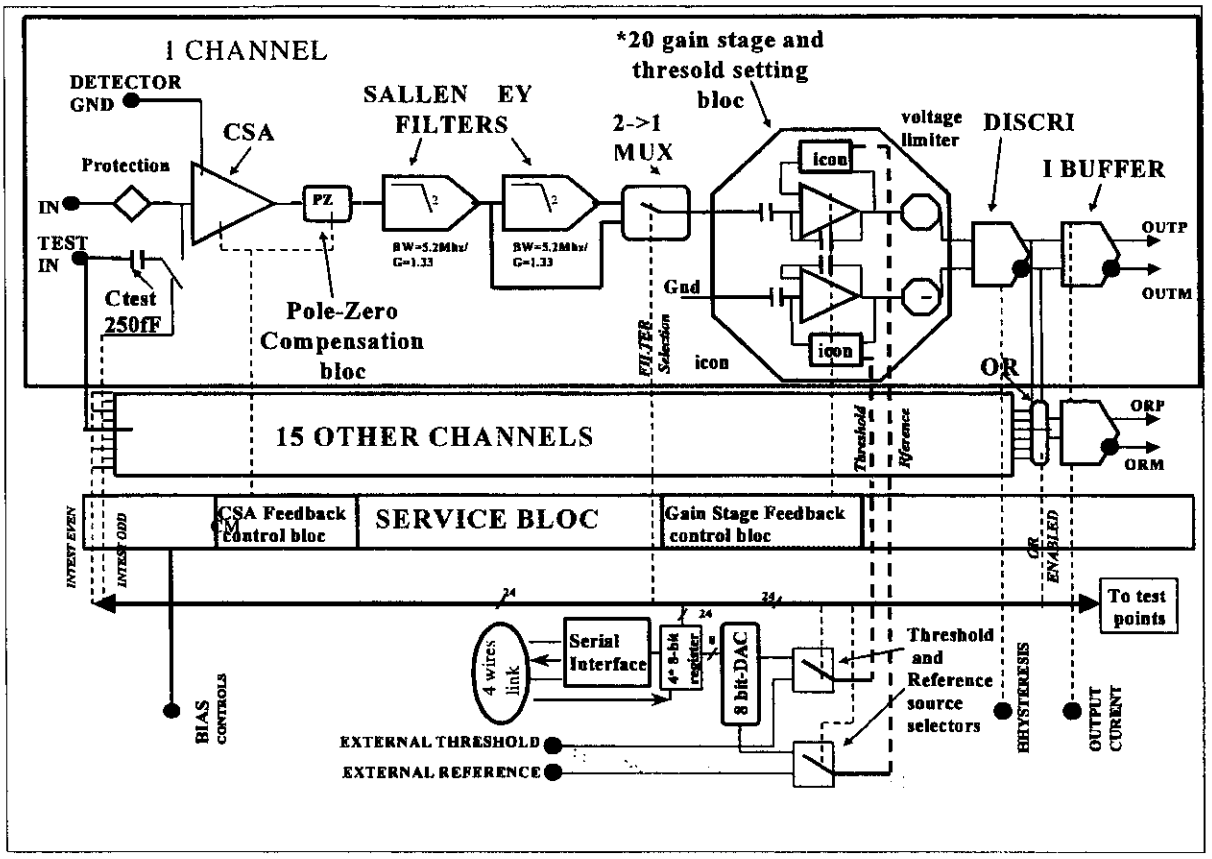


Fig. 4 : SFE16 architecture.

is 120 ohms so that its rise time is smaller than 15ns for a 40pF detector capacitance.

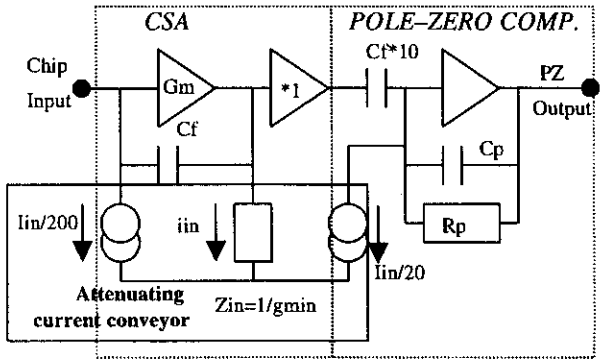


Fig. 5: CSA and Pole zero cancellation stages.

The CSA DC feedback, shown on Fig. 5, is realized using an attenuating current conveyor [5] simulating a high value resistor. The 2µs time constant due to this low frequency feedback is small enough to avoid any saturation effect of the CSA output even for a 400kHz flux. The CSA is buffered by a NPN emitter follower.

- A pole-zero compensation stage.

This stage cancels the low frequency pole introduced by the CSA DC feedback by adding a zero at the same frequency, and replaces it by a 21ns pole set by Rp and Cp. The cancellation is achieved using the second output of the current conveyor. The non linearities of the input impedance of the current conveyor NMOS input device are thus compensated.

- a shaper:

It consists of two cascaded second order, complex poles, Sallen-Key integrating filters. These filters have been prefered to passive one for their shortest occupancy time. These filters are built around bipolar input operational amplifiers, using polysilicon resistors.

The output of the filters are multiplexed towards the rest of the chain. When the first output is selected, the shaped signal peaking time is 65ns whereas it is 85ns when the second filter output is selected. In both cases, the shaped signals present a 1% undershoot.

- a high gain stage.

This stage, drawn in Fig. 6, is built around a high gain-bandwidth BiCMOS operational amplifier. Its NPN transitor input differential pair is buffered by NMOS source followers, to avoid any DC input current.

This bloc realizes 3 functions:

-It amplifies the shaped signal by a factor of 20 defined by the ratio C2/C1. This extra gain allows to limit the constraints on the discriminator and threshold voltage setting system offsets.

- it achieves an ac-coupling, with a long time constant, to the discriminator input. The R0 polysilicon

resistor in serie with a NPN input attenuating current conveyor (A= 1/1800) defines the low-frequency feedback path. The ac coupling time constant is defined by :

$$\tau_{AC} = R0/A * C2 = 30\ \mu s \quad (3)$$

The non linear behavior of the current conveyor limits the mean baseline shift at high counting rate.

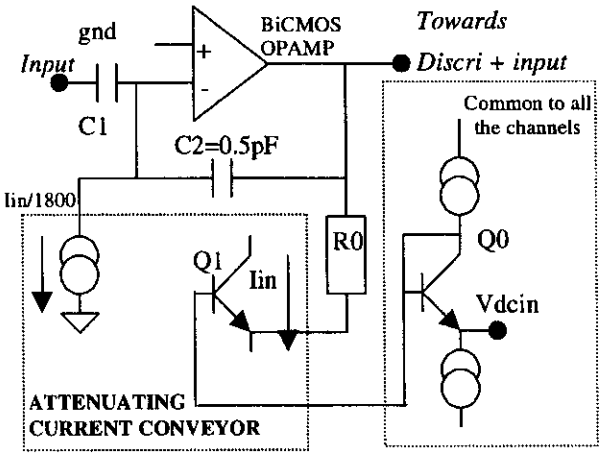


Fig. 6: 20 Gain stage

The DC output voltage of this bloc is defined by

$$Vdcout = Vdcin - VBE(Q1) + VBE(Q0) \quad (4)$$

Q0 is a reference transistor common to all the 16 channels. As the current density in the Q0 and Q1 emitters are identical, their two base-emitter voltages (VBE) are equal, and their process or temperature variations are compensated . The Vdcin input of the 16 gain blocs are connected to a common line Vrefth.

- it clamps the output signal to a voltage smaller than 2V. This is needed to avoid the breakdown of the BE junction of the discriminator input transistors. The saturation behavior of this stage has been carefully studied to allow an accurate timing of falling edge even on saturated signals.

The transfer function at the output of this stage is 110mV/fC.

- a fast discriminator driving a differential current output buffer.

The discriminator is a very simple low-offset, NPN input, fast comparator with programmable hysteresis. This hysteresis can be adjusted by an external resistor from 0 to 20mV.

The output buffer consists in an open collector NPN differential pair, which bias current can be externally adjusted in the 200µA-4mA range, depending on the output signal transmission length. This current is converted externally into voltage by resistors connected to the common mode voltage line. By using 50 ohm resistors and a 2mA current, it allows a 100 mV output swing compatible with the F1 chip input.

- a threshold setting system.

The negative input of the discriminator is connected to a bloc similar to the 20-Gain stage, but with the input connected to the ground. This differential structure improves the power supply rejection of the chain and allows to compensate systematic offsets due to the current conveyor blocs. The Vdcin input of this bloc is connected to a Vth voltage common to the 16 channels. The effective discriminator threshold is then defined differentially by :

$$Vtheff = Vth - Vrefth \quad (6)$$

Both Vth and Vrefth can be set either externally or by an internal DAC.

- A 250 fF test capacitance. The test capacitances can be enabled by group of eight (even or odd channel number).

The SFE16 chip also includes other blocs such as :

- an 8-bit DAC allowing to set the threshold.

This rudimentary DAC, based on minimum sized weighted NMOS current mirrors is temperature compensated. It supplies a voltage in the 0-587mV range for vth with a 2.3mV LSB. It also provides a fix voltage of 37mV for vrefth .Thus the internal DAC allows an effective threshold setting in the range -0.3fC to 4.5 fC.

- a logical OR of the 16 digital outputs which can be used for monitoring purpose. This functionality can be disabled.

- programmable test points on the 16$^{th}$ channel of the chip allowing to probe the signal through an internal buffer or to inject a signal in different points of the analog chain.

- a serial link.

This 4 wires serial link is compatible with the AD8842 protocol used by the F1 chip. Four 8-bit registers are charged inside the chip via this link. One is used to set the threshold level, the three others to conFig. the test points, the filter selection, the enabling of the injection capacitances and the enabling of the OR output.

## III. MEASURED PERFORMANCES

### *A. Electrical Tests*

The SFE16 chip area is 20mm$^2$ for 13000 transistors used. This chip has been fabricated in a MPW run, in which the polysilicon sheet resistor was 5% out of specification and 35% larger than its typical value. All the time constants, defined by an RC product, are then longer than expected. Anyway, the SFE16 chip is fully working, and has been characterized mainly using the output of the shortest filter.

The power consumption is 17mW/channel when a 2mA current is set in the output buffers. It is dominated by the CSA and the digital output current buffers. The measured performances of the on-chip DAC are summarized in the Table1.

Table 1: On-Chip DAC performances.

| | | |
|---|---|---|
| DAC LSB | 2.3 | mV |
| DAC LSB variation (20°C-60°C range) | <1 | % |
| DAC differential non linearity | +/- 0.7 | LSB |
| DAC integral non linearity (codes 0 to 127) | <1 | % |
| DAC integral non linearity (all codes) (fit forced to the origin) | <3 | % |

Even if it is not perfect, especially concerning the differential linearity performances, due to a non optimized layout, the DAC presents the expected characteristics and is accurate enough to be used to characterize the rest of the chip.

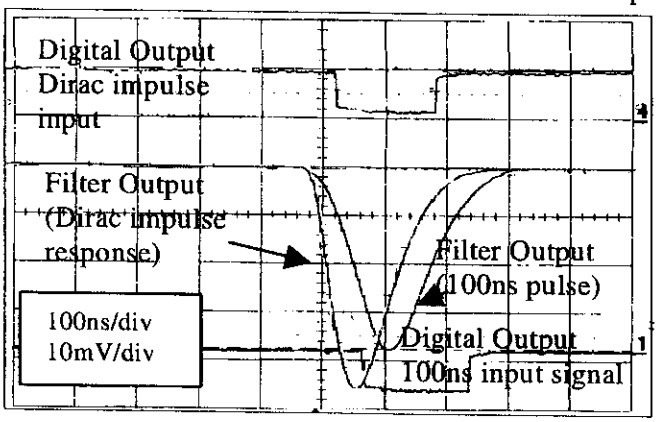


Fig 7: Response of the SFE16 chip (filter test output) to 4fC injected instantaneously or within 100ns.

Fig. 7 shows the response of the SFE16 chip for two different input pulses of different durations. As expected, the ballistic deficit is 19% for a 100ns long input.

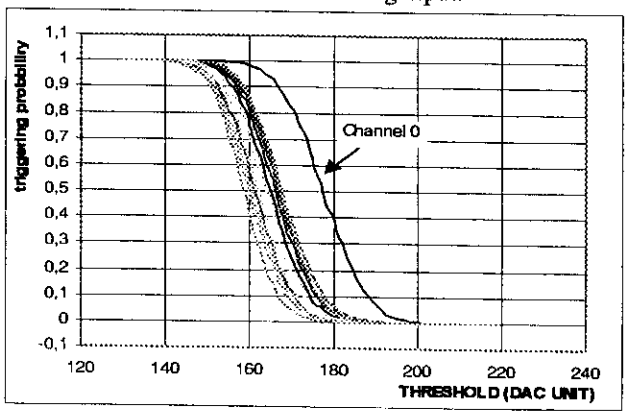


Fig 8 : Probability of triggering vs threshold value for a 3fC input (16 channels of a typical chip)

The chip characteristics, given in the Table 2, have been extracted using two classical methods :

- by an erfc function fit of the S-curve shown in Fig. 8 for different injected charges. It allows to extract both the gain and the noise parameters.
- by a gaussian fit to the noise frequency versus the threshold curve (Fig 9). It allows to extract both the signal baseline value and the noise value [5].

The chip transfer function is the expected one. It is uniform for all channels of a chip within +/-1 % excepted for the first channel which presents a gain 5% higher for a reason not yet explained.

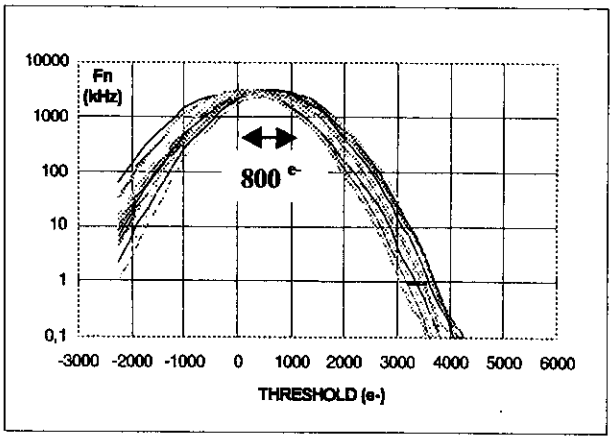


Fig 9 : Frequency of Noise hits versus threshold value (16 channels of a typical chip). The input capacitance is 32pF.

The total channel-to-channel baseline dispersion in a chip at the discriminator inputs level is 14mV peak-to-peak. It is principally due to offsets on the blocs achieving the low frequency feedback in the 20-gain stages. Together with the gain dispersion, it will be the main cause of a 1000 e- spread for a threshold set to the specified value of 6000 e-.

The Equivalent Noise Charge (ENC) versus the input capacitance (Cin) characteristics plotted in Fig 10 are 20% higher than the simulated one. Anyway for a Cin of 50pf, corresponding to the sum of an estimated detector capacitance of 40pF and a stray capacitance of 10pF, the ENC is smaller than the 1500 e- used as an hypothesis for the design.

Measurements confirm that the noise frequency (Fn) depends only on the ratio (TH/N) of the effective threshold over the rms value of the noise. For TH/N larger than 4, as expected, Fn is smaller than the required 1kHz.

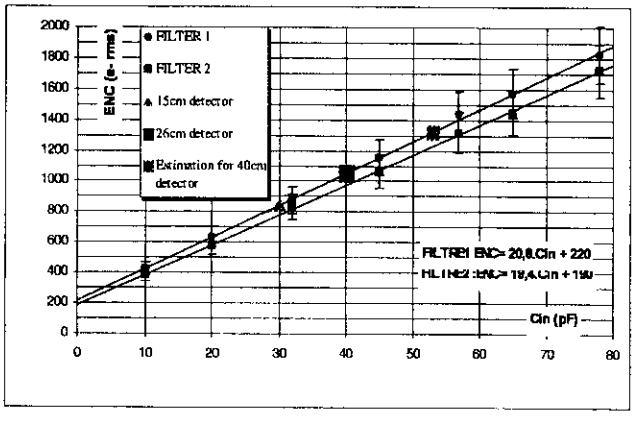


Fig. 10: ENC vs input capacitance (Cin).

As the chip does not include any true baseline restoration system, its high counting rate behavior has been checked. For a 100kHz rate of 16 fC charges injected (twice the mean charge expected), the mean baseline is only decreased by 200 e-. This

value is negligible compared to an expected threshold value of 6000 e-.

Table 2: Summary of the measured SFE16 chip performances .

| ***Signal parameters*** | |
|---|---|
| Transfer function at discri input (dirac) | 110mV/fC |
| DAC value conversion factor | 130 e- |
| Dynamic range | 0-80fC |
| Filter peaking time (filter1/filter2) | 85ns / 100ns |
| Transfer function dispersion in a chip | 5% |
| Transfer function T° coefficient | -0.1%/°C |
| On-Chip channel-to-channel cross-talk | <0.4% |
| Integral non linearity (0-4fC range) | <1% |
| | |
| ***Noise parameters*** | |
| ENC versus input capacitor Cin law (filter 1) | 220 e- +21 e-/pF rms |
| ENC versus input capacitor Cin law (filter 2) | 190e- + 19.5e-/pF rms |
| Noise hits frequency , threshold set at 4 times the noise rms value | <1kHZ |
| BaselineThreshold dispersion (inside a chip) | 800e- peak-to-peak |
| ENC temperature coefficient (20-60°C range) | +0.4%/°C |
| Baseline variation (20°C-60°C) | <1 DAC LSB |

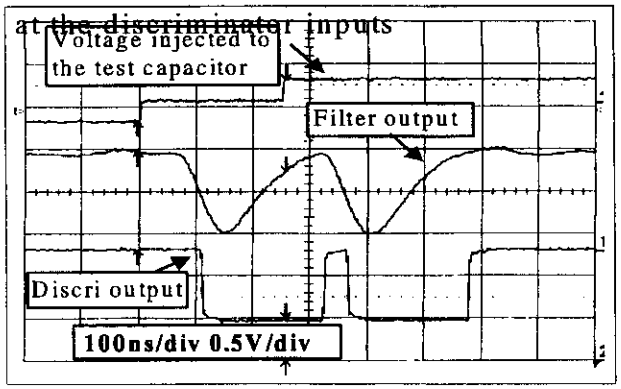


Fig. 11: Double pulse resolution (16fC input, thresold=6000 e-).

The measured double pulse resolution for two 16fC input signals, with a threshold set to 6000 e- is 260ns (Fig11), compatible with the 2.6%/channel occupancy previously estimated.

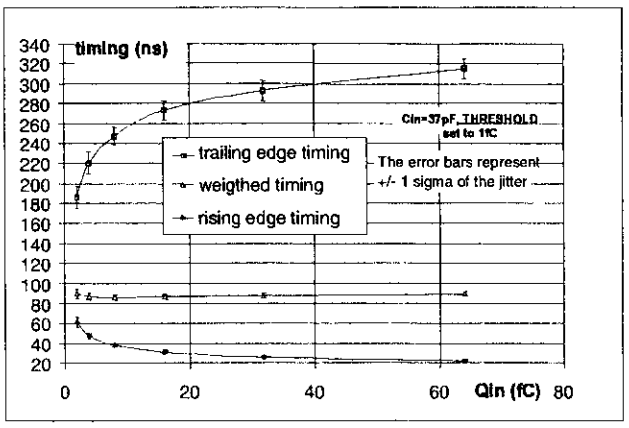


Fig. 12 :SFE16 walk and jitter.

As expected, the time walk refered to the leading edge discrimination is higher than 60ns. It is reduced (Fig. 12) to less than 10ns, when the timing is calculated from a weighted sum of the two edges timings as described in II.C. For the two types of discrimination, the electronics jitter remains smaller than 4ns rms.

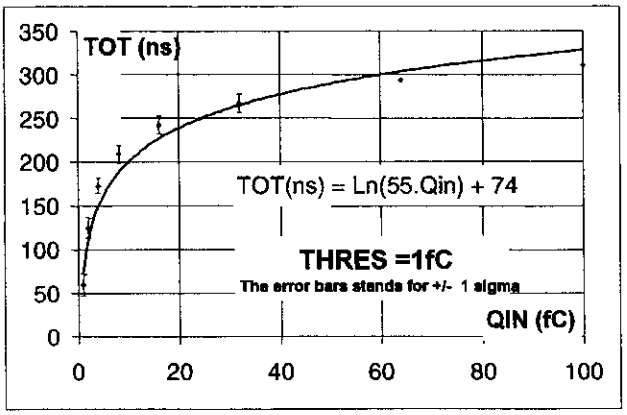


Fig. 13: TOT vs input charge law

The Time Over Threshold law obtained for impulse inputs is plotted in Fig. 13. Its precision is limited by the jitter on the trailing edge measurement.

## *B. Tests With Detectors*

The SFE16 chip has been successfully associated with both 15cm and 26cm microstrip length Micromegas detectors. The detector strip pitch was 317µm. The measured noise levels are plotted in Fig. 10. They tend to predict an ENC in the range of 1400 e- for the final 40cm-long detectors.

The 26cm microstrip length detector, associated to the SFE16 chips, has been tested in the 10GeV PS pion beam and in the 190 GeV COMPASS SPS muon beam at CERN. During these tests, two types of gas, with characteristics summarized on Table3, have been mainly studied.

Table 3: Summary of the characteristics of the two gas mixture tested

| Gas | Ar -$iC_4H_{10}$ 89%-11% | Ne-C2H6-CF4 79%-11%-10% |
|---|---|---|
| Mean number of primary electrons | 32 | 15 |
| Duration of the detector signal | 105 ns | 70 ns |

During all the tests, the threshold was set to 4250 e-, ensuring a noise hit frequency smaller than 1kHz for each channel.

For both gas mixtures, a plateau (Fig. 14) with an efficiency of more than 99% is reached, for modest detector gains (1500 with Ar, 2300 with Ne).

The tests in the COMPASS muon beam, were performed at the nominal intensity of $2*10^8$ muons per SPS spill. Operating the detector at the previous gain values, a maximum rate of 120kHz per strip was recorded, generated mainly by the flux

of particles from beam and target halos. In such conditions, we observed a number of discharges per spill of ~1 and ~0.1 for the Argon and the Neon based mixtures, respectively.

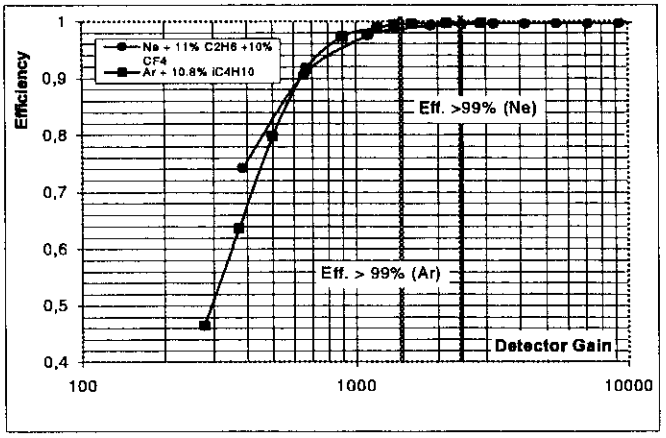


Fig. 14: Efficiency vs detector gain (15kHz 10GeV pion beam).

The timing distribution for a run taken on the pion beam, with a flux of 15kHz, using the Neon based gas mixture and a detector gain of 2300, is plotted in Fig.15a-d. In the plot a, only leading edge discrimination is used. The distribution of the timing is not gaussian and presents a 28ns rms jitter, dominated by the electronics time walk. While in the plot d, where both edges discrimination is used, the timing resolution is improved to 8.5ns rms and presents a gaussian shape. This timing resolution, half due to the detector jitter, is then better than the 100ns peak to peak required one.

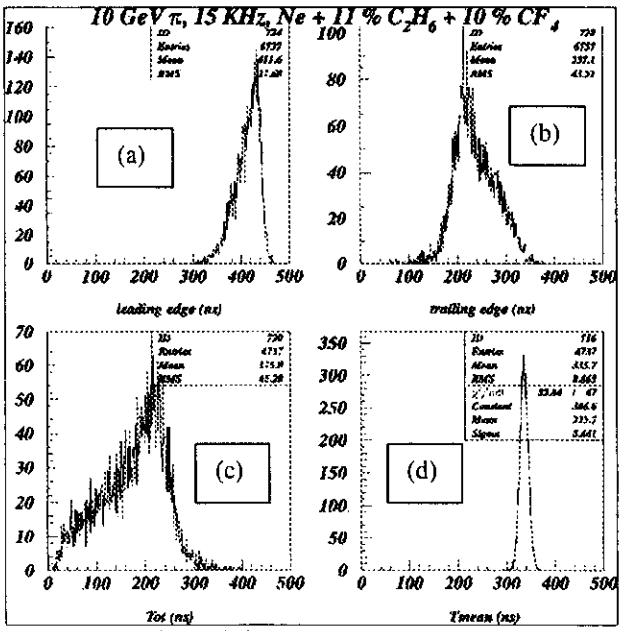


Fig. 15 a,b,d: Timings relative to the trigger measured on the pion test beam with the Neon based mixture: (a) leading edge, (b) trailing edge, (d) timing using both edges. (c) TOT distribution.

On the same beam, with the same conditions, the detector spatial resolution has been measured, using a tracker composed by three Micromegas. For perpendicular tracks, the spatial resolution is 75μm rms, when only the digital information is used. It is improved to 50μm rms when the TOT information is taken into account. In this case, the two strips of the cluster (the mean cluster size is 2.1) presenting the highest TOT are used and the reconstructed position is calculated as their barycentre using the TOT informations as weights.

Both spatial and timing resolutions are degraded by 20 % when the Argon based mixture is used.

## IV. Conclusion

The first prototype of a new front-end chip has been successfully tested. Associated with nearly final Micromegas detector, it already fulfills the major requirements needed for the SAT tracker of the COMPASS experiment. It has been used to test the detector in various gas and beam conditions, and to validate the signal treatment options chosen , as the compensation of electronics time walk by using both edges discrimination. It will allow to choose the gas to be used for the final experiment. However, some performances of the chip can still be improved, as for instance its threshold uniformity. The shaping time may also be revisited, taking into account the progress on gas choice, to decrease the channel occupancy. A final chip including these improvements will be submitted in the next months.

## V. References


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