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3rd RD49 Status Report
Study of the Radiation Tolerance of ICs for LHC

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1 Executive Summary

1.1 Introduction

Before the initiation of the RD49 project [1] in March 1997 it was widely believed that the electronics for the trackers and calorimeters of ATLAS and CMS would have to be built entirely from custom-developed ASICs using the relatively expensive radiation-hardened technologies available from only a few specialized, low-volume manufacturers. However, because of the very demanding requirements of the LHC front-end electronics, there was some concern about the stability and reproducibility of these dedicated rad-hard processes and the risk of some of them being withdrawn. At the same time it was also believed that the less severe radiation environments of the outer detectors would permit the trouble-free use of Commercial-Off-The-Shelf (COTS) components and ASICs developed in standard, non-hardened technologies. However, many years of experience in the Space community showed that there were actually significant risks associated with such an approach.

In view of all these uncertainties the RD49 project was approved in March 1997 with the dual objectives of first assessing a new approach to the development of radiation-tolerant ASICs for the outer detectors and secondly establishing collaboration with experienced radiation effects specialists in the Space agencies. It was hoped that, if a sufficiently high degree of radiation tolerance could be achieved, the RD49 approach could even provide a lower-cost, fall-back solution for the tracker and calorimeter electronics.

RD49's proposed new approach for ASIC developments was based on special radiation-tolerant design and layout methods to be applied in high-volume, commercial-grade sub-micron CMOS technologies. As a result of the RD49 work and the improved contacts with the Space agencies it was realized that the selection, qualification and procurement of sufficiently radiation-tolerant Commercial-Off-The-Shelf (COTS) components for the LHC experiments would be a much more complex, labour-intensive and risky procedure than had been anticipated. There was an urgent need of co-ordination of effort and the definition of recommended guidelines to minimize risks. The LEB therefore requested RD49 to propose a separate COTS framework project - this was presented to the LEB and approved in March 1999 [2].

Over the past three years RD49 has achieved outstanding results in two main areas that will have a major impact on the construction of electronics systems for the LHC detectors. First, the project has been successful in developing and demonstrating a design methodology, based on deep-submicron CMOS technology, that allows the production of lower-cost ASICs with robust radiation-tolerance. The radiation-tolerance achieved by this method far exceeds the original expectations. The second important contribution has been the improvement in the understanding and awareness within the HEP community about the important, but previously ignored, 'Single Event Effects' (SEE) in ASICs and COTS components. However, much still remains to be done, especially in the domain of risk management concerning the various radiation effects issues associated with the use of COTS components in LHC experiments.

1.2 Summary Of Results From The First Year

In its first year of activity RD49 demonstrated the radiation-tolerant approach at the device level. Total dose effects in CMOS technologies (threshold voltage shifts, leakage currents) are caused by the accumulation of radiation-induced holes trapped in the gate and field oxides. However, the thin gate oxides employed in deep submicron MOS technologies allow tunneling electrons to effectively neutralize trapped holes in the gate oxide. For gate oxide thickness below ~6nm, as employed in quarter micron CMOS technologies, the electron tunneling effect neutralizes trapped holes throughout the entire thickness of the gate oxide. To complete the radiation hardening, the layout of the NMOS transistor is made edgeless and is surrounded with guard-rings. This eliminates the radiation-induced leakage paths caused by holes trapped in the "bird's beak" and in the thick field oxide between devices. The use of guard rings also enhances the hardening against Single Event Latch-up. Since it depends only on the fundamental physics of electron tunneling in silicon dioxide and the use of 'edgeless' transistor geometry, the radiation-tolerant design approach was expected to be applicable in principle to all deep submicron MOS technologies, and to be insensitive to variations in the process parameters from run to run.

An initial investigation into the use of Commercial-Off-The-Shelf-components (COTS) in the LHC radiation environment showed that it poses formidable challenges. The LHC community would have to face complex issues in the selection, test, qualification and procurement of such COTS components.

1.3 Summary Of Results From The Second Year

In the second year of activity, RD49 characterised test devices in the 0.25μm technology and also developed several demonstrator circuits – a small array of pixel readout cells, a fast preamplifier, a few logic cells and a shift register as a test vehicle for digital circuits. These circuits were all designed with the radiation tolerant approach. Radiation testing of these demonstrator circuits revealed an impressive degree of radiation tolerance in excess of 10 Mrad of total dose for both digital and mixed-signal circuits. These demonstrator circuits also showed extremely good stability of their electrical characteristics. In particular, threshold voltage, carrier mobility and noise performance were very stable after 30 Mrad [3]. Further tests with protons has demonstrated a radiation-tolerance to a fluence of more than 9.10^{14} p/cm^2[4].

Similar hardening performance was obtained with two different quarter micron technologies, proving that this radiation tolerance depends only on the intrinsic properties of deep submicron technology, and does not differ substantially between silicon foundries. Building on the results of the demonstrator chips, a radiation tolerant standard cell library of 30 core cells and 10 I/O cells was developed in a quarter micron CMOS technology [5]. A model of the NMOS device with enclosed geometry was developed and integrated in CADENCE CAE tools. The sensitivity of 0.25μm CMOS digital circuits to 'Single Event Upsets' (SEU) was investigated by using heavy ions on three different shift register designs (static, dynamic and SEU-hardened designs). In the case of the SEU-hardened shift-register, the Linear Energy Transfer threshold value (LET_{th}), above which SEUs were observed, was found to be 89 MeVcm^{2}mg^{-1} when the circuit was not clocked during the irradiation - this is an excellent result. On the other hand, clocked circuits exhibited a much lower LET_{th} of 5.6 MeVcm^{2}mg^{-1}. In collaboration with CMS, a simulation method was developed for the prediction of the SEU rate in the LHC radiation environment. This method predicted upset rates, in the CMS tracker regions, for a submicron technology to be of the order of 8.10^{-7} to 8.10^{-10} upset/bit/s depending on the distance from the beam.

A common specification for a radiation tolerant Voltage Regulator was established with ATLAS and CMS, and a contract was signed with ST Microelectronics (STM) to develop it using a STM power bipolar technology that RD49 has already tested up to 1 Mrad and 2.10^{13} neutrons/cm^2. The importance of the selection, qualification and procurement of radiation tolerant COTS started to be recognized within the LHC community, and a proposal for a framework project to co-ordinate the usage of COTS at LHC was presented and approved by the LHC Electronics Board. Preliminary guidelines for COTS selection, qualification and procurement procedures for LHC experiments were investigated.

1.4 Milestones And Results For The Third Year (1999)

The LEB Committee set the following three milestones for RD49 to achieve in 1999:

(1) For the selected quarter-micron technology study:
- Complete the study of Single Event Effects and develop upset-tolerant circuit designs (flip-flops etc.)
- Complete the study of the analog characteristics of the process (device matching, flicker noise, charge injection in SC circuits, analog models, etc.).
- Develop standard monitoring structures for inclusion on future runs.

(2) Transfer of the radiation-tolerant design technique to LHC development teams:
- Advise and support LHC development teams using the RD49 rad-tolerant approach:
  - Development of a design kit and digital library for the CADENCE platform ,
  - Organization of quarter micron Multi-Project-Wafer runs.
- Develop radiation-tolerant LHC ASIC designs in quarter micron technology:
  - ALICE and LHCb pixel detector readout circuit
  - Front end electronics for the Silicon Drift Detector of ALICE
  - 1.2 Gbit/s digital link for detector readout.
  - receiver for the 80 Mbit/s digital link for the control of the CMS tracker,
  - 40 Msample fibre optic analog driver for CMS tracker readout

(3) In a joint project with ST Microelectronics complete the development and characterization of a rad-tolerant voltage regulator (test of the prototype and assessment of its conformity to the specifications defined together with the LHC collaborations).

1.4.1 Overview Of Achievements In 1999

In 1999 the RD49 collaboration concentrated on the milestones set by the LEB and developed several radiation-tolerant deep submicron CMOS circuits for LHC applications, coordinated COTS components issues in the LHC experiments, and developed a radiation-tolerant voltage regulator to meet LHC specifications. Thus, the third year of RD49's activity has seen the first fruits of the R&D effort invested in the previous two years. A call for tender was carried out to select a single supplier for 0.25μm CMOS foundry services for LHC applications. CADENCE design kits developed by RD49 to support the radiation tolerant design method in the selected technology were distributed to several HEP labs. As a result, several digital, analog and mixed-signal rad-tolerant ASICs have been successfully designed and tested in the

adjudicated quarter micron CMOS technology. These circuits encompass a very large spectrum of successfully developed radiation-hard and tolerant circuits, ranging from low-noise analog circuits, through an A-to-D converter, to very high-speed circuits for Gbit/s digital readout links. This wide spectrum of circuits confirms the effectiveness and the flexibility of the radiation-tolerant design approach. Several radiation-tolerant ASICs developed in the framework of RD49 have been presented at the LEB Snowmass conference.

1.4.2 0.25 micron ASICs

The preliminary radiation tests performed on the radiation-tolerant ASICs developed by members of the RD49 collaboration show an almost inalterable stability of the analog and digital performance, even after a 10 Mrad total dose exposure with X-rays. The performance of the following ASICs has been successfully measured before and after irradiation:

- 1.25 Gbit/s serializer for LHC data and trigger optical links [18]
- Amplifier with AGC for the 80 Mbit/s optical receiver for the CMS tracker [19]
- Dual-ported static 2k x9bits RAM circuit [20]
- 40 Mhz PLL circuit for the CMS tracker [6]
- Large dynamic range analog memory for the ALICE SDD front end readout
- A fast current sensitive low noise amplifier test circuit [7]
- A Multi-channel low power 10 bit A-to-D converter for the ALICE SDD front end readout
- An I^2C slave ASIC for the CMS muon chamber.

Several of these circuits have used the radiation-tolerant digital cell library developed in 1998 and enhanced in 1999 – this library is now included in the design kit made available to LHC design teams.

Several other ASICs have been also successfully developed and tested by other teams of the LHC community:

- APV-25: the complete front-end readout circuit for the CMS tracker, with 3 different preamplifier-shapers, by Imperial College, Rutherford Lab. and CERN [8]
- Beetle: a front-end circuit for the LHCb silicon tracker, by the ASIC Lab Heidelberg [9].

All of these quarter micron ASICs were functional and met their specifications. Results of the radiation tests performed up to 10 Mrad have shown an impressive stability of performance after radiation. Digital circuits do not show any sign of speed or functional degradation and there is no increase of power consumption. Mixed-signal circuits do not exhibit a visible degradation of their analog performance and in particular the noise performance of low-noise front-ends was very stable. All these consistently excellent results have reinforced our confidence in the radiation-tolerant design approach.

1.4.3 Study Of Analog Characteristics And Design Techniques

Two complex switched capacitor mixed-signal circuits have been developed; a 1mW, 10-bit, 4 Msample/s ADC, and a 2-volt analog memory. These circuits use the two types of capacitor available in the selected quarter micron technology: a high-precision low-density capacitor in the case of the ADC, and a high-density low-precision capacitor for the analog memory. The results obtained on both circuits fulfil the target specification, and radiation tests up to 10 Mrad total dose (X-rays) do not show any visible degradation. These demonstrator circuits will be used next year as the basis to build the Silicon Drift Front End of ALICE. Further study of the noise has confirmed the low noise characteristic of the quarter micron process, but the excess flicker noise observed on short channel (<0.6μm) NMOS transistors has not yet been explained [10].

1.4.4 SEU Study

The understanding of Single Event Upset in the LHC environment has greatly improved this year. This effort was carried out in close collaboration with CMS. The computational method developed last year to estimate the error rate has been refined by extracting information concerning the sensitive volume size from available heavy ion irradiation data. To check the validity of the methodology, measured proton irradiation data have been compared with simulation results for the same component. The results of such comparison are very satisfactory, confirming the validity of the simulation approach. The details of the computational method have been reported in a complete paper [11].
The study of the Single Event Effects sensitivity of deep submicron ASICs has been carried out at the cyclotron of Louvain-la-Neuve (Belgium) using proton and heavy ion beams. Shift registers made up of the several types of DFF cells have been exposed. As expected, dynamic cells are far more sensitive to SEU than static cells, their threshold charge for upset being considerably lower. Standard static cells can be made even more resistant by modifying the

aspect ratio of some transistors, or by adding a capacitive load to some nodes. The effectiveness of this approach has been measured, and all the results referring to this study on shift registers have been included in the LEB workhop proceedings [20]. SEU measurements took place also on real circuits developed for LHC: a dual-ported static RAM and a serializer for a Gbit/s optical link, both designed in the quarter micron process using radiation-tolerant design techniques. For both circuits, we have traced the cross-section curve for an irradiation with heavy ions. From this curve, it is possible to estimate the upset rate these circuits would experience in the LHC radiation environment. For the SRAM, the dominant error mechanism was single bit error, and the estimated rate, for instance, in the outer tracker and behind the End-cap of ECAL is $2.1 \cdot 10^{-6}$ and $6.6 \cdot 10^{-6}$ upset/(chip·s) respectively. For the serializer, the dominant error mechanism was loss of synchronization, and this very recent result is still under study to understand what causes this error to appear, and how to protect the circuit/system against it. No Single Event Latchup has ever been observed in any of the circuits irradiated with either protons or heavy ions - up to a LET higher than 100 $MeVcm^2mg^{-1}$.

1.4.5 Readout Circuit For Pixel Detectors

Following the successful development in 1998 of a small 130 channel pixel readout prototype, the design of a full 8000 channels pixel readout chip was started for application in the ALICE pixel vertex detector and LHCB RICH. For LHCB 8 pixels of 50 by 425 square micron are grouped into one big pixel of 425 by 400 square microns, which contains more than 12000 transistors[12].The full chip size is about 13.6 mm by 16 mm, and contains about 13 million transistors [13]. The design is carried out systematically using edgeless NMOS transistors to provide radiation tolerance. The large die size put special constraints on the design, and required the use of six metal layers.

1.4.6 Design Support And Technology Access

A call for tender resulted in the selection of one company to supply quarter-micron CMOS foundry services for LHC applications for the four years through to and including 2003. A corresponding CERN ‘frame contract’ is now almost ready for signature - it allows for optional extensions to the agreement beyond 2003. In 1999 a MPW run combining 17 different designs was organized in the selected 0.25μm technology and resulted in the successful delivery of the demonstrators and LHC ASICs mentioned above.
The Cadence design kit supporting the radiation-tolerant design method in the selected quarter-micron technology was further enhanced. The radiation-tolerant digital standard cell library was extended to include 30 logic cells, 18 types of I/O and power pads. The design kit and library were distributed to 5 institutes.

1.4.7 RD49, COTS Meetings And New Institute Member

In 1999 two RD49 collaboration meetings were held at CERN in which experts from European industry, the European Space Agency, the French National Space Centre (CNES), and several other specialized institutes participated. Members of ATLAS, CMS, ALICE, LHCb and the LHC machine groups who are active in the domain of COTS also attended these meetings. During the December meeting the Cyclone Group of the University of Louvain-La-Neuve expressed interest to participate in RD49. This group has already a wide expertise in SEE testing through its long collaboration with ESA, and will advise RD49 collaborators and LHC users on experimental methods for evaluating SEU.

1.5 COTS Project

The COTS coordination project was approved by the LEB in March 1999 with the following objectives:

(1) Define and document (on the web) appropriate test procedures for identifying COTS electronic components and sub-systems that will operate reliably in the particular radiation environments of the LHC experiments and the LHC machine.
(2) Organize an appropriate database framework to facilitate the collection and sharing of the results of the above defined test procedures for the various COTS components and subsystems.

The use of COTS components in the radiation environment of the LHC has been the subject of several meetings with engineers from ATLAS, CMS and the LHC machine. One of the first tasks of this COTS working group has been to improve the understanding of the COTS issues in the Collaborations by giving tutorials within ATLAS and CMS[14]. To further improve the situation, a one-week course on radiation effects in electronic systems has been scheduled for the first quarter of 2000 in collaboration with the CERN Technical Training service.
Preliminary guidelines for COTS selection, qualification and procurement procedures for LHC experiments have been discussed. In a pragmatic approach that takes into account the shortage of resources and the lateness in the LHC development program, a simplified proposal for a qualification procedure for COTS components has been proposed within CMS [15]. This qualification procedure is tailored to the particular radiation environments of the muon detectors and the hadronic calorimeter - it recommends irradiation with 60-200 MeV protons so as to identify any risks associated with SEE (total dose risk is not considered to be an issue in these environments).

1.5.1 Radiation Tolerant Voltage Regulator

In collaboration with ST Microelectronics, a radiation tolerant positive voltage regulator based on a specification agreed by ATLAS and CMS, has been developed with a guaranteed hardening level of 500 krad and 2.10^{13} neutrons/cm^2. A prototype has been tested, and its basic functionality and performance have been demonstrated. Preliminary results of radiation tests have shown the correct performance of the circuit up to 10^{14} protons/cm^2, and 4 Mrad total dose (X-rays)[16]. Statistical measurements performed at CERN on one wafer have shown a yield of more than 90%. After correction of minor design imperfections, a final prototype of the positive voltage regulator has been submitted for manufacturing and should be available to LHC detector teams in the first quarter of 2000. At the request of ATLAS and CMS, the development of a negative version of the voltage regulator has also been negotiated with ST Microelectronics. A first prototype of the negative version should be available for evaluation at CERN during the second quarter of 2000.

1.6 Radiation test equipment

At CERN a laboratory-based X-ray irradiation facility has been built up to support radiation testing and later to monitor the radiation-tolerance of wafers delivered during the production phase of the LHC electronics. This irradiation facility is built around an X-ray machine from Seifert Gmbh that has been customized following our specification and can perform the irradiation of un-lidded packaged samples, hybrid circuits and wafers (up to 8 inches diameter). A Labview program allows the control of the X-ray machine, the temperature of the wafer chuck (-15º C to 125º C), the positioning of the wafer probe and the operation of the test and measurement instruments. This equipment has been successfully used to characterize the first wafer of the radiation tolerant Voltage Regulator fabricated by ST Microelectronics.

1.7 Proposed objectives for 2000

In the year 2000 the RD49 collaboration proposes to concentrate on three important areas:

- COTS
- Quarter-micron technology
- Further study of SEU at the LHC
- In-situ dosimetry for the LHC experiments

1.7.1 Objectives For COTS

1. Support the CERN Technical Training action on radiation effects in electronics.
2. Complete the development and radiation-tolerance study of the rad-tolerant positive voltage regulator, and prepare its industrialization in collaboration with ST Microelectronics.
3. Complete the development of the negative rad-tolerant voltage regulator with ST Microelectronics
4. Advise and assist the LHC experiments in setting up approved qualification procedures for COTS in their radiation environments.
5. Assessment of a qualification test procedure for the evaluation of the Low Dose-Rate Effect in bipolar technologies in the LHC radiation environments.
6. Provide radiation effects consultancy on request of the LHC machine community.
7. Organize the compilation of radiation data on COTS for LHC experiments
8. Complete the development and calibration of the proton and neutron irradiation facilities (IRAD1 and IRAD2) at the CERN PS; coordination of irradiation runs for users.

1.7.2 Objectives For Quarter-Micron CMOS Technology

1. Monitor the performance and radiation-tolerance of the selected 0.25 micron CMOS process
2. Complete work on analog demonstrators for LHC experiments (front-end circuits for the binary readout of ATLAS Si strips and LHCb muon detector) and complete the characterisation of the existing demonstrators.
3. Finalize the measurements on device matching.
4. Transfer of the design of the ADC and analog memory to ALICE for the SDD front end
5. Support the submission of MPW runs in the selected 0.25 micron technology for the HEP community.
6. Support on-going quarter-micron ASIC designs for the LHC experiments.
7. Transfer maintenance of the design kit to Rutherford Lab

1.7.3 Objectives for SEU study

1. Further SEU measurement and SEU-optimization of rad-tolerant 0.25 micron digital circuits (memory, Gbit link, and others).
2. Compare experimentally the rates of neutron and proton induced upsets (at the same energy) in order to further validate a proposed simple qualification procedure for COTS and ASICs.

1.7.4 Development Of A Dosimeter Adapted To Requirements Of The LHC Experiments

Develop active dosimeters for in-situ dose monitoring in the LHC experiments. Two approaches will be explored: the use of high sensitivity RADFETs with a reset feature and alternatively the use of optically stimulated luminescent films[17]. A specification common to the requirements of the LHC experiments and the LHC machine groups will be established in collaboration with experts of the CERN radiation group.

2 Analog Performance And Mixed-Signal Demonstrator Circuits

Commercial submicron technologies are intended for large volume digital applications, and data available on noise and matching are generally missing or incomplete. The power supply voltage used in a typical 0.25 μm technology, 2.5 V poses new design challenges especially for circuits like switched capacitors used in ADC and analog memories. Examples of some of these challenges are:

- the lack of dense and precise capacitors. The evolution of deep submicron processes is generally driven by digital applications, and therefore these processes do not have, at least in their early stages, many of the important features for analog design;
- the presence of substrate noise in mixed-mode integrated circuits;
- the reduced power supply voltage, compared to less advanced technologies.

Two radiation tolerant demonstrator mixed-signal circuits have been developed - a 10 bit ADC and a large dynamic range analog memory.

2.1 Noise Characteristics

More extensive noise measurements have been performed this year on the quarter micron CMOS technology. Results indicate, as shown in figure 1(left) that the thermal noise coefficient Γ is minimized when the transistor operates in weak or moderate inversion. Measurement of the radiation response of the flicker noise coefficient Ka (see the right part of figure 1) as function of the total dose shows an increase of a factor 1.6 (NMOS) to 3.5 (PMOS) after 30 Mrad.

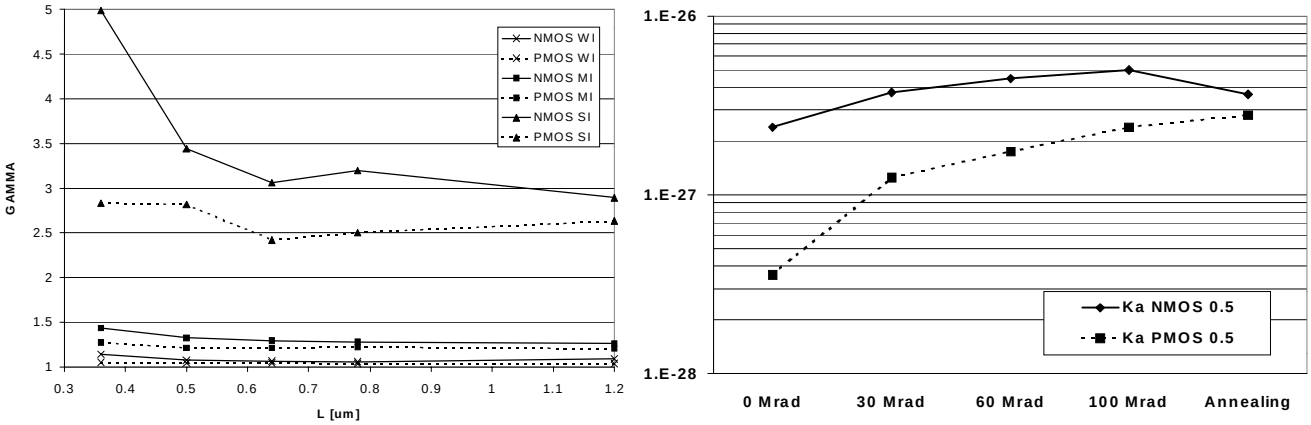


Figure 1 Left- *Noise coefficient Γ extracted for PMOS and NMOS transistors of W= 2000 μm and for different gate length. Measurement is done for 3 biasing conditions, weak, moderate and strong inversion.* **Right**- *Flicker noise coefficient Ka extracted as a function of the total dose*.

2.2 A Multi-Channel Low Power 10 Bit A-To-D Converter

The main purpose of the development of this ADC was to demonstrate the effectiveness of our radiation-tolerant approach on switched capacitor circuits, which are fundamental building blocks in data acquisition systems for high energy physics. In addition, an ADC circuit is the ideal mixed-signal circuit demonstrator because it utilizes several analog and digital circuits, and the digitization operation probes itself the characteristics of the circuit.

For the design of this ADC circuit we have systematically used enclosed NMOS transistors to obtain an effective hardening in 0.25 μm CMOS technology. Unfortunately, the technology operates with a maximum supply voltage of 2.5V, and because of the tight constraints on space and power dissipation typical of high energy physics experiments, conventional switched capacitor circuits can not be easily replaced by alternative architectures more suitable for low voltage operation. Therefore, limitations induced on switched capacitor building blocks by low voltage supplies are an important issue to investigate on experimental circuits.

The choice of a charge redistribution ADC for the architecture stems from the fact that this circuit has only two critical blocks and failure modes can be easily identified. Additionally, this kind of converter is needed in the implementation of some detector Front-ends presently under design, such as the front-end chip for the Silicon Drift Detectors (SDD) of ALICE.

For compatibility with the ALICE application we have targeted a resolution of 10 bits - which usually can be attained without the need of cumbersome calibration procedures - a conversion speed of 250ns or 4 Msample/s (40MHz sampling frequency clock) and an aggressive power budget of 1mW.

2.2.1 ADC Architecture

The converter utilizes a successive approximation technique, based on the principle depicted in figure 2. This architecture has been chosen because it allows low power consumption in deep submicron technology while operating at sampling frequency above 1 Msample/s. The circuit consists basically of a comparator and a digital-to-analog converter, made of capacitors with binary weighted values. The DAC is used both to sample the input signal and to provide partitions of the reference voltage necessary for the digitization.

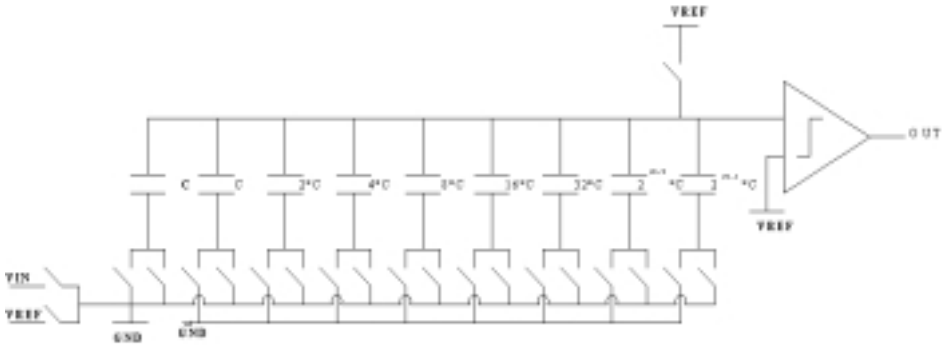


Figure 2 *Basic scheme of an n-bit charge redistribution ADC*

The conversion is performed in three steps:

- In the first step, the bottom plates of capacitors are connected to the input voltage V_{in}, whereas the top plate is connected to the reference. The ADC is in the acquisition mode.
- In the second phase the bottom plates of the capacitors are switched to ground and the switch connecting the top plate to V_{ref} is opened. Due to the charge conservation, the voltage on the top plate changes from V_{ref} to V_{ref} - V_{in}. The ADC is in the hold mode.
- In the last step, the ADC enters the conversion mode and finds the digital code by determining one bit per clock cycle.

2.2.2 Circuit Implementation

The 0.25μm technology used in the implementation of this ADC has very linear metal to metal capacitors with a satisfactory density; therefore this capacitor has been chosen for the implementation of the DAC. Assuming that a capacitor of 75fF (the minimum value allowed in the technology) is employed for the LSB, table 1 shows as a function of the number of bits the total area and the total capacitance needed to implement a binary weighted DAC. It is apparent from this table that a direct implementation of a 10-bit DAC would have both a too large silicon area, and a too large load capacitance at the input node of the comparator. The latter, in fact, results in a severe speed limitation of charge redistribution converters. To overcome this obstacle, we have implemented an additional voltage reference on the bottom plates of the capacitors, which provides in this way a sub-division of the reference voltage.

Table 1 *Area and total capacitance of a charge redistribution DAC as a function of the number of bits*

Number of bits	Area (μm^2)	Capacitance (pF)
5	10000	2.4
8	83000	19.2
9	166000	38.4
10	332000	76.8

In our design this has been implemented using a second charge redistribution DAC, as shown in figure 3. In this circuit, the signal is sampled only by the first DAC that operates in stand-alone mode for the decision of the first 8 bits; the second sub DAC is connected only for the last 2 bits via the termination capacitor C.

The timing of the circuit is the following:

- During the *sampling* phase, the main DAC samples the input signal and the sub DAC is grounded.
- In the first *redistribution* cycle, the first eight bits are determined by the main DAC.
- In the second *redistribution* cycle, the termination capacitor of the first DAC is connected to the output of the sub DAC and the two last bits are extracted.

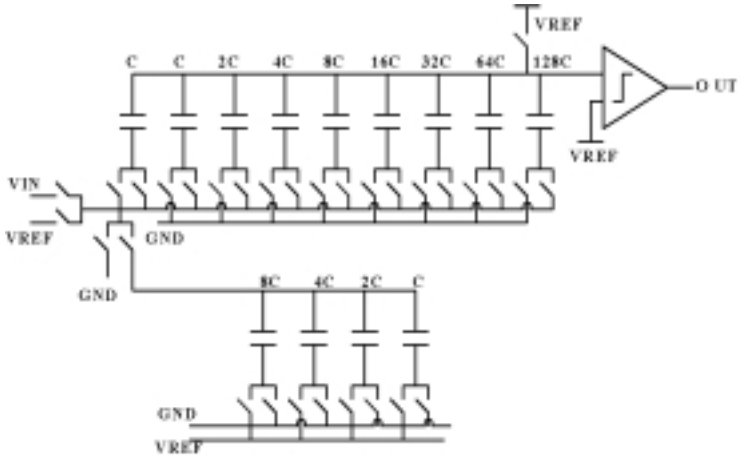


Figure 3 *Simplified schematic of the implemented converter.*

Since no voltage buffer is used between the two DACs, some error due to the direct coupling has to be expected. However, this error affects only the two least significant bits and is reduced by increasing the total capacitance of the sub-DAC. Therefore, it can be easily made negligible at the level of 10 bits resolution.

2.2.3 ADC Layout

The DAC and the sub-DAC have been laid-out by replicating the same elementary cell, corresponding to the smallest capacitor in the array (75 fF). Bigger capacitors are obtained by connecting a suitable number of these small structures in parallel. A common centroid geometry has been used in order to minimize the impact of parameter gradients on the matching between capacitors.

In the technology used to implement the converter, the capacitors are implemented using two higher levels of metal. Therefore, the capacitor array could be shielded from the substrate with a layer of metal1 connected to ground. The layouts of the DAC and of the comparator are shown in figure 4. The larger area is occupied by the DAC, 700 x 150 μm^2. As can be seen from figure 4 (left), a substantial fraction of the area is occupied by the coupling capacitors; this is mainly due to the fact that to optimize matching, a ring of dummy capacitors has been laid-out all around the signal capacitors. The same technique has been applied to all the other blocks in the circuit. To reduce as much as possible the coupling between digital and analog parts the control signals are routed at the periphery of the comparator and therefore all the reset switches are placed near the edges. The total size of a single converter is 0.3 x 1 mm^2

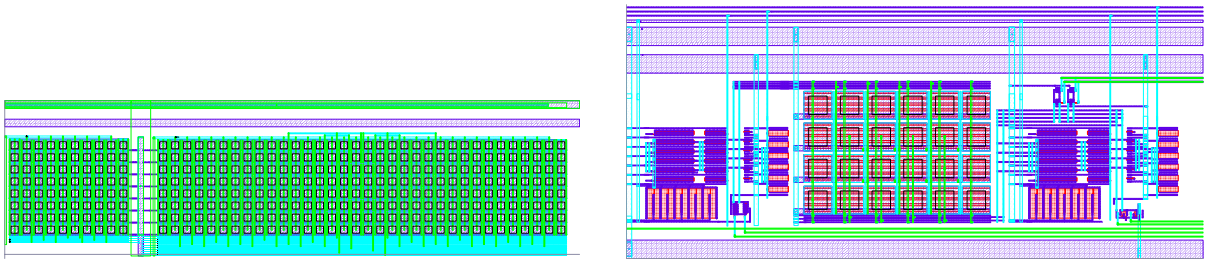


Figure 4 *Layout of the binary weighted DAC and of the voltage comparator.*

2.2.4 ADC Test Results

The converter has been tested using a full-scale sinusoid as the input signal. The output of the converter is sent to a logic state analyzer and a software program calculates the integral non linearity, the differential non linearity and the fast Fourier transform in order to evaluate the distortion.
The tests with a clock frequency of 40MHz detect some missing codes near the MSB transition. This problem is common for all the converters measured and disappears if the clock frequency is scaled to 20MHz. All the other codes are correctly detected and the sizes of the steps are quite uniform; this explains the low level of distortion. All the harmonics are at least -58dB below the fundamental.

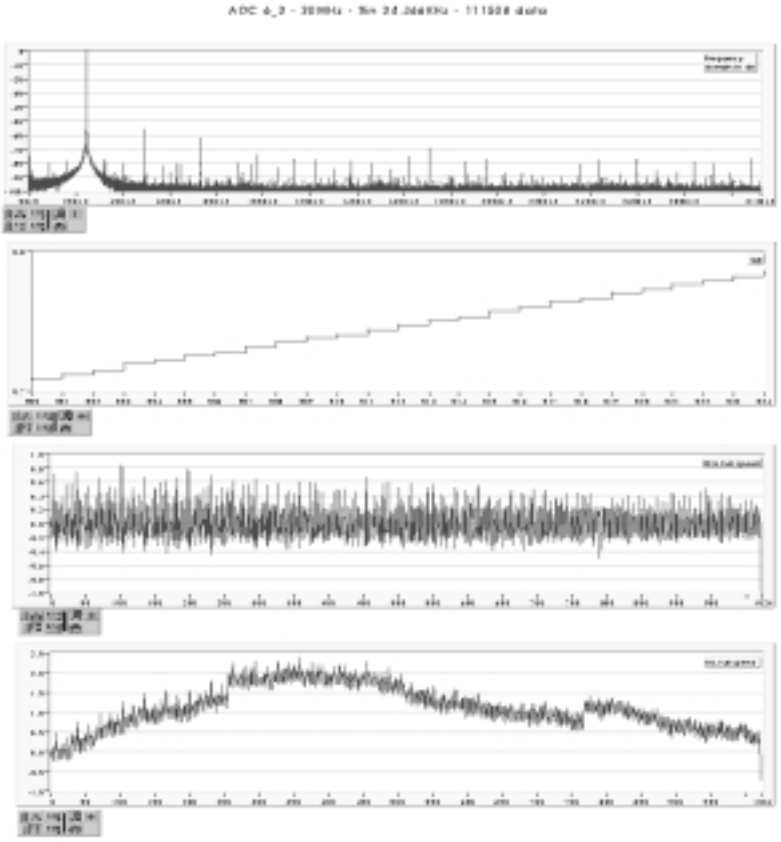


Figure 5 *Analysis of the output of a typical ADC. The figure shows from the top to the bottom: the FFT of the output, the reconstruction of a portion of the input signal, the DNL profile and the INL profile. These measurements were taken with a clock frequency of 20 MHz before the irradiation. After 10 Mrad, no degradation is observed.*

The fact that some codes are missing depending on the clock frequency is clearly a dynamic phenomenon that does not depend on the matching of the capacitors chosen to implement the DAC. Actually, the problem occurs when the inputs of the comparator are very close to the equilibrium and the numbers of missing codes change modifying the bias of the comparator.
Three ADCs have been tested to a total dose of 200krad, 1Mrad and 10Mrad respectively. No degradation in circuit performance was seen in any of the three chips tested and the plots before and after irradiation are remarkably close. Figure 5 shows from the top to the bottom: the FFT of the output, the reconstruction of a portion of the input signal, the DNL profile and the INL profile. These measurements were made with a clock frequency of 20 MHz before the irradiation.

2.3 Large Dynamic Range Analog Memory

A demonstrator analog memory has been designed in a commercial 0.25 µm CMOS process with the aim of studying the various analog design issues for such processes and investigating how far the analog performance of low-voltage high-density mixed-mode integrated circuits can be pushed.

2.3.1 Circuit Principle and Description

The architecture chosen for the memory is showed in figure 6 (left). All the switches are CMOS, the transistors are laid out with enclosed geometry and with guard rings all around in order to prevent post-irradiation leakage currents. Two switches have been used to connect the capacitors to the common lines, in order to have a more symmetric charge injection. The circuit works as follows: during the write cycle the switches SW_W are closed and connect the common lines to the input signal. The switches SW_R are open and the switch SW_F is closed. The digital control logic closes the switches of each cell, one cell after the other, to sample the input signal on the capacitors. The values stored can be read (read cycle) opening the switches SW_W and SW_F, closing the switches SW_R, and connecting the cells one after the other in the amplifier feedback loop. The switch SW_F is closed at the end of the reading of each capacitor to discharge it and to reset the read amplifier.
An example of the timing required is shown in figure 7 (left), where CK is the clock of the shift register which drives

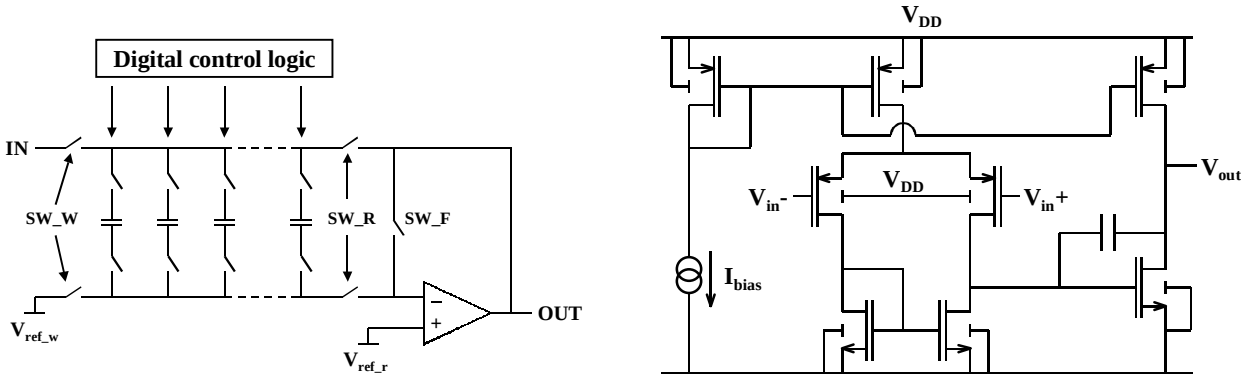


Figure 6 Left - *Schematic of the Analog memory channel;* **Right**- Schematic of the Operational Transconductance Amplifier used as read amplifier.

the switches of the cells and Q1, Q2 and Q3 are the driving signals of the first three cells. In order to avoid charge sharing between adjacent cells, it is very important not to have overlapping between the signals driving two consecutive cells, as shown in figure 7 (right). This has been achieved by inserting between the output of each flip-flop and the corresponding cell a series of inverters with one of them controlled by a low biasing current, as shown in figure 7 (right). This allows to delay the rising edge of each flip-flop output, and in this way the rising edge of flip-flop number n will be delayed compared to the falling edge of flip-flop number n-1. The delay can be adjusted by changing the current in the controlled inverter.
Figure 7 (right) shows that the substrate contacts are connected to a ground (GND) that is separated from the ground to which all the n-channel sources are connected (GNDD). These two grounds have been kept separated on the chip in

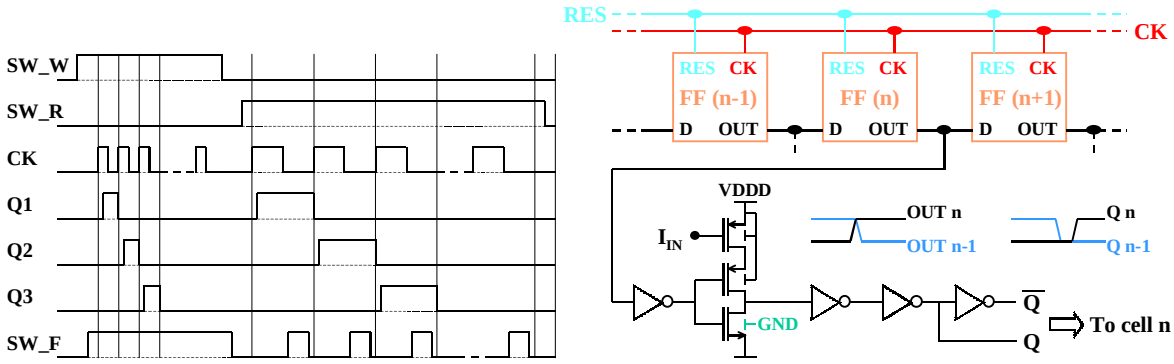


Figure 7 Left -*Example of the timing used to write and read the memory;* **Right**- *Schematic of shift register with non overlapping clocking.*

order to avoid injection of high switching currents locally into the substrate.

The read amplifier has been implemented as a simple Operational Transconductance Amplifier with a Miller compensation capacitor. The circuit schematic is showed in figure 6 (right). The wells of the p-channel transistors have been connected to V_{DD} to increase (in absolute value) their threshold and to be able to work with the inputs (i.e. V_{ref_r}) closer to ground. With I_{bias} = 120 μA the power consumption is around 3.5 mW and the output response to an input step of 1 V has a rise time of 32 ns with a capacitive load of 20 pF.

As anticipated, a problem of using a deep submicron process for an analog memory arises from the choice of the

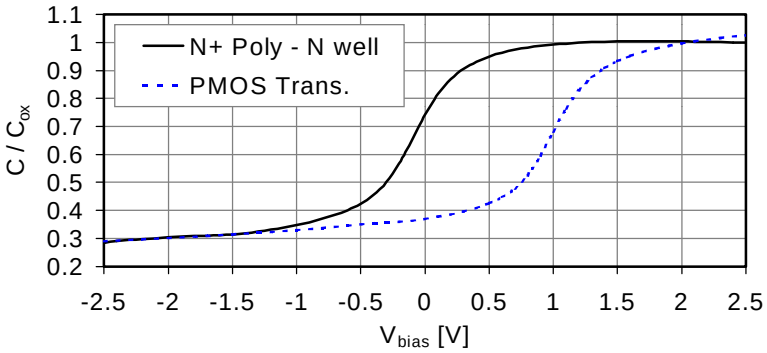


Figure 8 *Comparison between the gate capacitance (normalized to the oxide capacitance) as a function of the bias voltage for a normal PMOS transistor (P+ polysilicon gate – dotted line) and for a N+ polysilicon – N well capacitor.*

capacitors. A possibility is to use a PMOS transistor in accumulation in order to exploit its gate capacitance (which is quite high in deep submicron technologies, being about 5fF/μm^2). In modern technologies, the polysilicon of PMOS transistors is generally strongly P doped (P+), and this gives origin to a flat band voltage around 1 V. As shown in figure 8, this creates some problems because the value of the capacitors varies by a factor three when writing signals from 0 to 2V. In the technology we used there is the possibility to make a capacitor using as dielectric the gate oxide, and as top and bottom plates respectively polysilicon strongly n doped (N+) and N well. In fact this capacitor is like a PMOS transistor with the polysilicon gate N+ doped and without the source and drain diffusions. Using it in accumulation from 0 to 2.5 V we can see from figure 8 that the variation of the capacitor value is smaller than before. From the two curves of figure 8 we can also notice that the difference in the flat band voltage of the two devices is exactly 1.12 V, i.e. the difference in potential between the conduction and the valence bands.

2.3.2 Layout of the Analog Memory

The layout of a single memory cell (turned through 90 degrees) is shown in figure 9. The cell area is 56.1x11.1 μm^2, the CMOS switches use minimum size edgeless transistors, and the capacitor has a value of 600 fF. The layout is symmetric with respect to a horizontal as well as a vertical axis passing through the center of the cell. The cells can be easily abutted, in order to make a channel with as many cells as desired. The clock lines (horizontal lines in figure 9) are made in the third level of metal (the top level) and carry opposite signals, so they should not disturb the top plate of the capacitor. Anyway, a metal-2 plate has been placed between the clock lines and the capacitors to provide some shielding. Guard rings have been used around transistors and capacitors, and another guard ring surrounds each channel.

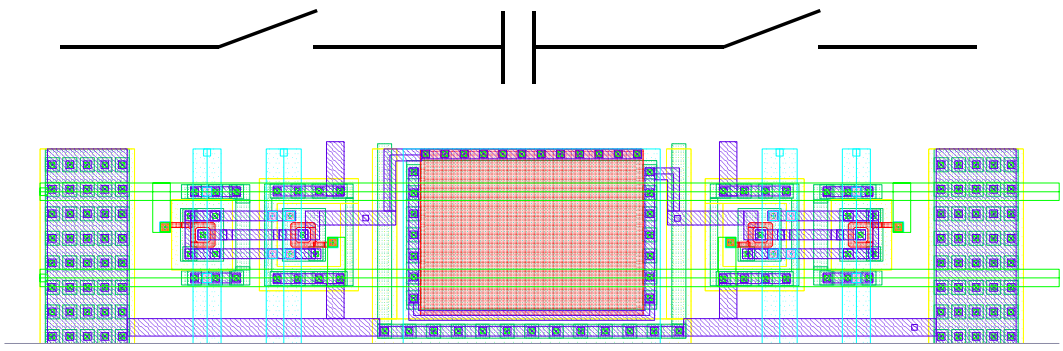


Figure 9 *Layout of an Analog Memory cell.*

A test chip has been fabricated containing 8 memory channels, each one made up of 128 cells and the read amplifier, and the shift register. Attention has been paid to keep the digital circuitry as much as possible separate from the analog parts and to separate the analog ground and V_{DD} (GND and VDD) from the digital ground and V_{DD} (GNDD and VDDD).

2.3.3 Linearity and Dynamic Range of the Analog Memory

The measurement set-up consists of an HP1663EP Logic Analyser and Data Pattern Generator, a Tektronix TDS540 Digital Oscilloscope, a test board and the necessary power supplies and waveform generator. This set-up offers great flexibility in changing the digital patterns sent to the memory and testing quickly the functionality of different chips (chips are packaged in LCC40 chip carriers which fit in the socket of the board and which can be easily changed). The drawbacks of the set-up are that we are limited in precision by the 8-bit ADC of the Digital Oscilloscope and that the noise introduced by the board makes it impossible to measure the intrinsic noise of the analog memory.
The Input – Output characteristic of one channel of the analog memory is shown in figure 10 (left). The linearity starts to deviate from a straight line for input values higher than 2 V. Fitting with a straight line the characteristics measured for few channels and extracting the slope of the fit we find the DC gain, which is always very close to one (between 0.967 and 0.976).
Figure 10 (right) shows the deviations of the Input – Output characteristic from the linear fit. It is interesting to note that

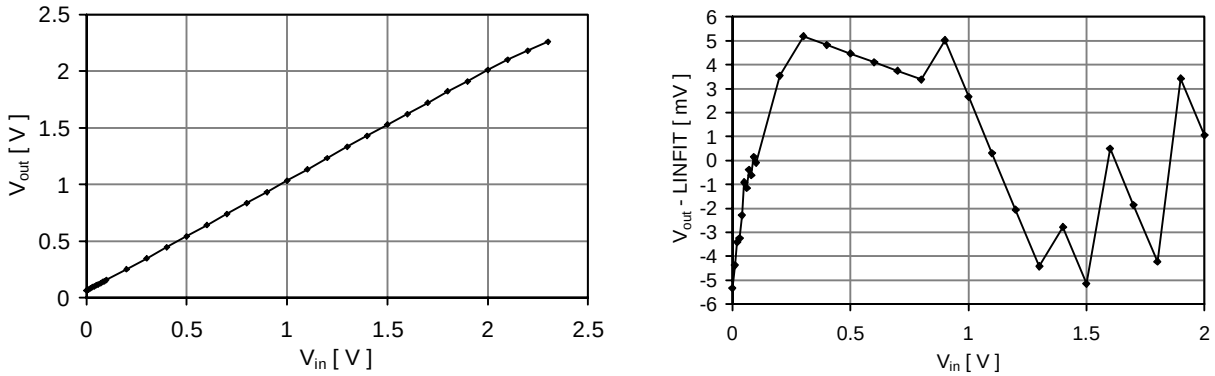


Figure 10 Left - *Input-output characteristic; the dynamic range is 2V***; Right -** *Deviation from linear fit.*

the deviation varies from its minimum to its maximum for an input signal varying from 0 to 0.5 V. This is probably related to the change in the capacitors value when writing signals in that range. If we define the dynamic range as the signal-to-noise ratio, a dynamic range between 11 and 12 bits is found.

2.3.4 Pedestal Uniformity and Noise

We have measured the output of all the cells of the memory with a 0V input voltage. The pedestal variation is ± 1 mVpp over 1 channel and ± 3.5 mVpp over the entire memory.
The noise of each cell has been measured to be around 0.8 mV rms, and this number is dominated by the noise due to the measurement set-up.

2.3.5 Radiation Tolerance of the Analog Memory

The test of the radiation tolerance of the analog memory was performed with the 10 KeV X-rays Seifert RP149 irradiation system of the CERN microelectronics group. We irradiated the chip up to a total dose of 10 Mrad (SiO_2) with a dose rate of 31.6 Krad/min. During irradiation the chip was biased, clocked and with a DC input signal of 1.5V. As can be seen in figure 11 (left), the irradiation did not affect the dynamic range. The systematic variation observed in the pedestal pattern (figure 11 (right)) does not come from radiation effects, but from variations in charge injection of the test board due to change in clock and signal wires position.

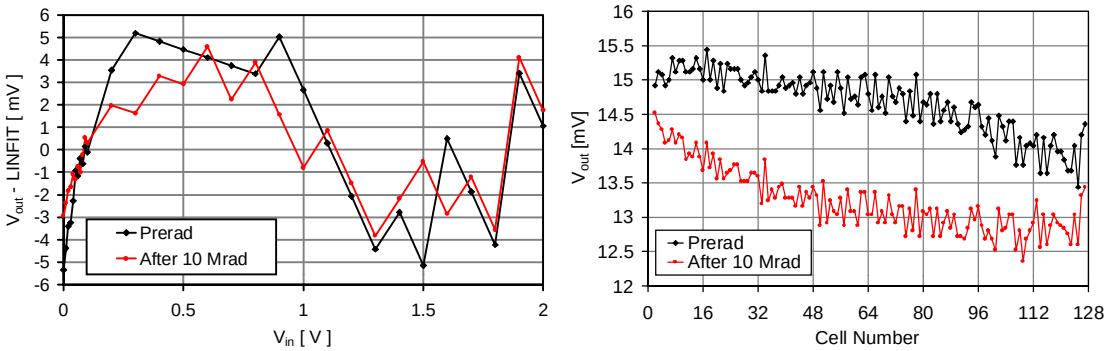


Figure 11 Left: *Deviation of the Input – Output characteristic from its linear fit, before and after irradiation.*
Right: *Pedestal variation from cell to cell for one channel of the memory before and after irradiation.*

3 Radiation Tolerant Digital Library

To facilitate the design of digital circuits of significant size and complexity a radiation tolerant digital standard cell library has been developed in the selected commercial 0.25µm technology. The library has been integrated into a complete design kit supporting the radiation-tolerant design method. Table 2 lists the digital standard cells that are available in the library. There are 30 core cells, 12 I/O pads and 6 power pads. The number of the library cells has been

Table 2 *List of the digital standard cells included in the Radiation Tolerant Library.*

CERN LIB Digital Standard Cells

Core Logic	Cell Name	Trans. count	Size (l m) 16x	Area (l m^2)
Boolean				
Inverter 1X Drive	E_Inv1	2	3	48
Inverter 2X Drive	E_Inv2	3	5	80
Inverter 4X Drive	E_Inv4	6	9	144
Inverter 8X Drive	E_Inv8	10	17	272
2 Input NAND	E_Nand2	4	7	112
3 Input NAND	E_Nand3	6	12	192
4 Input NAND	E_Nand4	8	14	224
2 Input NOR	E_Nor2	4	5	80
3 Input NOR	E_Nor3	6	11	176
4 Input NOR	E_Nor4	8	21	336
2 Input XNOR	E_Xnor2	12	18	288
Complex Gates				
2-Wide 2-Input AND-OR	E_AO22	10	16	256
2-Wide 2-Input AND-OR-INVERT	E_AOI22	8	13	208
2-Wide 2-Input OR-AND-INVERT	E_OAI22	8	12	192
Multiplexers				
2-Input MUX	E_Mux2	12	18	288
4-Input MUX	E_Mux4	28	40	640
Buffers				
Buffer X4 Drive	E_Buf4	8	11	176
Buffer X8 Drive	E_Buf8	16	26	416
Simple Cells				
Logic 0	LOGIC0	2	3	48
Logic 1	LOGIC1	2	3	48
Adders				
1-bit Half Adder	E_HAD1	18	27	432
1-bit Full Adder	E_FAD1	34	45	720
Flip Flops				
Static D FLIP-FLOP	E_dff	24	33	528
Static D FLIP-FLOP with Reset	E_dff_R	28	41	656
Static D FLIP-FLOP with Set	E_dff_S	28	41	656
Static D FLIP-FLOP with Set & Reset	E_dff_SR	32	47	752
Static D Flip Flop with Scan	E_dff_SR_SC	40	59	944
Dynamic TSPC D FLIP FLOP	E_TSPC	11	19	304
Latches				
D-Latch	E_LD	18	25	400
D-Latch with Reset	E_LDR	21	29	464

I/O Logic	Cell Name	Trans. count	Size (l m) 458x	Area (l m^2)
Output Pads				
8mA Drive Standard	OB8mA	16	115	51865
16mA Drive Standard	OB16mA	26	115	51865
20mA Drive Standard	OB20mA	34	115	51865
8mA Drive with Slew Rate control	OBSR8mA	14	115	51865
16mA Drive with Slew Rate control	OBSR16mA	30	115	51865
20mA Drive with Slew Rate control	OBSR20mA	38	115	51865
Input Pads				
CMOS Inverter Input	IB1	6	115	51865
Simple PAD	INPAD	0	115	51865
LVDS I/O Pads				
LVDS TX	LVDStx	33	235	105985
LVDS RX	LVDSrx	18	235	105985
I^{2}C interface I/O Pads				
20mA Open Drain Output	OD20mA	9	115	51865
Bidirectional with 20mA Open Drain	IOD20mA	17	115	51865
Power Pads				
VDD for periphery & core	VDD	0	115	51865
VDD for periphery	VDD_CORE	0	115	51865
VDD for core	VDD_PERI	0	115	51865
VSS for periphery & core	VSS	0	115	51865
VSS for periphery	VSS_CORE	0	115	51865
VSS for core	VSS_PERI	0	115	51865
Corner for I/O periphery	CORNER	0	115	51865
Guard-ring cells				
Endcap Cell Left	CAPL	0	115	51865
Endcap Cell Reft	CAPR	0	115	51865
Filler Cell	FILLERCELL	0	115	51865

kept to a minimum in order to facilitate fast technology updates.

Two circuit techniques were mainly used in the cells: complementary CMOS gates and pass-transistor logic. Neither of these requires static power consumption, and the pass transistors allow the implementation of complicated multiplexing gates and registers cells in a small area. A less common circuit technique is the dynamic circuit. It is used

for area efficiency and speed but it has been seen to be more sensitive to SEU introduced by energetic particles; thus it has been employed sparingly in the standard cell library. The True Single Phase Clock (TSPC) flip/flop is an example of a dynamic cell. Radiation tolerant layout techniques have been employed on the cell layouts to achieve total dose hardness levels consistent with the LHC environment. The use of the second layer metal for interconnection inside the cell was limited as much as possible and has been applied only in the more complex cells. The cell terminals are located at multiple locations (target pins) on the first and the second metal layers. These two layout techniques improve considerably the routing resources for the design.

A design kit that supports ASIC development on the CADENCE CAE platform has been developed. The kit offers analog and digital circuit design entry, analog simulations based on HSPICE, digital simulations based on VERILOG and mixed analog/digital simulations. To facilitate analog circuit design entry and simulation a number of analog primitive cells and parameterized cells have been prepared. These cells are listed in Table 3. The necessary database structures that enable mixed signal simulation have been created.

The standard cells have been characterized to enable simulations of digital circuits. The switching characteristics of the digital standard cells were determined via HSPICE simulations. The extensive use of scripts that automate the cell characterization and the generation of the timing information library file (TLF file) as well as the VERILOG simulation library files proved to be very beneficial in the cases of technology updates where the cells had to be re-characterized.

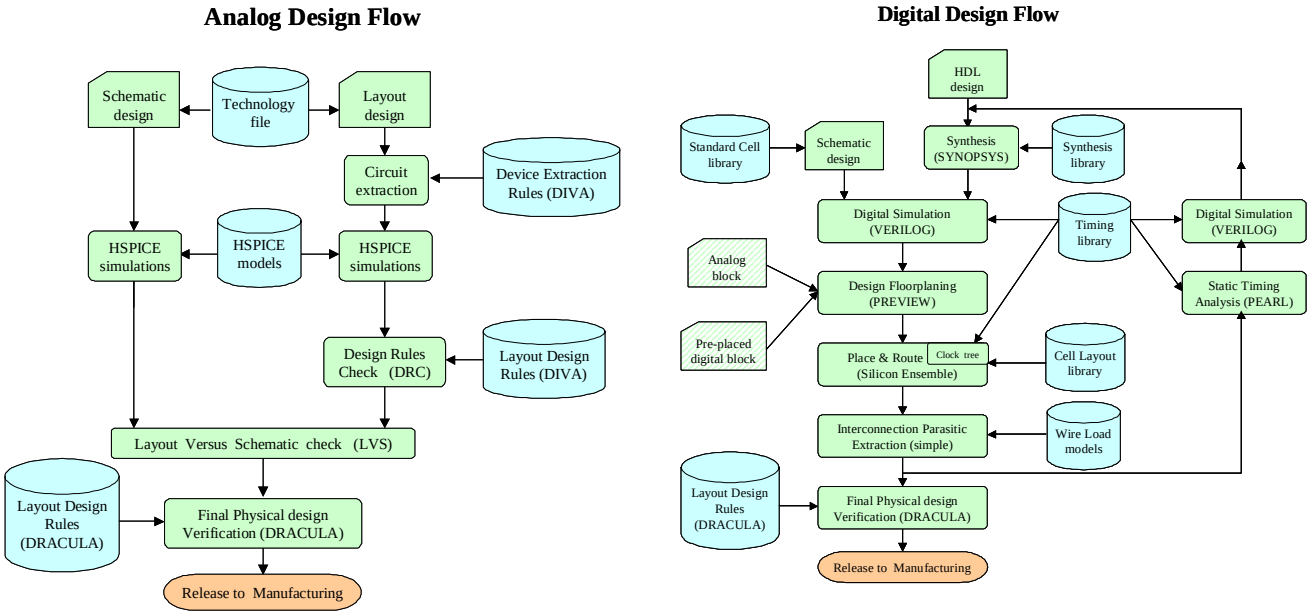


Figure 12 *Design flow for an analog circuit and a digital circuit*

The design kit also offers the capability of logic synthesis using the SYNOPSYS design compiler. For this purpose a library of synthesis timing information had to be created. Investigation showed that, the most suitable delay model to choose was the CMOS Non-linear Delay Model. This model uses lookup tables that can be directly mapped from simulation results, and interpolation to compute cell delays. This model is flexible enough to provide close timing correlation with a wide variety of submicron delay modelling schemes. It requires at least the measurement of the propagation delay (rise and fall cell delays) for several output loadings and several input slopes, and the same for the output slope (rise and fall transition delays). We have then 2-dimensional tables where the indexes are the output load (total output capacitance) and the input slope (input transition time). The output slope read in the table is then used for the cell delay calculation of the next stage logic. This model also uses scaling factors to model the effects of variations in process, temperature and voltage. We have used combined scaling factors (common) at the library-level for typical, worst and best case conditions.

The design kit also supports the use of the Silicon Ensemble Place-and-Route tool. This tool delivers advanced floor-planing and routing capabilities for building compact designs of high complexity. A set of special cells, called Guard-ring cells (Table 2), has been added in the standard cell library. The purpose of these cells is to close all the guard rings in the circuit layout for a radiation tolerant design and the Place-and-Route tool can automatically insert them. Library database preparation to support the use of this tool has also been done, involving the generation of a set of cell abstracts and a Library Exchange Format file (LEF file) containing the necessary cell layout information and technology-specific parameters. The LEF file has also been set up with Wire-Load-Model (WLM) information that

models the interconnection parasitics. Silicon Ensemble is capable of doing a simple extraction of interconnection parasitics of a routed digital design, thus enabling post layout simulations and static timing analysis to be performed.

The design kit offers two levels of physical design verification. The first one is based on the DIVA tool that is integrated in the CADENCE design framework and is used during the design process of a circuit. The second one is based on the DRACULA stand-alone tool and is used for final design verification of a complete chip. Design verification with special physical rules has been developed in order to check for inconsistencies in radiation-tolerant designs such as openings in guard-rings around n^+ diffusions.

Table 3 *List of the devices available in the Radiation Tolerant Library*

MOS devices	**Resistors**	**Capacitors**	**Parameterized cells**
PMOS	Polysilicon	Metal-metal	Standard layout NMOS
NMOS	N-diffusion	Poly-diffusion	Enclosed layout NMOS
Zero-Vt NMOS	N-well	Poly-N-well	Standard layout PMOS
		Metal-metal capacitor	Enclosed layout PMOS

The above-mentioned capabilities of the design kit are well integrated on the CADENCE CAE platform and are summarized graphically in Figure 12, which presents the design flows for an analog and for a digital design.

The functionality of the design kit has been tested in several digital and mixed analog/digital designs of variable sizes (400K to 1,2K standard cells). These designs were submitted for fabrication on a Multiple-Project-Wafer run and they all proved to be successful.

4 Pixel Readout Chip

After the successful design and testing of a small 130 channel prototype implemented in commercial 0.25 micron CMOS technology [4], the design of a full pixel readout chip was started for application in the ALICE pixel vertex detector and LHCb RICH.

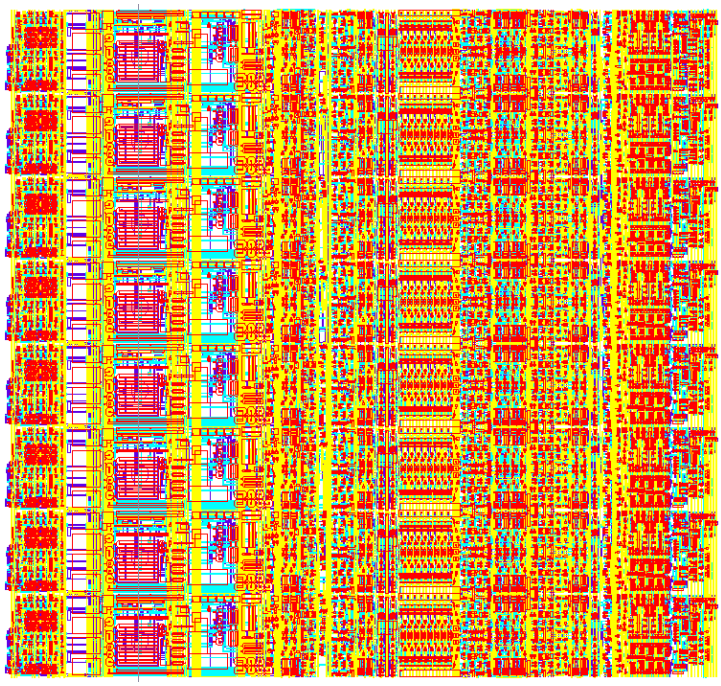


Figure 13 *Eight pixel cells of 50 x 425 μm containing 12000 transistors. The full chip will contain 8000 cells-13 million transistors.*

The design is now almost completed. The chip contains 8000 channels, each comprising an analog front-end (charge preamplifier, shaper filter and discriminator) and readout logic. The readout logic contains two synchronous delay lines providing a delay corresponding to the trigger latency.

Two are implemented to allow a new particle hit to be received within trigger latency (maximum 12 μs) after a first hit. For LHCb eight pixels of 50 by 425 square micron are grouped into one big pixel in which then the delay lines are grouped in a bank of 16 for reduced dead time. Each big pixel, shown in figure 13, measures 425 by 400 square micron, and contains more than 12000 transistors.

The periphery of the chip contains I/O, digital-to-analog converters for bias settings and slow control functions. The full chip will measure about 13.6 mm by 16 mm, and will contain about 13 million transistors. As for the small prototype the design is carried out systematically using edgeless NMOS transistors to provide radiation tolerance. The large die size put special constraints on the design, and required the use of six metal layers, which is the maximum offered in this commercial CMOS technology.

5 Radiation Tolerant Asics For Digital Optical Links

5.1 1.25 Gbit/s serializer for LHC data and trigger optical links

Several LHC detectors require high-speed (~ Gbit/s) digital optical links for transmission of data between the different sub-detectors and the data acquisition systems. Typically, high-speed data transmission is required for both the trigger systems' data path and the data readout systems. In general, those links will be uni-directional with the transmitters located inside the detectors and the receivers situated in the control rooms. In this arrangement, the transmitters will be subject to high radiation doses over the lifetime of the experiments. To address this problem, high-speed radiation hard transmitter ICs will have to be developed. During 1999 the feasibility of such an IC employing radiation tolerant layout practices in a mainstream sub-micron CMOS technology was assessed. A prototype that incorporates the most critical functions of a high-speed transmitter has been developed and tested. The IC includes: a serializer that transforms 10-bit parallel words into a 1.2Gbit/s serial bit stream, a clock multiplying PLL that generates the internal 1.2GHz clock from the 40.08MHz LHC clock and an high-speed 50 Ω driver that allows the chip to interface with most common optical transmitters. The prototype was conceived having in mind data transmission in trigger systems, thus allowing synchronous transmission of data at rates compatible with the LHC bunch-crossing frequency.

5.1.1 Serialiser Architecture

The block diagram of serializer ASIC is shown in figure 14. Its operation can be described as follows: an external 20-bit wide bus accepts parallel data at a rate of 60MWords/s. This data is time division multiplexed by the "Word Mux" into two 10-bit words which are then fed to the "10-bit Serializer" at a rate of 120MWords/s. Then, the serializer converts the 10-bit words into an 1.2Gbit/s serial stream. Finally, the data out of the serializer is passed to the "50 Ω Output Driver" that converts the internal CMOS levels into Pseudo-ECL (PECL) levels to allow interfacing the ASIC with commercial optical transmitters.

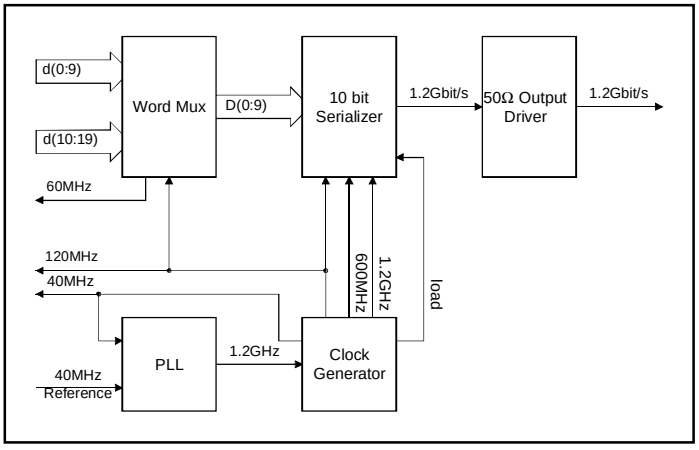


Figure 14 *Block diagram of the 1.25Gbit/s Serializer ASIC*

The operation requires several clocks and control signals at different frequencies. These are generated in the IC by the Phase-Locked-Loop (PLL) and the "Clock Generator" circuit. For operation at 1.2Gbit/s, the PLL takes as its reference the 40.08MHz LHC clock and compares it with its output signal divided by the "Clock Generator" by a factor of 30. In this way, a 1.2GHz clock is obtained at the PLL output. The "Clock Generator" provides the 60 and 120MHz clock signals required by the "Word Multiplexer", the 600MHz clock and the "load" signal needed by the high-speed serializer. A detailed description of the circuit and its operation can be found in [18] and it will not be repeated here.

5.1.2 Measurement And Test Set Up

A test-setup has been developed for the serializer ASIC. The block diagram of the transmitter side of the setup is depicted in figure 15. It consists of the serializer ASIC, an FPGA, a clock generator and an optical transmitter. To avoid the use of a special package to house the serializer – due to the high frequencies involved – the ASIC was directly bonded to the PCB.

The reference clock to the IC and the FPGA device can be provided either from an external source or from an on board 40MHz-clock generator. The ASIC interfaces with the optical transmitter through a 50Ω transmission line that can also be used to drive the serial signal out of the board for electrical measurements. The role of the FPGA device is threefold: it is used to program the serializer test configuration, it monitors the serializer's PLL locking state and it generates the test data patterns to be serialized. At the receiver end of the test-setup a commercial G-Link receiver is used to de-serialize the incoming data and to check for transmission errors.

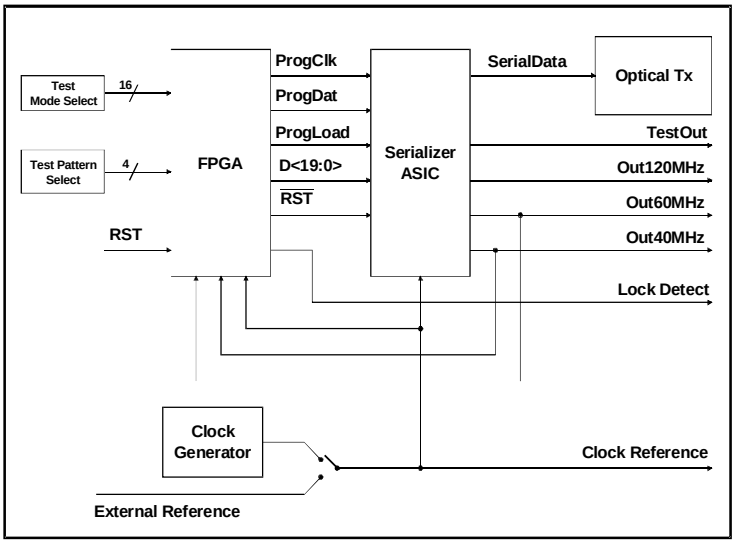


Figure 15 *Block diagram of the Serializer ASIC test-card.*

5.1.3 Experimental Results

An optical transmission test was made using the test-setup described previously. The test proved the ASIC prototypes to be fully operational at 1.2Gbit/s data rate. The data transmission test was done both before and after irradiation with X-rays. In both cases the data link was operated error-free for 72 hours. The irradiation was performed in a single step to a total dose of 10Mrad (SiO_2) at a dose rate of 11.7Krad (SiO_2)/min. The post-irradiation data transmission test was initiated one hour after irradiation and lasted for 72 hours. Jitter measurements were made before and straight after irradiation to evaluate any possible degradation of the analogue performance of the circuit. The jitter was measured with an HP infinium oscilloscope having a 1.5GHz analog bandwidth and a time resolution of 8Gs/s. The post-irradiation eye-diagram and its corresponding jitter histogram are shown in figure 16. The jitter values are 22ps RMS and 170ps P-P, and are essentially the numbers obtained for the pre-irradiation measurements.

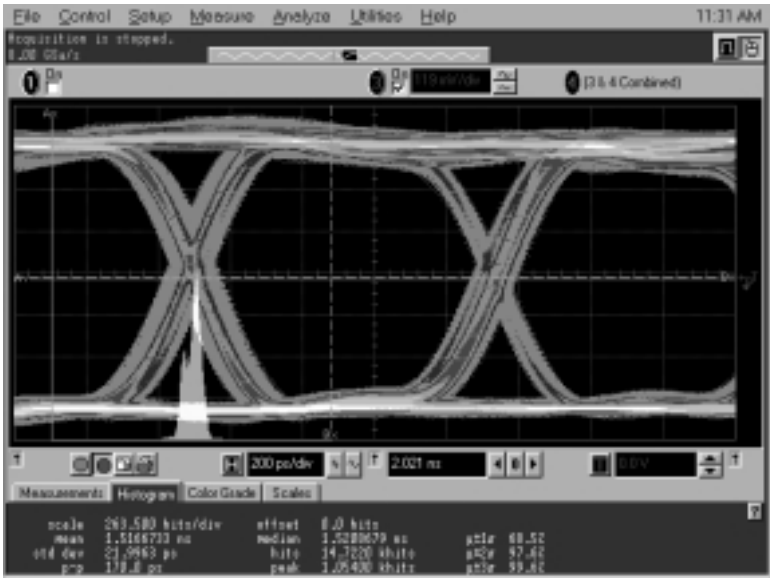


Figure 16 *Post-irradiation eye-diagram. Jitter: 22ps RMS and 170ps P-P*

The circuit sensitivity to Single Event Upsets (SEU) was studied by irradiating the IC with heavy ions while monitoring the transmitted data for errors. In this experiment it was verified that the main cause of transmission errors was loss of synchronization between the transmitter and the receiver. It is however, not clear what mechanism was causing synchronization loss and further tests and simulations have to be done to clarify this point. The measured cross-section for loss of synchronization is plotted in figure 17 as function of the Linear Energy Transfer (LET) of the ions. The observed threshold is about 7Mev cm^2/mg and the saturation cross-section is $4\ 10^{-5} cm^2$ (no errors were observed for LET = 6.2Mev cm^2/mg, fluence $9\ 10^6$). Using the measured data and extrapolating for different LHC environments, as proposed in [11], the error rates for such device can be estimated. This is done in table 4 where four different CMS environments are considered.

The numbers given in the table were calculated assuming a sensitive volume of 1 μm^3. In the technology used the thickness of the sensitive volume is probably smaller than 1 μm. The correct estimate for that thickness should be a factor of 2 to 4 higher than the one shown in Table 4 for the 1 μm^3 sensitive volume.

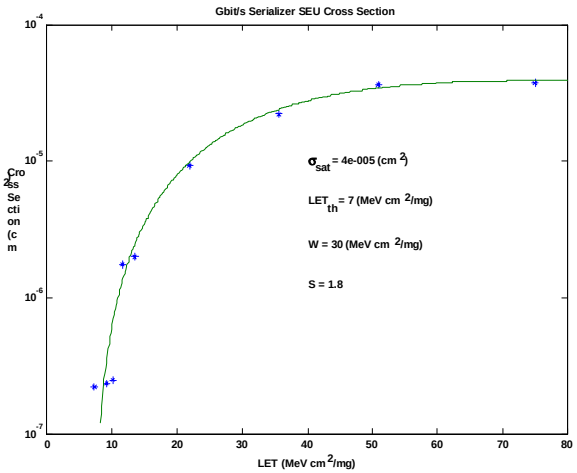


Figure 17 *Experimental SEUcross-section for the serializer*

It should be noticed that in the circuit no special precautions were taken against SEU. It is thus expected that the consequences for system operation of single event upsets can be minimized in the future if special circuit techniques are used to reduce the SEU sensitivity.
Additionally, system architectures should be used that will help to deal with any error induced by radiation. In particular, at the system level the receivers and the data acquisition systems should be able to react to error situations caused by momentary failure of the transmitter.

Table 4 *Error rates per chip per hour in for different CMS environments*

Environment	Pixel R = 4-20cm	Endcap ECAL R = 50-130cm	Outer Tracker R = 65-120cm	Expt. Cavern R = 700-1200cm
Errors/(chip hour)	$1.4\ 10^{-2}$	$1.9\ 10^{-4}$	$8.4\ 10^{-5}$	$3.1\ 10^{-8}$

5.2 Amplifier With AGC For The 80 Mbit/S Optical Receiver For The CMS Tracker

The CMS tracker control system will use approximately 1000 digital optical links for the transmission of timing, trigger and control signals. These digital signals, transmitted serially at a bit rate of 40 Mbit/s (80 Mbit/s for the clock signal), will be converted into electrical signals by a PIN photodiode at the receiver end. The front-end element of the optical receiver is a transimpedance amplifier, which has to amplify the photo-current delivered by the PIN diode. This amplifier has to be radiation-tolerant up to a total integrated dose of 10 Mrad, and its main specifications are reported in table 5:

5.2.1 Specifications And Circuit Architecture

As no commercial amplifier satisfying all these conditions exists, we have developed an ASIC in a commercial 0.25 µm CMOS technology using our radiation tolerant design approach (edgeless NMOS transistors and guardrings). The circuit architecture is shown in figure 18, and a complete description of the circuit design has been presented at the LEB workshop in Snowmass, and published in the proceedings [19]. Four amplifier channels are integrated in the chip.
The circuit performance has been measured by bonding its input to a Fermionics PIN photodiode, the diode type currently planned to be used in the digital optical link of CMS.

Table 5 *Circuit specifications*

DC input current [µA]	100
AC input current [µA]	10-500
Bandwidth [MHz]	80
Jitter [ns]	0.5
Output voltage level	LVDS
Supply voltage [V]	2.5
Sensitivity [dBm]	-30 prerad, -20 after rad
Bit error rate	10^{-12}
Reset output	high on missing clock
Coupling with p-i-n diode	DC
Diode bias voltage [V]	1.8

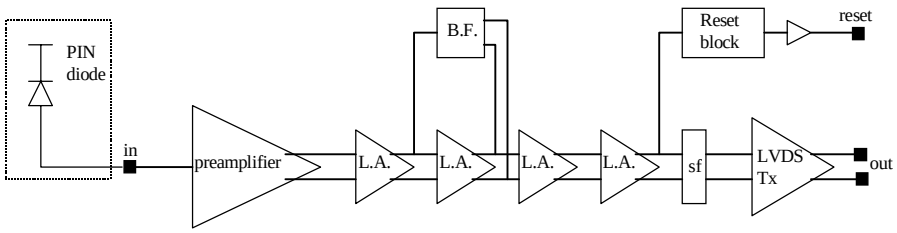


Figure 18 *Circuit architecture of the receiver chip.*

5.2.2 Measured Circuit Performance

Before irradiation, the circuit performance satisfies all the specifications, with a power consumption of about 122 mW. The LVDS output levels have been measured to be 1.24 V (low) and 1.52 V (high), and the amplifier bandwidth is about 110 MHz. The functionality of the AGC has been tested by changing the input signal amplitude over a wide range and producing an eye diagram. The minimum signal that could be resolved into a clear eye diagram without any error is about 1.25 µA. The amplifier continues to work properly up to an input signal of about 1.9 mA, the limit set by the measurement setup. Therefore, the AGC works correctly and allows the amplifier to cope with signals over a dynamic range of more than 30 dB.

To test the functionality of the leakage compensation feedback loop, we increased the DC input signal level to simulate the photodiode leakage current. The amplifier still performs well up to the specified 100 µA leakage current in presence of the smallest specified signal (10 µA). With such small signal, it was possible to increase the leakage up to 130 µA with unchanged performance. With higher signal, it was possible to increase the simulated leakage up to 200 µA without any noticeable performance penalty.

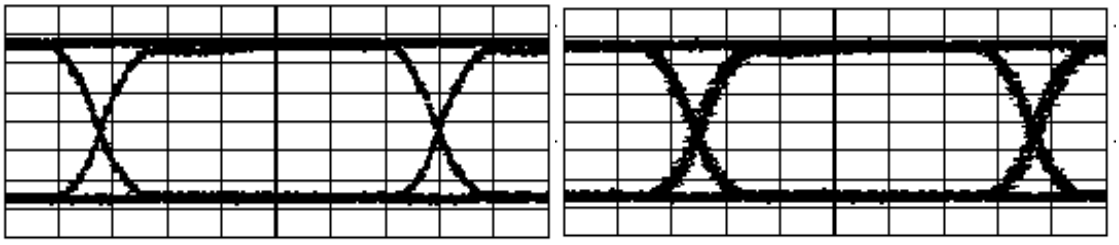
The jitter was measured in the worst case signal condition (10 µA signal and 100 µA leakage). The typical peak-to-peak (corresponding to 6 σ) jitter is about 0.3 to 0.5 ns. The power supply voltage was changed to 2 and 3 V, with the amplifier still operating well within specifications. We measured the channel-to-channel cross-talk on a chip where two channels were bonded to two PIN photodiodes and were operated simultaneously in different conditions (same signal frequency and amplitude but different phase, different signal amplitude and frequency). No performance degradation due to cross-talk was measured in any condition. The injection of a 20 to 40 mV peak-to-peak signal on the circuit power supply to simulate noise allowed the measure of the amplifier Power Supply Rejection Ratio (PSRR). The effect of the noise is an increase of the signal jitter for small levels of injected signal, but the eye diagram still stays wide open. From these results, we can safely conclude that the PSRR is sufficiently good for the circuit to operate correctly in the real application.

As required in the specifications, the reset signal goes high when the input signal is missing for more than about 2.45 µs, then goes low whenever the input signal starts again. The behavior of the reset is correct if the input signal is missing for a limited amount of time (the optimum is about 5 µs). Nevertheless, there is a problem when the signal is missing for a time longer than about 15 µs. In that case, in some circumstances the reset goes low and then starts to present random spikes. Therefore, the reset is not reliable for long periods of missing signals (which might occur in case of problems with the transmitter or in case of interruption of the optical line), and we decided to redesign it in the next circuit version.

5.2.3 Irradiation Results

The optical receiver has been irradiated with X-rays (10keV X-rays from the SEIFERT generator of the CERN microelectronics group) up to a total dose of 10 Mrad (SiO_2). The irradiation has been performed in one step at a dose rate of about 11.7 krad(SiO_2)/min. Measurements were performed about 2 hours after the end of the irradiation, then after one week annealing at 80°C.

a) *Before irradiation: signal ~ 500µA, no leakage:* *Before irradiation: signal ~ 10µA, leak ~ 130µA:*



b) *After 10Mrad: signal ~ 500µA, no leakage:* *After 10Mrad: signal ~ 10µA, leak ~ 130µA:*

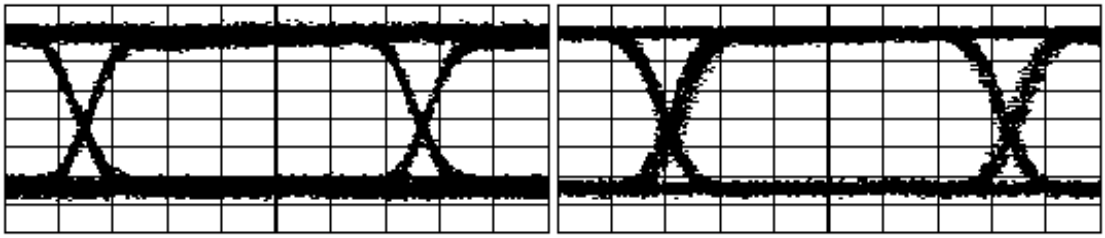


Figure 19 *Example eye diagrams for different levels of input signal and leakage current are shown before in a) and 2 hours after the irradiation up to 10 Mrad(SiO_2) in b).*

Immediately after irradiation, the chip still performs well within the specifications. The current consumption increases by about 6% to 51.8 mA, and consequently the LVDS levels lower to 1.18 V (low) and 1.48 V (high). The bandwidth decreases to about 85 MHz. Also the sensitivity slightly decreases, the minimum input signal for a clean eye diagram with no errors being about 1.9 µA. The jitter is slightly increased to about 0.6 to 0.8 ns (peak-peak value). All the other performance parameters were unchanged.
The annealing took place at 80°C for one week under DC bias (2.5 V). The annealing temperature was limited below the normally used 100°C to avoid damaging the plastic package of the photodiode. The chip almost recovered the pre-irradiation performance in terms of speed and noise. After annealing, the current consumption is about 51 mA, and the LVDS levels are 1.19 V (low) and 1.49 V (high). The bandwidth is about 100 MHz. The sensitivity improves with annealing, the minimum input signal for a clean eye diagram with no errors being equal to the pre-rad value. The jitter does not show recovery after annealing, its peak-to-peak value (corresponding to 6 σ) being about 0.6 to 0.8 ns, as immediately after irradiation.
These results show that the optical receiver can stand a total dose of 10Mrad without any important change in its performance, which is constantly well within specification.
Example eye diagrams for different levels of input signal and leakage current are shown in Figure 19 before and 2 hours after the irradiation up to 10 Mrad(SiO_2).

6 Single Event Upset Measurements In Deep Sub Micron Circuits

6.1 Test Structures

We have used two types of test structures in a commercial 0.25 µm CMOS process to validate our SEU measurements. In addition to a dual-ported static RAM, a circuit which is representative of the real application, a set of shift registers has been implemented to evaluate the SEU sensitivity of basic building blocks used in ASICs design. All the designs used the radiation-tolerant layout practices and aimed at hardening the circuits to total dose effects. Therefore, all NMOS transistors were designed with special geometries, and guardrings were extensively used across the circuit. A detailed description of the test structures and of the measurement results has been included in the proceedings of the LEB workshop held in Snowmass [20].

6.2 Measurement Results

SEU measurements took place at the ESA-UCL line of the "Cyclone" cyclotron of Louvain-la-Neuve, Belgium, with both heavy ion and proton beams.
The memory circuit was irradiated while powered at V_{dd}=2.5 V with heavy ions up to an effective LET of about 32 MeVcm^{2}mg^{-1}. The explored LET region is the most significant for our aims. In fact, to predict the upset rate for a circuit in LHC, we need to have good Weibull fit parameters in the LET region representative of the fragments produced by nuclear interaction of hadrons in silicon. The LET of such fragments does not exceed 15 MeVcm^{2}mg^{-1}. The cross-section curve measured for the memory chip is shown in Figure 20, where the solid line represents the Weibull curve fitting the experimental points.

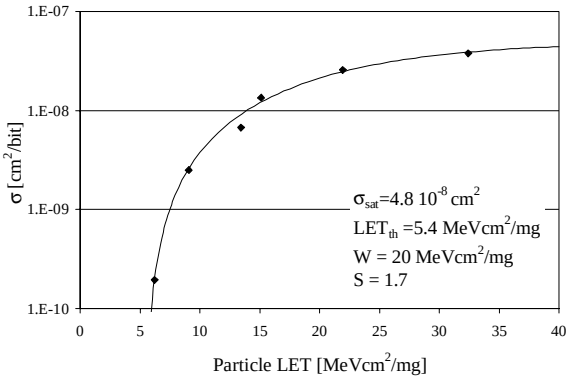


Figure 20: *Cross-section curve for the memory circuit irradiated with heavy ions. The measured points are fitted with a Weibull function (solid line), and the fitting parameters are reported.*

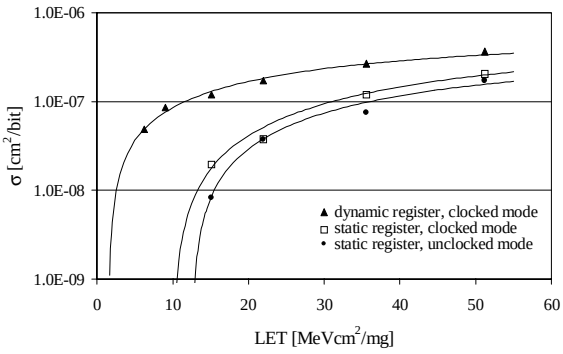


Figure 21: *Measured cross-section for dynamic and static shift registers with a heavy ion beam. Experimental data are fitted with a Weibull curve in all cases. The frequency of the clocked test was 30 MHz.*

With the Weibull parameters, and using the method described in [11], we can estimate the upset rate this memory chip would experience in different points of the CMS experiment. The method is based on an extensive simulation work, and

we will use it with the hypothesis of a cubic Sensitive Volume (SV) of 1x1x1 μm^3. From the calculations, one can see that the upset rate is always dominated by hadrons (including neutrons) of energy above 20 MeV. The highest total (> 20 MeV hadrons + 2-20 MeV neutrons) upset rate of $2 \cdot 10^{-4}$ is found in the pixel detector. If we assume that LHC will run for $5 \cdot 10^7$ seconds in the foreseen 10 years of its operation, the memory chip will experience a total of about 10000 upsets. In the outer tracker the estimated total number of upsets falls to about 105, behind the endcap of ECAL it is 330, and no upset are expected for this memory in the experimental cavern.
The shift register circuits have been irradiated with heavy ions and protons in both the "unclocked" and the "clocked" operation mode. The cross-section curves measured with a heavy ion beam are shown in Figure 21 for the dynamic shift register (clocked mode) and for the standard static shift register (clocked and unclocked mode). Two important tendencies can be noticed in Figure 21. The most striking is the much higher sensitivity of the dynamic shift register if compared with the static one. Additionally, the static shift register is more robust to SEU when it operates in the unclocked mode.

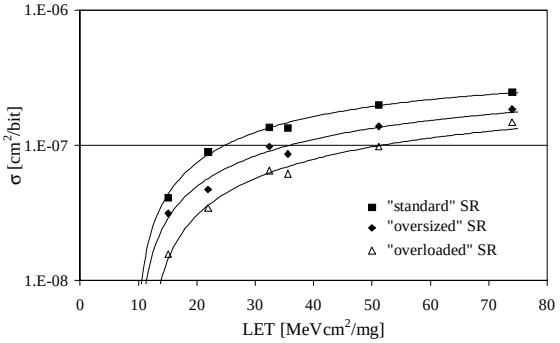


Figure 22: *Measured cross-section for the different static DFFs irradiated with heavy ions in the clocked mode.*

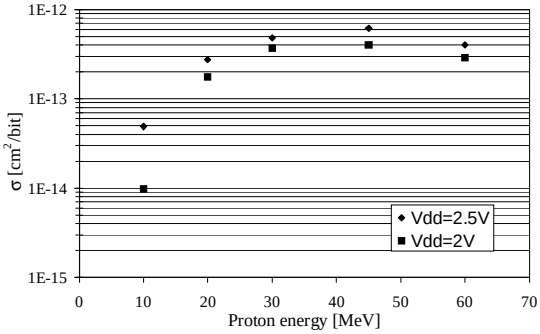


Figure 23: *Measured cross-section for the dynamic shift register irradiated with a proton beam at different power supply voltages in the clocked mode.*

To verify whether the two modified versions of the static DFF cell, the "oversized" and the "overloaded" cells, have an improved SEU cross-section over the standard cell, we have irradiated them with heavy ions. The resulting cross-sections are reported in Figure 22, where they are compared with the behaviour of a standard static cell integrated in the same test chip. This figure refers to the clocked mode, at a frequency of 30 MHz. The modified cells are less sensitive to SEU than the standard DFF, with the "overloaded" solution being the most effective. This cell pays a penalty in terms of speed and power consumption, but it still easily complies with most of the applications in ASICs for LHC, where a speed of 40 MHz is a standard requirement. The use of the Weibull fit parameters to estimate the upset rate for these cells in LHC reveals that the upset rate for the "oversized" DFF is almost a factor of 2 lower than for the standard DFF, this factor increasing to 10 for the "overloaded" cell.
The standard static and the dynamic shift registers have also been irradiated with protons. During the irradiation at 2.5 V, no upset was observed for the static register, indicating an upset cross-section below $6 \cdot 10^{-15}$ cm^2/bit for 60 MeV protons. From the heavy ion irradiation, we estimated for that proton energy a cross-section of about $3 \cdot 10^{-16}$ cm^2/bit. For the dynamic cell, we observed as expected a considerably higher upset cross-section, as shown in **Figure 23**.
All the SEU measurements have confirmed that circuits designed in the quarter micron technology using the radiation tolerant design approach present an upset rate considerably lower than what would be expected for normal designs in such technology. This characteristic is due to the use of enclosed geometry transistors, which do not allow the use of minimum size transistors. As a consequence, the node capacitance is higher and the transistor current drive is also higher, and the SEU sensitivity decreases. The use of guard-rings, which is typical of our design approach, is also very effective in increasing the resistance against Single Event Latch-up. In our experiments, no SEL was ever observed up to the maximum LET of the heavy ions used that was sometimes higher than 100 MeVcm2/mg.

7 Estimate of the SEU Rate in LHC

As reported in the previous status report, an activity was started in 1998 to evaluate the risk associated to Single Event Upset (SEU) in the LHC radiation environment. This work has been done in strict collaboration with CMS, therefore it is focused on the CMS radiation environment; the results can nevertheless be easily extrapolated to ATLAS and to the other radiation environments in LHC.
In 1998, we developed the simulation procedure based on the use of the FLUKA simulation package [21] for the simulation of the nuclear interactions, and on TRIM [22] to compute the energy loss of the fragments produced by the interaction. Actually, the TRIM code has been modified to be more compatible with our application and to be able to treat a full atomic cascade. In 1999, the procedure has been completed to deal also with low-energy (below 20MeV)

neutrons. In this domain, reactions are generated directly from the information contained in the ENDFB-VI cross-section tabulations without any involvement of the FLUKA code. Moreover, the whole computational method to estimate the SEU rate has been improved by the use of the measured heavy ion cross-section to obtain the required information on the Sensitive Volume (SV) size and on the critical energy. Such information is necessary to correctly compute the error rate in any environment.
The confidence in this computational method has been well established by the comparison of its results with experimental benchmarks. A set of devices for which both heavy ion and proton beam measurements were available has been identified. For such devices, we could estimate the measured proton SEU cross-section within a factor of 2 using the heavy ion data as an input to our computational method.
The developed simulation approach has been extensively documented in a paper submitted for publication [11], which also applies the method to estimate the error rates in several positions in the CMS experiment. One of the most important outcomes of the paper is that all over the detector the SEU rate will be dominated by high energy (higher than 20MeV) hadrons. The only possible exception is for the outer regions of the detector, where for some particular components an important contribution might come from thermal neutrons. This possibility seems nevertheless quite unlikely, as it would require at the same time high boron doping and very low threshold energy for the device. In an example case of a typical DRAM circuit with a quite low threshold energy, thermal neutrons do not significantly contribute to the estimate error rate in any part of CMS, whilst 2-20MeV neutrons only contribute to about 10% of the total SEUs.
Based on these results, we propose a simplified method for generic testing of ICs intended to be used in the LHC radiation environment [15]. A suitable test procedure would be to use a 60-200MeV proton beam to irradiate the devices, as this should provide a reasonable estimate of the SEU rate in most locations around the LHC. Only for inner trackers this might be too optimistic and a dedicated test in a pion beam of about 200MeV would be closer to reality.

8 Development Of The Radiation Hardened Voltage Regulator

In 1998, the radiation-tolerant power bipolar technology proposed by ST Microelectronics was found sufficiently radiation hard to launch the development of a positive hardened voltage regulator. The first prototype was manufactured in February 1999. Unfortunately, it turned out that the prototype suffers from design bugs preventing a normal functioning. This problem was caused by the inaccuracy of the simulation models used. It was the first time that a high-speed bipolar technology was used to design a power device, necessary for the hardening against displacement damage, and some inconsistencies in the modeling were found.
ST Microelectronics then took quickly the decision to modify 3 mask levels to partly correct the faulty prototype in order to resubmit very quickly a new production for the evaluation of the radiation hardness.

8.1 Electrical Characterization Of The Voltage Regulator Before Irradiation

The performance of this modified prototype did not totally conform to specification, but the functionality was sufficient to assess the level of radiation hardness. In July 1999 the modified prototypes were delivered to CERN for evaluation. The 6 “ wafers received contained 5 versions as shown in figure 24.

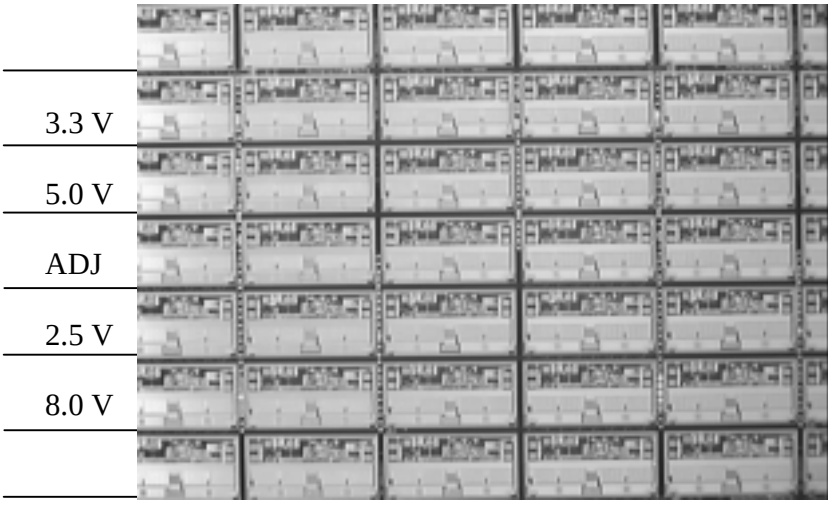


Figure 24 *Magnification of an area of the Voltage Regulator wafer. The 5 different versions of stacked vertically. In the scribe line region ares placed test structures for technology and hardness characterisation .*

These versions were for 2.5V, 3.3V, 5V, 8V and an adjustable version (from 1.25V to 8V).
Several samples of the 2.5V, 8 V and adjustable version have been tested in load and line regulation, and results have been reported at the LEB workshop in Snowmass [16]. The overall functional characteristics of the regulator were found to be correct, except for the following problems caused by inadequate models for the breakdown voltage of the base-emitter junction:

- The reverse breakdown voltage of base-emitter transistor at 6V in the control circuit prevents voltage drop operation between IN and OUT larger than 6.5 Volt. This will be corrected in the final prototype by a design change.
- The Over-current signal was unstable, the problem was also caused by the breakdown voltage of emitter-base.
- Dropout voltage was 0.7V/A and not 0.5V/A as specified. This was caused by the inaccuracy of the modeling of power transistor in high-speed bipolar technology.

The line regulation and load regulation have been characterized and are shown in figure 25, which gives the typical load characteristic of the regulator with a current limited to 3.5 A.
Preliminary measurements of the output noise and ripple rejection have been done. Output voltage noise, which is an important parameter for Front-end electronics of calorimeters and trackers, is about 100 µV to 400 µV rms in the frequency range of 50 Hz to 10 Mhz. Ripple rejection is about 60 dB in the range of 50Hz to 1 Mhz. Statistical measurements of the output voltage have been performed on the 2.5V and 8V version of the voltage regulator by probing die on wafer. Results indicate a spread of the output voltage of about 0.7% rms, which is within specification of 2%.

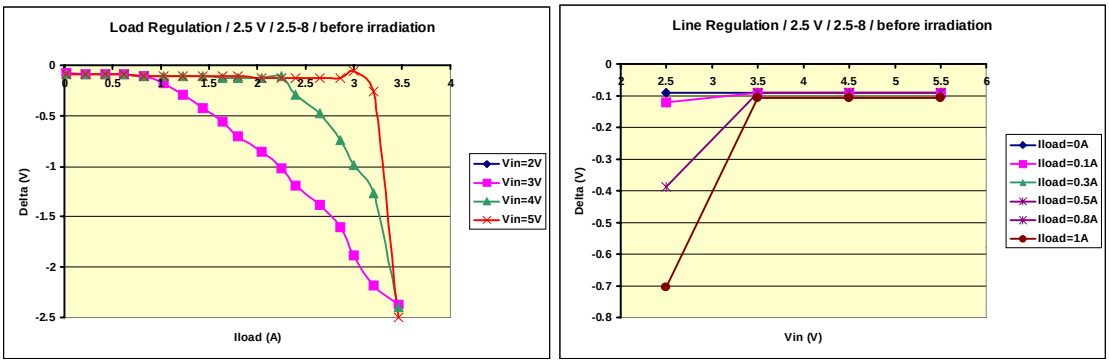


Figure 25 *Typical load regulation (left), line regulation (right). The maximum current is limited by internal over-current control set at 3.5 A. Minimum dropout voltage is 0.7V/A.*

8.2 Radiation Test of the Voltage Regulator

Several radiation tests have been performed on the voltage regulator prototype to evaluate the radiation resistance to total dose and displacement damage. Table 6 shows the different radiation tests performed. Results indicate that the voltage regulator radiation tolerance far exceeds the specification established for the LHC application, 2.10^{13}

Table 6 *Radiation tests performed on the voltage regulator with Co60, X-rays and at the CERN PS in the IRRAD1-2 facilities.*

Irradiation	Dose/Fluence	Date	Place	Chips
Co60	1.3Mrad	Aug-99		ADJ
X-Rays	3.9Mrad	Jul-99	CERN-MIC	2.5
Proton	$1*10^{13}$ p/cm^2	Jul-99	CERN PS East Hall	2.5, ADJ
	$5*10^{13}$ p/cm^2	Aug-99	CERN PS East Hall	8.0, ADJ
	$3*10^{14}$ p/cm^2	Nov-99	CERN PS East Hall	2.5
Neutron	$1*10^{13}$ p/cm^2	Jul-99	CERN PS East Hall	2.5, ADJ
	$8.5*10^{13}$ p/cm^2	Nov-99	CERN PS East Hall	2.5, wafer

neutrons/cm^2 and 500 krad.

In figure 26 (right) is shown the typical radiation response of the 2.5V Voltage Regulator in the proton flux of IRRAD1 up to 1.7 10^{14} protons/cm^2. Further test have shown that the device starts to be severely damaged above 2.10^{14} protons/cm^2, its failure mode being a decrease of the output voltage from 2.5V to 0V. An additional radiation test with neutrons has been performed on an entire 6 " wafer. The result of the measurement performed on 50 die probed on-

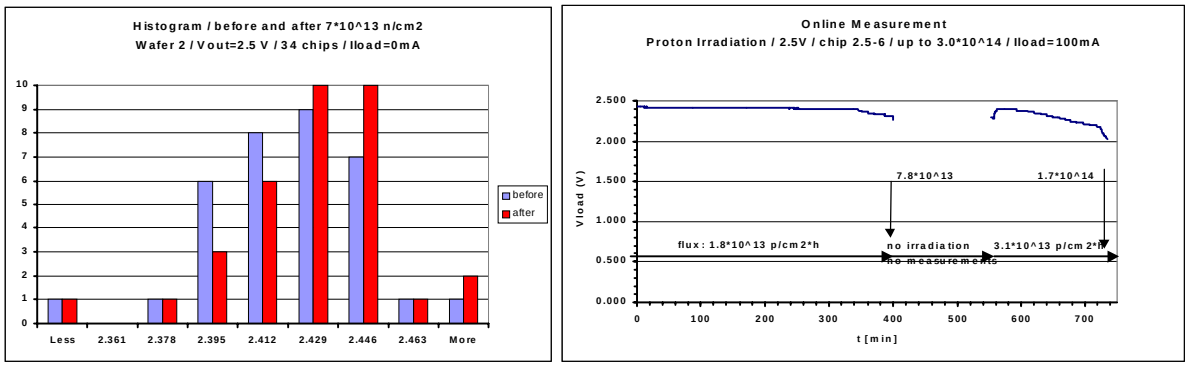


Figure 26 –Left:- *Statistical measurement of the output voltage before (light shading) and after 7 10^{13}neutrons/cm^2.*
Right- *Evolution of the output voltage of a 2.5V voltage regulator exposed to a proton fluence up to 1.7 10^{14} cm^{-2}, the gap in the measurement corresponds to a beam off- time period.*

wafer (2.5 V and 8 V versions) have shown an almost insignificant increase of the the ouput voltage as can be seen in figure 26 (left).
Single effect Latch-up tests have been performed on the 2.5 V and 8.0 V voltage regulators at the Cyclotron CYCLONE with protons (65 MeV) and Heavy Ion (ions: Argon, Krypton). As expected, no latch-up was detected up to a fluence of 3 10^{11} /cm^2 for protons and up to a fluence of 10^6 /cm^2 for ions.

8.3 Negative Voltage Regulator

Following the successful result of the first prototype of the positive voltage regulator, several LHC users have requested the development of a negative version. This has been agreed by STM, and a contract for the development has been placed. Specification of this negative version is the mirrored specification of the positive version, except for the over-current signal and the inhibit control for which the levels have been kept positive. Thus, the regulator control and regulator monitoring can be performed in common with the positive regulator, making easier the implementation of the power supply at board and system level.

9 Radiation Induced Leakage Current In Ultra-Thin Gate Oxide

The objective of this study was to investigate the risk of radiation induced gate leakage and gate breakdown in deep sub micron CMOS technologies.

9.1 Introduction

In modern CMOS 0.25µm technologies, the MOS gate oxide (thickness ≤ 5 nm), shows a low field Radiation Induced Leakage Current (RILC) after irradiation [23,24]. RILC is usually attributed to a trap assisted tunneling (TAT) of electrons through neutral oxide traps generated by radiation stress. Studies of Single Event Gate Rupture (SEGR) of thin gate oxides upon irradiation with heavy ions show a non-catastrophic Soft Breakdown (SB) [25]. After a SB the device shows a higher leakage current than in the case of RILC.
Irradiation experiments were performed on square MOS capacitors with oxide thickness t_{ox}=4 nm and gate area 10^{-2} cm^2. We used four different sources: 8 MeV electron beam, 158 MeV Si ion beam, 213 MeV Ni ion beam and 257 MeV Ag ion beam. Ig-Vg measurements were performed before and after irradiation.

9.2 Results

9.2.1 Leakage Current After Irradiation

In figure 27 is plotted the positive I_g-V_g curves of 4-nm oxide capacitors before and after irradiation with different sources, the low field gate current increases between V_g=-1.5 V and V_g=-5 V. During irradiation capacitors were biased at flat band ($E_{ox,bias}$ = 0), corresponding to $V_{g,bias}$=-1.1 V. The oxide charge trapping after irradiation is negligible and the flat-band voltage shift is less than 10 mV.

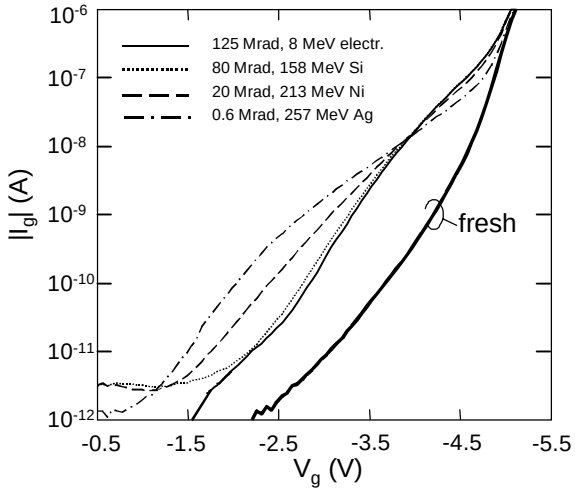


Figure 27 *Negative Ig-Vg curves measured before and after irradiation with four different radiation sources.*

Despite the largely different LET values, the gate excess current shows the same functional dependence on the gate voltage in the two cases (electrons and Si ions), and it can be described in terms of the RILC conduction mechanism. Hence, this current is associated to a TAT via a single neutral oxide defect, even for Si ion irradiated devices. This means that the density of defects generated even in the dense Si ion track is not high enough to permit the onset of a conductive path involving several neighboring defects.

In figure 27, the excess current produced by Ni and mainly Ag ions exhibits a different shape which cannot be attributed to RILC. This current derives from the onset of Radiation induced Soft Breakdown (RSB) conductive paths across the oxide. Curves obtained after Ag ion irradiation are well fitted by:

$$I_e = a \cdot V_g^{\,b} \qquad (1)$$

where I_e is the excess gate current, V_g is the gate voltage, and a and b are two parameters which are empirically correlated as:

$$b = -0.78 \cdot \log(a) - 3.27 \qquad (2)$$

The corresponding values of the parameters $a = 2.10^{-14}$ and b = 7.3 follow eq. 2, confirming the SB nature of the radiation induced current. This parameter choice gives a nice fit of both negative and positive I_g-V_g characteristics. On the other hand, the excess current obtained after Ni irradiation is not dominated by RILC (as for low LET particles) or by RSB (as for Ag irradiation), but both conduction mechanisms seemingly give similar current contributions, which cannot be easily separated.

9.2.2 Leakage Current Dependence On Bias During Irradiation And LET

The RSB dependence on oxide field is illustrated in figure 28-*left*. All currents were read at $|E_{ox}|$=6 MV/cm (V_g=+3.5V and V_g=-4.18 V), but similar results are found in a large voltage range (for instance, from Vg=-1.5V to Vg=-4.9V for the Ag irradiated device). After Ag irradiation, RSB is minimum at zero bias, while positive RSB is always lower than negative RSB. Hence, the bias applied during irradiation enhances the generation of RSB paths even in case of small oxide fields (3 MV/cm). The occurrence of RSB even at zero bias may derive from the accumulation of local oxide damage due to the overlap of different ion tracks, which can be expected due to the high ion fluences used in our tests. No data have been collected for irradiation with low fluences, where track overlap does not take place. The minimum Ag fluence used in our experiments was $7 \cdot 10^8$ cm^{-2}, and RSB was already active.

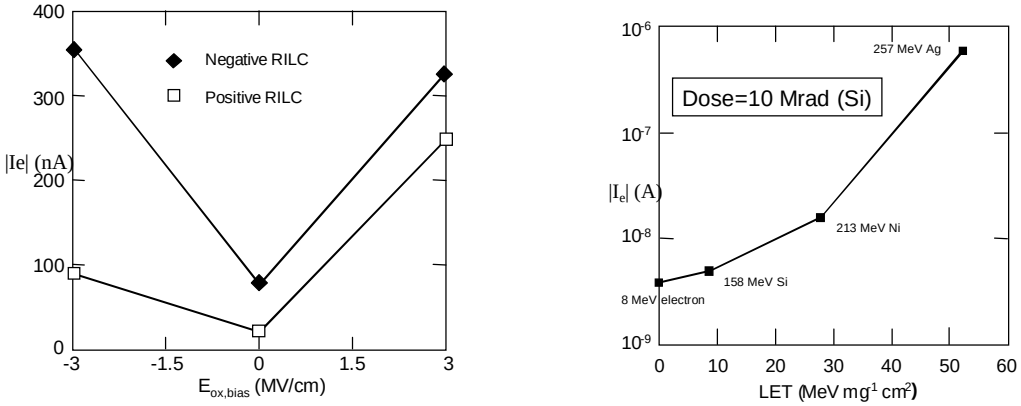


Figure 28 Left:*-RSB versus the oxide field ($E_{ox,bias}$) applied during a 1.6 Mrad (Si) irradiation with 256 MeV Ag.*
Right- *RILC/RSB versus the LET. All devices have received 10 Mrad and have been biased at flat band gate voltage ($E_{ox,bias}$=0).*

In figure 28-*right* we have plotted the excess current (read at Eox=6 MV/cm) as a function of LET for four different radiation sources after 10 Mrad(Si). The large LET difference between electrons and Si ions produces no large variation of the excess current. Only when the RSB conduction is activated, a substantial increase of the leakage current (up to two orders of magnitude) is observed. While RILC seems to be not sensitive to LET variation, RSB appears only for high LET values, indicating again that a large density of e-h pairs are needed to produce conductive paths through several defects across the oxide. This result indicates that the LET threshold for the onset of RSB in our 4-nm oxides is around 20 $MeV \cdot mg^{-1} \cdot cm^2$.

9.2.3 Kinetics of RILC

In figure 29 is shown the positive RILC versus the cumulative total dose for electron or Si beam irradiation. RILC data can always be well fitted by:

$$I_e = K_R \cdot Dose^{\beta} \qquad (3)$$

β ranges between 0.75 and 1, while K_R is a constant depending from the read-out gate voltage. β(Si) is always close to 1, indicating that the amount of neutral oxide defects linearly grows with the radiation dose. β(electrons) is always smaller than β(Si) and varies with the oxide field.
Similarities of RILC accumulation kinetics between Si ions and electrons could sound quite unexpected, as RILC has been attributed to holes surviving prompt recombination, which should be a very modest fraction of those generated by the incident ion. Instead, we see that the amount of defects assisting RILC is even (slightly) higher for ion than for electron irradiation. These results suggest a rethinking of the *e-h* recombination processes in ultra-thin oxides. Apparently, much more holes survive in the columnar regime than expected.

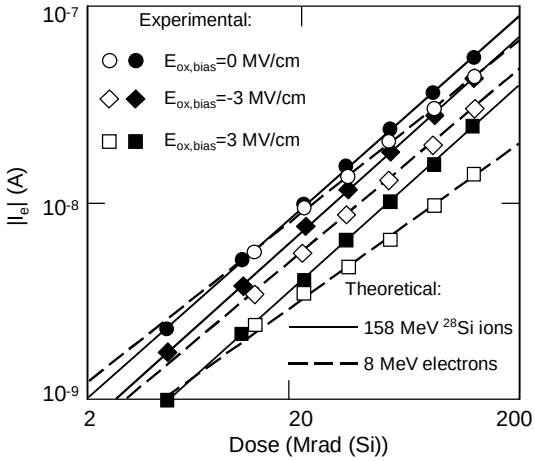


Figure 29 *Positive RILC read at E_{ox}=6 MV/cm versus the cumulative dose after electron or ion beam irradiation for different gate voltages during irradiation. Fitting curves are obtained from eq. (3).*

9.2.4 Risk Of Radiation Induced Gate Damage

Previous experimental results show that gate leakage and soft burnout induced by radiation are possible in LHC environment. However, those types of radiation effects are not very harmful, and do not result in catastrophic failures. Hard burnout like Single Event Gate Rupture is unlikely to occur in LHC environment. This effect seems to occur only for heavy ions of very large LET on electrically stressed gates, which is not a normal operating condition for integrated circuits in LHC electronics.

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