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2nd RD49 Status Report
Study of the Radiation Tolerance of ICs for LHC

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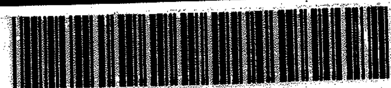

Executive Summary

The RD49 project was approved in March 1997 with the objectives of assessing radiation tolerant design and layout techniques applicable to commercial sub-micron technologies, and establishing collaboration with radiation effects specialists from the Space agencies. The selection, qualification and procurement of Commercial-Off-The-Shelf (COTS) components in a radiation environment is a field where the Space agencies have valuable experience and have developed solutions which could be adapted to the needs of the LHC experiments.

Radiation effects in ICs can be divided into three classes:

- **Total Ionizing Dose (TID) effects**: Total dose effects are caused by the trapping of radiation-induced holes in the insulating oxide layers and by the formation of "interface states" (charge traps that accumulate at the oxide-silicon boundary and modify the electrical properties of the channel of the MOS transistor). TID effects include threshold voltage shifts, leakage currents, and degradation of the carrier mobility (speed), gain and noise performance.
- **Displacement damage**: Damage to the crystal lattice caused by protons and neutrons, resulting in the degradation of the performance of bipolar transistors and optoelectronic devices (optocouplers, LEDs, etc.).
- **Single Event Effects (SEE)**: Single-event effects are caused by the local deposition of charge by a single particle strike; the deposited charge may result in a number of different effects. The two most important single-event effects in the CMOS technology are Single-Event Upset (SEU) and Single-Event Latch-up (SEL). SEU may appear as a temporary malfunction (glitch) of a circuit, or it may flip the state of a memory element. In SEL the deposited charge turns on a parasitic circuit that conducts current from the supply to ground; it can only be turned off by powering off the circuit. SEL may destroy the IC.

The radiation tolerant approach pursued by RD49 relies on the fact that holes trapped in the thin gate oxides employed in submicron MOS technologies can be neutralized by tunneling electrons. The approach uses quarter micron CMOS technologies with gate oxide thickness below 6nm, so that the tunneling mechanism is fully effective. In addition, the NMOS transistor layout is made edgeless (by using an enclosed geometry instead of the traditional linear geometry). The edgeless transistor eliminates the radiation-induced leakage paths caused by holes trapped in the "bird's beak" (the zone at the edge of the non-enclosed transistor in which the thin oxide of the gate joins to the thick field oxide). The third feature of the radiation tolerant design approach is the isolation of devices by cutting leakage paths between devices under the thick field oxide; this is achieved by surrounding NMOS transistors with guard rings. The use of guard rings also helps to protect against Single Event Latch-up.

The following milestones were set for 1998:

- The detailed study of total dose and single-event radiation effects in quarter micron CMOS processes.
- The completion of the assessment of the radiation tolerant design practice based on the development of demonstrator circuits in a quarter micron CMOS process
- The transfer of the radiation tolerant design know-how to LHC design teams.
- The understanding of the LHC needs in Commercial-Off-The-Shelf (COTS) components for LHC experiments

In 1998, six new institutes joined the RD49 collaboration: the Fermi National Accelerator Lab, the University of Montreal, the Institute of Physics in Prague, the University of Rome II, the Brunel University of London and the TIMA lab of Grenoble. The main technical study of the collaboration has been the detailed evaluation of the radiation tolerance of quarter micron CMOS technologies, and the demonstration of the feasibility of designing digital and mixed-signal VLSI circuits with the proposed radiation tolerant practices. The approach has attracted considerable interest in many physics institutes and a number of radiation tolerant developments for specific LHC detectors are now underway or being started. A call for tender for the provision of foundry services in a suitable quarter micron technology has been carried out and a design kit supporting the radiation tolerant methodology is being developed. A radiation tolerant standard cell library is also being developed.

In 1998 two RD49 collaboration meetings were held at CERN in which experts from American and European Space Agencies and companies interacted with representatives of the LHC experiments. As a result, the LHC community has become aware of the importance of the following SEE issues:

- **The risk of Single Event Upset** (SEU) induced by high-energy particles, protons and neutrons above an energy of 10 MeV has been recognized. Preliminary results obtained by the ATLAS LArg group on their G-link readout data link showed an unexpected sensitivity to neutron-induced SEU. Measurements made by the space and avionics industry on the correlation between the fluence of atmospheric neutrons and the occurrence of SEU in memory chips confirm this sensitivity. This SEU risk potentially exists for other COTS components used in the calorimeters, muon detectors, and in-cavern electronics where the neutron flux represents the dominant contribution of the radiation environment. Moreover, it has been noticed that low energy neutrons (<1 eV) could also induce upsets in SRAM chips. The $^{10}B(n,\alpha)$ ^{7}Li reaction, for which the cross-section increases exponentially with the decrease of the neutron energy seems to be responsible for the upset induced by low energy neutrons.
- **The risk of Single Event Latch-up** (SEL) has been demonstrated on a standard ASIC developed in a 1.2μm CMOS process for the readout of the silicon strip Tracker of ALICE. The measured threshold LET of 8 $MeVcm^2mg^{-1}$ makes the chip vulnerable to latch-up induced by nuclear reactions in silicon. This case shows that the LHC experiments should exercise great care in using components manufactured in commercial-grade (non-hardened) technologies (both ASICs and COTS components).

The assessment of the radiation tolerant approach has been completed by the development of demonstrator circuits designed and fabricated in commercial quarter micron CMOS technologies. Three demonstrators have been developed and tested in 2 different processes (referred to as Technology A and Technology B):

1. **A test vehicle circuit (Technology B):** it consists of low noise transistors, ring oscillators, an LVDS driver, several shift registers and total-dose and SEU-hardened digital standard cells. Measurement of the chip has confirmed the intrinsic radiation tolerance of the ultra-thin gate oxides of 0.25μm MOS. The radiation tolerant design technique developed to enhance the robustness to total dose and SEE effects has also been demonstrated. Measurement indicates that the threshold voltage shift after a very high total dose of 30 Mrad is only 20 mV for NMOS and 50 mV for PMOS devices. The carrier mobility, which governs device speed, is only decreased by 5% after the same total dose. Transistors designed in 0.25μm technology with radiation tolerant practices have shown no significant leakage current degradation after 30 Mrad of total dose exposure. Transistors for noise measurement were also included. The white noise voltage spectral density has been measured as approximately 1.3 $nV/Hz^{1/2}$ for transistors with W=2000 μm and L=0.36μm, and with a drain current of 500 μA.
2. **A demonstrator pixel readout array developed in collaboration with ALICE (Technology B)**[1]. This is a mixed-signal circuit developed with radiation tolerant practices, with particularly challenging analog specifications. Before irradiation measurement of the demonstrator confirmed its full functionality and showed that the performance was in reasonable agreement with simulations. It has been successfully tested to radiation in the NA50 beam with 450 GeV/c protons. The chip remained functional up to a flux of $9\ 10^{14}$ $protons/cm^2$ (localized in an area of 2mm x 2mm) and recovered its initial analog performance after 20 hours annealing at room temperature. No evidence of latch-up has been observed during the radiation test with high-energy protons. A radiation test carried out with 10 keV X-rays has confirmed the result obtained with the proton irradiation.
3. **An analog demonstrator chip (technology A).** This demonstrator circuit consists of large transistors for noise measurement, and a fast transimpedance preamplifier designed for the readout of silicon drift and silicon strip detectors. Recent preliminary measurements before irradiation confirm the expected simulated analog performance: peaking time of 10ns, gain of 10 mV/fC, and noise under 1000 e^- rms. Radiation tests are under way.

The measurements of total dose effects in elementary devices in Technology A and Technology B confirm that commercial 0.25μm CMOS technologies offer a very high level of radiation tolerance when enclosed transistor geometry and guard rings are employed. A geometrical model of the enclosed MOS transistor has been developed and successfully compared with experimental results.

The SEU sensitivity of digital circuits designed in deep submicron CMOS technologies is now recognized to be an important issue for the LHC experiments. We have used heavy ions to characterize SEU effects in three different versions of shift registers: one based on standard static DFF cells, another on dynamic DFF cells, and

[1] The pixel demonstrator was manufactured on the same engineering run as the technology test vehicle.

one on a novel SEU-hardened static cell. Measurements in the absence of clock (unclocked mode) have revealed an LET_{th} of 15 $MeVcm^2mg^{-1}$ for the standard static register. This relatively high threshold, which could be high enough to protect the cell content in the LHC radiation environment, is a consequence of the use of enclosed devices. The SEU-hardened cell, with a measured LET_{th} of 89 $MeVcm^2mg^{-1}$, is a very efficient solution to protect the content of memory cells, but is not adequate for clocked applications (such shift registers) as its SEU tolerance decreases dramatically in that case (LET_{th} decreases to 5.6 $MeVcm^2mg^{-1}$). Finally, the dynamic cell is very sensitive to SEU, with a LET_{th} of 3.2 $MeVcm^2mg^{-1}$.

In collaboration with CMS, a simulation tool based on the FLUKA and TRIM codes has been developed for the prediction of the SEU rate in the LHC radiation environment. The simulations estimate the upset rates, in the CMS tracker regions, for a submicron technology to be of the order of 8.10^{-7} to 8.10^{-10} upset/bit/s depending on the distance from the beam line. The upset rate prediction does not yet include the contribution of thermal neutrons, which could play a major role in the outer detector regions

Building on the experience and results of the demonstrator chips, a radiation tolerant standard cell library has been developed in a quarter micron CMOS technology. The cell library includes 30 core cells and 10 I/O cells, and is designed with the radiation tolerant layout techniques. Simulations indicate an improvement in speed of a factor 5, with a power reduction of a factor 25 and an increase in gate density of a factor 8 when compared with a less advanced 0.8 µm CMOS technology. The dependence of propagation delay of an inverter (50ps at 2.5V) and power dissipation (0.03 µW/MHz/gate) on total dose effects has been measured. After 30 Mrad there is no evidence of degradation in speed, or of increased power dissipation. A design kit supporting ASIC development on the Cadence CAE platform is in development. This will support the design of both analog and digital circuits in quarter micron technology using the radiation tolerant standard cell library, and will be compatible with standard simulation and Place-and-Route CAE tools.

The use of COTS components in the radiation environment of the LHC has been discussed with experts of specialized agencies and institutes. Preliminary guidelines for COTS selection, qualification and procurement procedures for LHC experiments are under study. A coordination effort for COTS support among LHC experiments is in preparation. In collaboration with ST microelectronics, a radiation tolerant bipolar technology suitable for the development of a low drop radiation tolerant voltage regulator has been identified, tested and qualified up to a total dose of 500 krad and 2.10^{13} $neutrons/cm^2$. The specification has been established in collaboration with ATLAS and CMS. The production of the Voltage Regulator prototype is under way.

For 1999, work on the selection, qualification and procurement of COTS components for LHC will be carried out in the framework of a separate co-ordination project, which is the subject of an independent proposal [1]. The RD49 collaboration proposes to complement the R&D study carried out in 1998 by addressing the following goals:

1. **Radiation effects in quarter micron technology**
   - **Total dose**: monitor the radiation tolerance and process characteristics of the quarter micron process selected as the result of the call for tender. To this purpose, we propose to develop a test vehicle in the selected 0.25 µm CMOS process, which will be regularly placed in all future foundry submissions. The test vehicle will help to monitor the stability of the radiation tolerance for the future processing runs.
   - **SEE**: improve the understanding of the proton- and neutron-induced SEU mechanisms. This work will combine simulation and a measurement effort on SEU rate. Design solutions for SEU-tolerant flip-flops and memory cells will be developed and tested with particular attention to the clocked working mode. Test structures will be developed in the quarter micron process to perform pulse height measurements of the collected charge.
2. **Study of the analog characteristics of the selected quarter micron process**
   - Measurement of matching characteristics of enclosed transistors; the present measurements indicate an unexpected mismatch on large devices, which will be carefully explored using a dedicated test.
   - Characterization of the flicker noise of NMOS devices will be performed to clarify the noise increase for gate lengths below 0.5µm.
   - Development of a demonstrator analog memory circuit for the study of charge injection and the limits to dynamic range of analog circuits.
3. **Support to LHC experiments**

- **Design kit**: A design kit compatible with the CADENCE platform in the selected quarter micron process will be completed and made available to LHC design teams. The radiation tolerant standard cell library in development in 1998, will be completed, assessed and integrated in the design kit.
- **Organization of quarter micron MPW**: the first Multi-Project-Wafer runs will be organized by CERN to facilitate access of the new users to quarter micron technology.
- **LHC ASIC designs:** the transfer of radiation tolerant design know-how will be pursued for the following projects
  - (i) Completion of the development of the readout chip for ALICE pixel detector in quarter micron CMOS technology.
  - (ii) Front end electronics for the Silicon Drift Detector of ALICE in a quarter micron technology , in particular for the blocks which employ large dynamic range switched capacitor circuits: the 10-bit low power ADC
  - (iii) Development of the 1.2Gbit/s digital link for detector readout.
  - (iv) Continuation of the development of the 40 Mbit/s digital link for the control of the CMS tracker, and a 40 Msample fibre optic analog driver.
  - (v) Advice and support to other development teams using the RD49 rad-tolerant design approach (RAL, Heidelberg, Pisa, etc.).

4. Completion of the radiation tolerant voltage regulator project with ST Microelectronics

- Test of the prototype chip and assessment of the conformity with the specifications defined together with the LHC collaborations.
- **Radiation test**:
  - (i) total dose: post-rad measurement with X-ray up to 1 Mrad.
  - (ii) Displacement damage: Test to a neutron fluence up to 2.10^{13} n/cm^{2}.
  - (iii) SEL: measurement of the Threshold LET with ion beams

1. Introduction

During its second year, the RD49 collaboration has pursued the three main objectives that were proposed in the first status report [2] and were subsequently approved by the LHCC Electronics Board [3], namely:

- The detailed study of total dose and single event radiation effects in deep submicron CMOS processes.
- The transfer of radiation tolerant design know-how to LHC design teams.
- The understanding of the LHC needs in Commercial-Off-The-Shelf (COTS) components

Thus, in 1998 the collaboration has continued the study of the radiation tolerance of submicron CMOS technologies and has consolidated the results obtained in the first year. This study has focussed on quarter micron CMOS technology and, together with a detailed assessment of the radiation-tolerant design technique, has formed the main effort of the collaboration.

We recall that the rad-tolerant design approach relies on the use of deep submicron technologies to eliminate the effects caused by holes trapped in the gate oxides of the MOS transistor (the ultra-thin gate oxides employed in such technologies result in hole neutralization by tunneling of electrons). Effective radiation-tolerant designs can then be achieved when enclosed geometry devices are used to eliminate leakage paths under the thick field oxide along the edges of NMOS transistors. Further, the use of guard rings prevents leakage between devices and reduces sensitivity to single-event latch-up.

In order to confirm the intrinsic tolerance of deep submicron technologies to total dose effects and also to verify the radiation-tolerant layout technique, as documented in the previous status report, we obtained samples of integrated transistors from a second manufacturer. These samples included transistors laid out using both the standard and the enclosed device geometry in a quarter micron CMOS technology (hereafter referred to as technology A). The enclosed transistors were shown to have total dose characteristics very similar to those of the first quarter micron technology characterized (which we will refer to as technology B).

This important result has confirmed our expectation that a high tolerance to total dose effects can generally be achieved in quarter micron CMOS technologies, and is not a feature of the details of a particular technology.

A quarter-micron CMOS demonstrator chip has been developed in technology B using radiation tolerant practices in order to study total dose and single event effects in more detail. This demonstrator contains appropriate test structures; several digital standard cells and a prototype pixel readout array laid out using the radiation-tolerant design rules. These demonstrator circuits have been characterized for both total dose and single event effects. In order to understand whether single-event effects are an important issue at the LHC, we collaborated with CMS to estimate Single Event Upset (SEU) error rates in the environment of the tracker by combining our technology measurements with Monte Carlo simulations of the radiation environment.

The radiation-tolerant design methodology in quarter-micron technology proposed by the RD49 collaboration has attracted considerable interest in the LHC physics community. Six new institutes have joined the RD49 collaboration: FERMI National Accelerator Lab, the University of Montreal, the Institute of Physics in Prague, TIMA Grenoble, the Brunel University of London and the University of Rome II. Several institutes have now decided to employ this strategy of hardening ASICs for LHC front-end electronics applications and are now engaged in design work. In order to support these LHC developments RD49 has designed a radiation-tolerant standard cell library and developed a design kit for the Cadence CAE tool environment that allows design rule checking (DRC), comparing layout versus schematic (LVS) and parasitic extraction for enclosed devices.

A call for tender for the provision of foundry services in quarter-micron CMOS technology for a period of five years has been issued. This is intended permit prototyping for the rad-tolerant developments and the subsequent production of radiation-tolerant electronics for the LHC experiments.

Awareness of the numerous risks associated with the selection and procurement of COTS components for reliable operation in the outer LHC detectors and the caverns is increasing and the collaborations have set up working groups to examine specific aspects (e.g. power supplies and other electronics in the caverns). However, these COTS issues apply equally to several sub-detectors in the LHC experiments. At the request of the LHC Electronics Board, a proposal for a co-ordination effort for COTS support among LHC experiments has been

prepared [1]. In collaboration with ST Microelectronics, we have started the development of a low drop radiation tolerant voltage regulator based on the specification established with the LHC collaborations.

2. Characterisation of the total dose effects in 0.25 μm CMOS processes

Total dose effects in two quarter-micron CMOS processes from two different semiconductor manufacturers (technologies A and B) have been measured. Total dose irradiation tests have been performed at room temperature, under bias, mainly using the SEIFERT RP-149 X-ray facility (10 keV peak with tungsten target) operated by the CERN microelectronics group. The dose rate was about 4 krad(SiO_2)/min for total doses up to 1 Mrad, and about 15 krad(SiO_2)/min for total dose up to 30 Mrad(SiO_2). Additional irradiation tests have been performed for technology B with a ^{60}Co γ-ray source.

The dependence of radiation effects as a function of the total dose was monitored by measuring MOS device parameters such as the threshold voltage, source-drain leakage current, transconductance and subthreshold swing. To study post-radiation effects (neutralization of oxide traps and the formation of interface states), parametric measurements were performed after annealing. Annealing took place under bias at room temperature for one day, and then for one week at 100 °C (qualification procedure ESA/SSC No. 22900).

2.1 Total dose results for the technology A

In our previous status report [2] we presented measurements of total dose effects made with devices integrated in the quarter micron CMOS process of foundry B. This year the total dose study was repeated on integrated transistors delivered by a different silicon foundry (Technology A) in order to confirm that the observed radiation tolerance can be attributed to characteristics that are common to all deep submicron technologies and are not a feature of a particular technology. The devices characterized in Technology A included standard NMOS and PMOS transistors and enclosed NMOS transistors found in the manufacturer's standard test vehicle. The tested devices included several transistors with common gate, common source and separate drains. Some of these transistors had a protection diode at the gate. The devices studied were:

- **Standard NMOS transistors**. All the transistors tested had a channel width of 10μm, but their length varied between 0.25μm and 10μm.
- **Standard PMOS transistors**. The width of the transistors was constant (10μm) and again the length varied between 0.25μm and 10μm.
- **Enclosed NMOS transistors**. The transistors had constant width (50μm) and their length varied between 0.25μm and 10μm. For enclosed transistors with W/L ratio of 50/0.25μm, two types of polysilicon gate contact were implemented – in one case over the field oxide and in the other case over the active area.

Standard NMOS

Figure 1 shows the dependence of the source-drain leakage current for three devices with different channel lengths (0.25, 0.4 and 10 μm) as a function of total dose. Irradiation took place in steps of 10 krad(SiO_2) up to a final total dose of 100 krad(SiO_2). The leakage current starts to increase at around 20 krad(SiO_2) with a lower total dose threshold for 0.25 μm gate length[2]. After annealing, devices recovered their prerad characteristics except for the shorter device. Further irradiation up to a total dose of 1 Mrad (not shown here) resulted in a saturation of the leakage current within the 10-100 μA range, and no significant recovery was observed after annealing.

[2] Note that the total dose threshold for the onset of leakage current in standard NMOS devices implemented in Technology B [2] was higher than that observed here. The difference is believed to be due to differences in the Shallow Trench Isolation (STI) technique and the radiation behavior of the thick field oxide employed in the two technologies, which is technology dependent and might be better in a specific technology.

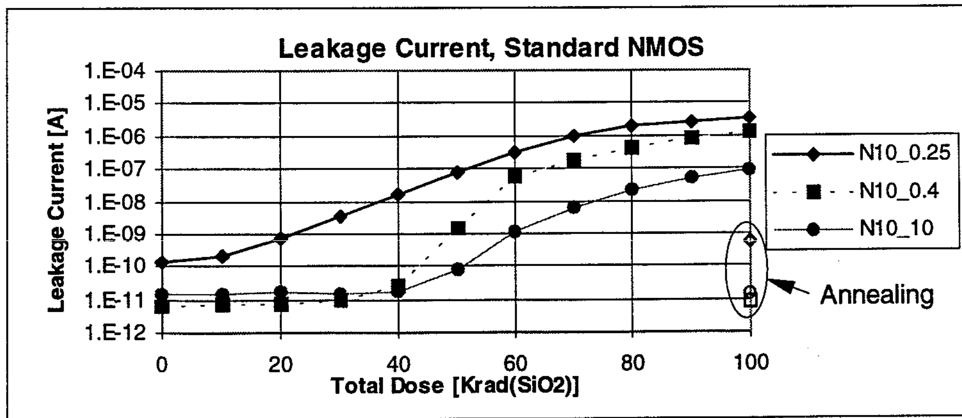

Figure 1. Leakage current in standard NMOS of technology A up to 100 krad

Measurements of the threshold voltage shift of technology A NMOS transistors are reported in Figure 2. For the two smaller devices the threshold voltage shift observed after 1 Mrad(SiO_2) is less than 5 mV. This measurement confirms the result obtained last year with another quarter micron technology (technology B) [4]. The large threshold voltage shift of the long channel transistor (W/L=10/10μm) is a measurement artifact due to the transistor leakage current. For this device, the leakage current is comparable to the channel current at $V_{gs} = V_{th}$

After annealing, a small 'rebound effect' of very small amplitude (ΔV_{th}=4 mV) indicates the formation of new interface states.

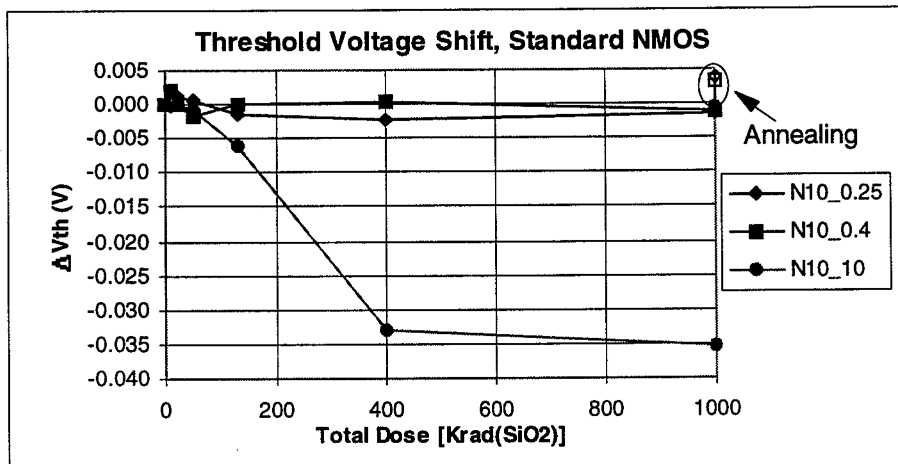

Figure 2. Threshold voltage shift in standard NMOS of technology A

Standard PMOS

Measurement of the source-drain leakage current has also been performed on technology A PMOS devices (not shown here) and, as expected, no visible increase has been observed after 1 Mrad. The threshold voltage shift has been measured up to 1 Mrad as shown in Figure 3. The observed threshold voltage shift is less than -6 mV, about the same amplitude observed with the NMOS device. A negligible annealing of the threshold shift of about +1 mV was observed.

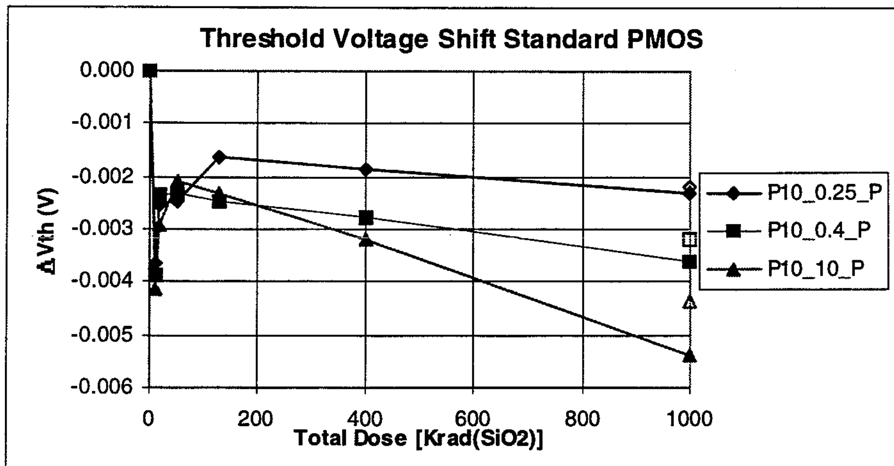

Figure 3 Threshold voltage shift of standard PMOS technology A

Enclosed NMOS

Edgeless NMOS transistors with an enclosed gate topology are used to eliminate the post-irradiation leakage paths associated with the transistor edges of the layout topology. As shown in Figure 4, the enclosed NMOS devices in Technology A exhibited no increase of leakage current in measurements up to total doses of 10 Mrad. This confirms the effectiveness of this radiation tolerant layout practice as demonstrated last year with another quarter micron technology (technology B) [4].

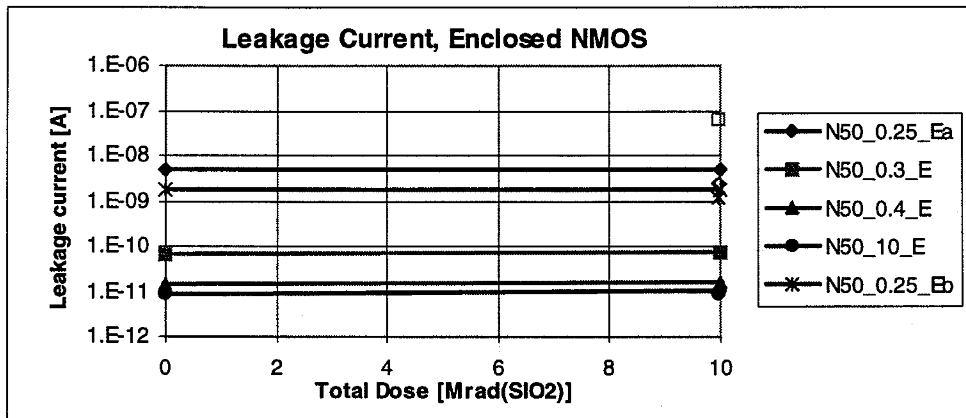

Figure 4. Total dose effect on source-drain leakage current of enclosed NMOS in Technology A. No degradation is observed up to 10 Mrad.

The measurement of the threshold voltage shift for enclosed NMOS devices is shown in Figure 5 for total doses up to 10 Mrad. A positive shift of amplitude of +15 mV is observed. This is explained by the fact that the relatively long exposure time to reach the total dose of 10 Mrad was sufficient to enable the formation of interface states during irradiation. This causes a positive shift in the threshold voltage since the contribution of the interface states dominates over oxide-trapped charge. After annealing, the positive shift is increased up to 30 mV, consistent with the formation of new interface states. This result indicates that the threshold voltage shift of quarter micron NMOS transistors is dominated by the formation of negative gate interface states. Holes trapped in the gate oxide are neutralized by electrons tunneling through the very thin (6 nm) gate-oxide and do not contribute significantly to the V_T shift.

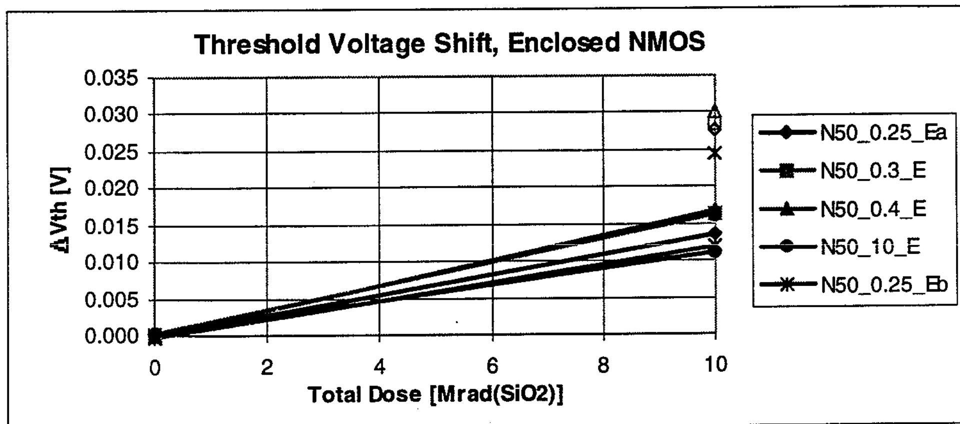

Figure 5 Threshold voltage shift of enclosed NMOS transistors in technology A up to 10 Mrad for devices with 5 different gate lengths.

The total dose effect on the sub-threshold swing has been measured after irradiation and after annealing. For an enclosed NMOS with an aspect ratio of 50/0.25 the sub-threshold swing increases from 85 mV/dec measured pre-rad to 88 mV/dec measured after 10 Mrad. The change in mobility, extracted from the transconductance measurement, showed a decrease of less than 5% after 10 Mrad.

2.2 An Analog demonstrator chip in 0.25 μm Technology A

A demonstrator chip has been developed in Technology A in order to study the analog characteristics of quarter micron CMOS process. The demonstrator contained:

- Large standard PMOS, standard NMOS and enclosed NMOS transistors for noise measurement. The transistors had a constant gate width of 1000 μm and gate lengths of 0.25, 0.35, 0.4 and 0.5 μm
- A fast Transimpedance preamplifier specially designed to exploit the intrinsic high speed of the quarter micron technology.

The preamplifier was designed keeping in mind a typical specification for the readout of silicon strip detectors. Our SPICE simulations, shown in Figure 6, indicate that a pulse peaking time of 10 ns can be achieved with a power consumption of about 1.2mW. Such speed performance is superior to that which can be achieved with less advanced CMOS technology, and is comparable with the speed obtained in front-end amplifiers designed in bipolar processes. Samples of the demonstrator chip have been recently received and preliminary measurements are in agreement with the simulation results.

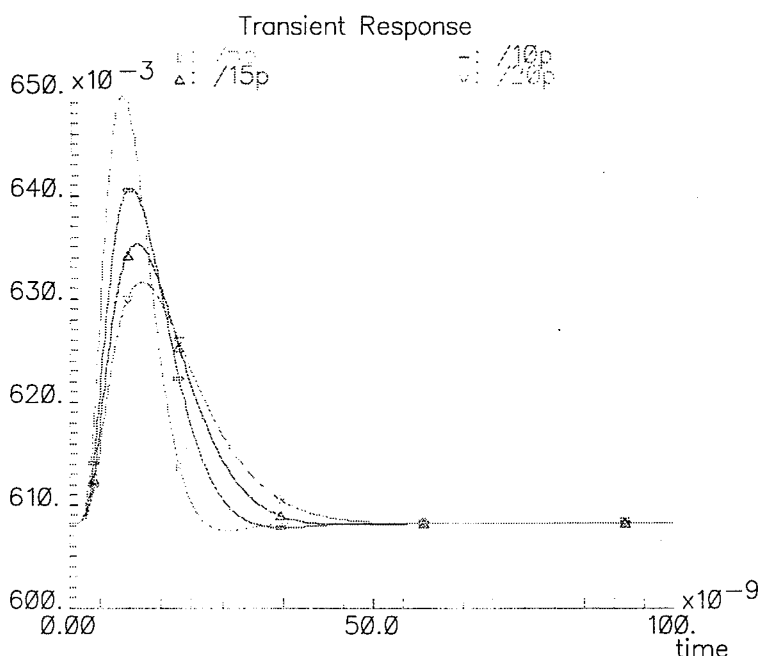

Figure 6 SPICE simulations of the fast transimpedance preamplifier designed in 0.25 µm Technology A. Output pulse waveforms are shown for an input capacitance of 5, 10, 15 and 20 pF. Input charge is 4 fC.

2.3 A demonstrator chip in 0.25µm Technology B

Extensive results obtained with Technology B[3] have been reported at the LEB workshop that was held in Rome, September 1998 [5]. The characterization of Technology B has been performed with a radiation tolerant evaluation chip developed by the RD49 collaboration.

The evaluation chip designed for this study contained the following test structures:

- Single transistors (enclosed and standard, NMOS and PMOS) with different gate lengths.
- Very large transistors for noise measurements. The channel width of 2000µm in order to have a high drain current white noise density. Different gate lengths of standard PMOS and enclosed NMOS have been done (L = 0.36, 0.5, 0.64, 0.78 and 1.2µm).
- Matched enclosed NMOS transistors with different gate lengths.
- Guard rings around NMOS transistors were always used.
- Digital standard cells (inverters, nand and nor gates, flip-flops) laid out with and without the radiation tolerant approach.
- 3 shift registers for characterization of total dose and SEU effects.
- A radiation tolerant LVDS receiver.
- A demonstrator pixel readout array using the radiation tolerant technique.

2.4 Summary of total dose effects for transistors and resistors, Technology B

Enclosed NMOS transistor

Enclosed transistors with gate length close to minimum were irradiated under worst case bias conditions and showed limited threshold voltage shifts: 35mV for NMOS and 70mV for PMOS after 30Mrad(SiO_2) as shown in Figure 7. For a total dose of 10 Mrad, the corresponding values are 15 and 30mV respectively. Very little

[3] Technology B is a commercial 0.25µm CMOS technology and was selected for the demonstrator chip on the basis of the promising results obtained in 1997 with devices supplied by the vendor [2]. The study of total dose effects with technology B has now been extended up to 30 Mrad.

degradation of other parameters such as transconductance and mobility was observed (always less than 6%). The measurement of the sub-threshold swing showed an increase of 5mV/dec for the NMOS and 2mV/dec for the PMOS. This indicates that for thin gate oxide (5nm), both hole trapping in the oxide and generation of interface states give contributions of the order of tens of mV to the threshold shift after 10-30Mrad of total dose.

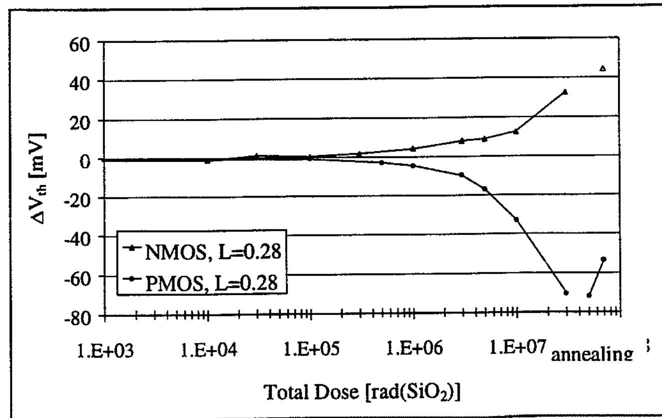

Figure 7 Threshold voltage shift of PMOS and NMOS devices in Technology B. Unfilled symbols show the evolution after 24 hours of annealing at room temperature, and after 1 week at 100°C.

These total dose results are in good agreement with the preliminary results obtained last year for Technology B, and also with the result obtained for Technology A as reported in section 2.1. No leakage current was observed after irradiation of these enclosed devices, as can be seen from Figure 8 (by comparing the pre-rad and post-rad curve for Id=f(Vgs)). Our measurement also confirmed that the systematic use of guard-rings around NMOS transistors provides effective device isolation.

We have also investigated whether the variation of the threshold voltage shift after irradiation could be gate length dependent. Our measurement indicates that there is a small effect on the NMOS; an increase of a few mV for shorter gate lengths. However, we believe this effect is small enough not to be an important issue.

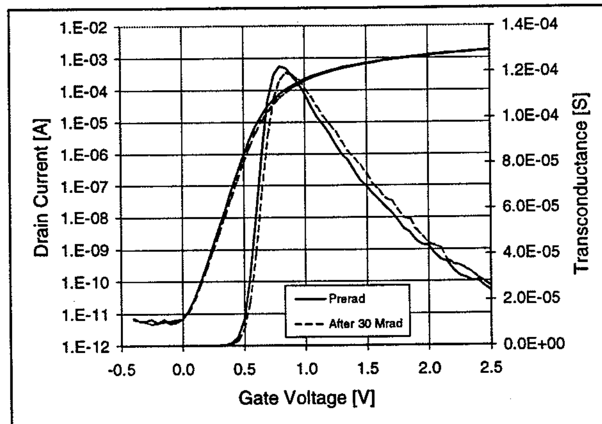

Figure 8 Drain current (log scale) and transconductance before and after irradiation for an NMOS edgeless device with L = 0.28μm (Technology B).

Standard NMOS post-rad leakage current

The source-drain leakage current has been measured for standard NMOS transistors of different gate length up to 200 krad. No increase of leakage current was observed, the leakage staying constantly below 10 pA for all standard NMOS transistors gate lengths (0.28 to 5μm). These results are much better than the measurement reported on technology A in section 2.1. The quality of the field oxide and differences in Shallow Trench Isolation (STI) processing can explain the different radiation tolerance of the two technologies to leakage.

Resistors

Three n-well resistors were implemented in the demonstrator chip in Technology B, with nominal values ranging from 0.2 to 3.3 kΩ. The observed variation of the resistor values after a total dose of 10 Mrad (SiO2) was less than +4% in all cases. This increase is well within the min/max range of process variations, and therefore should not add any significant uncertainty factor for the design of analog circuits.

Total dose effects on noise

A preliminary noise measurement made in 1997 on a 0.5 µm CMOS process indicated that submicron processes exhibit good noise characteristics. The study of the noise and its degradation after irradiation

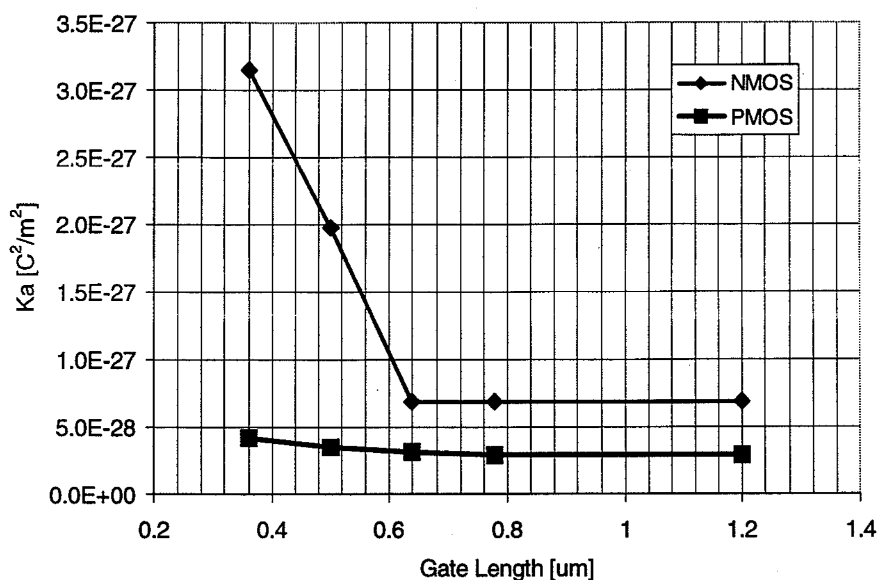

Figure 9. 1/f noise parameter K_a for NMOS and PMOS in Technology B as a function of the gate length

performed in 1998 with the quarter micron Technology B confirms this behaviour. However, measurements before irradiation of the large transistors showed that 1/f noise of NMOS devices exhibit an unexpected increase for gate lengths smaller than 0.64 µm, as can be seen in Figure 9. This indicates that short channel NMOS devices should be avoided in analog designs where noise is an issue, or PMOS devices, which do not exhibit this effect, should replace them. After a very high total dose of 30Mrad under worst case biasing, very little degradation occurred for both PMOS and NMOS devices, as shown in Figure 10.

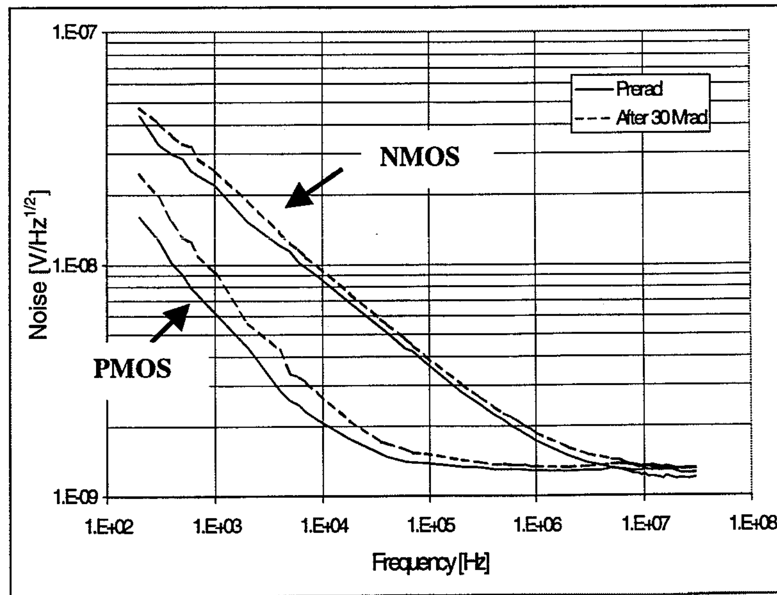

Figure 10 Noise spectra for an NMOS (top plots) and a PMOS (bottom plots) device in Technology B measured before and after irradiation. L = 0.36μm for both the devices.

The white noise measurement has been performed on five NMOS and five PMOS devices, with a constant W=2000μm and five different gate lengths of 0.36, 0.5, 0.64, 0.78, 1.2 μm. The layout of the NMOS has an enclosed gate (radiation tolerant), and the PMOS employs a standard layout geometry. The measurements have been made with a drain-source voltage Vds of 800mV, and the substrate and well were grounded. During the measurement the drain current was 500 μA, a value for which the MOS devices were in a moderate inversion regime. It was not possible to perform noise measurement in the strong inversion regime, which would have required a drain current above 10mA for the large transistor geometry used. However, the noise result obtained is applicable to the input transistor of low-noise amplifiers, which usually operate in the moderate inversion regime. Table 1 shows values of the tranconductance (g_m) and the noise spectral densities measured at 10 MHz, a frequency where the 1/f noise contribution is negligible.

Table 1. Measurement of transconductance and noise spectral density of Technology B PMOS and NMOS devices at 10 MHz. The gate width was 2000 μm and the drain current was 500 μA.

Gatelength [μm]	0.36	0.5	0.64	0.78	1.2
PMOS g_m [mS]	9.5	8.8	8	7.5	6.6
PMOS noise [nV/Hz$^{1/2}$]	1.28	1.32	1.37	1.43	1.59
NMOS g_m [mS]	11.5	11.1	10.6	10.2	9.3
NMOS noise [nV/Hz$^{1/2}$]	1.18	1.2	1.22	1.25	1.28

The measured noise spectral densities are not very different, and they are in the range of 1.2 – 1.6 nV/Hz$^{1/2}$. This is easily explained by the fact that values of the transconductance close to weak inversion do not change very much with the gate length.

To extract the white noise coefficient Γ, we have expressed the white noise voltage referred to the gate by the relation:

$$V_n = 4kT(\tfrac{1}{2})\frac{\Gamma}{gm} \quad \text{for the MOS operating in weak inversion}$$

We find that the white noise coefficient Γ (ideally 1) ranges from 1.9 to 2 for the NMOS devices and from 1.87 to 2 for the PMOS devices.

2.4 Summary of total dose effects of digital circuits in Technology B

Shift registers

The three radiation tolerant shift register designs (1000-2000 stages) implemented in the Technology B demonstrator chip have been irradiated with X-rays. Samples were biased with a power supply of 2 V, and measurements were performed at 1, 3, 5, 10, and 30 Mrad(SiO2). During the irradiation the shift registers were in operation, and an alternating pattern of 0s and 1s was circulated at a frequency of 1.25 MHz. No error was detected during irradiation up to 30 Mrad, and no increase of power consumption has been observed.

LVDS receiver

A Low Voltage Differential Signaling (LVDS) receiver was implemented in the demonstrator chip using radiation tolerant practices. The receiver circuit proved to be fully operational and it was irradiated with X-rays under bias and at ambient temperature with a dose rate of 16.2 krad/min. The irradiation tests were made in two steps: one up to a total dose of 1 Mrad and the other up to 10 Mrad. In both cases the receiver was tested after irradiation with the performance showing no observable degradation. The receiver was designed to operate with a nominal 2V power supply; however, it was possible to operate it successfully for power supply voltages between 1.5 and 2.5V. Since the allowed common mode range for an LVDS signal at the input of an LVDS receiver is 0.2 to 2.2V and the receiver was designed for a 2V nominal power supply its input stage was designed as a true rail-to-rail amplifier. The tests showed that the receiver could be operated with common mode voltages between 0V and the power supply voltage. Tests were successfully carried out for frequencies up to 120 MHz. The receiver displays a nominal delay of 830 ps for an input differential signal of 300mV amplitude.

2.5 Summary of the development of the pixel readout demonstrator chip in Technology B

Together with the submission of the demonstrator test vehicle chip in Technology B, we have submitted a pixel readout chip in collaboration with the ALICE collaboration. This demonstrator chip is a mixed-signal ASIC with the typical constraints of a front-end electronics chip for LHC experiments: namely high readout channel density, high speed operation, low electronic and coupling noise and low power consumption. Last year, a previous pixel test chip implemented in a commercial 0.5µm CMOS process, and also designed with radiation tolerant practices, was tested for total dose effects. The total dose tolerance of the 0.5µm pixel chip, measured between 600 krad and 1.7 Mrad, was limited by the radiation-induced threshold voltage shifts that were intrinsic to the technology used.

The new 0.25 µm demonstrator chip builds on the experience of the previous pixel readout. It is an array of two columns each containing 65 identical cells. Full results have been already reported elsewere [6,7].

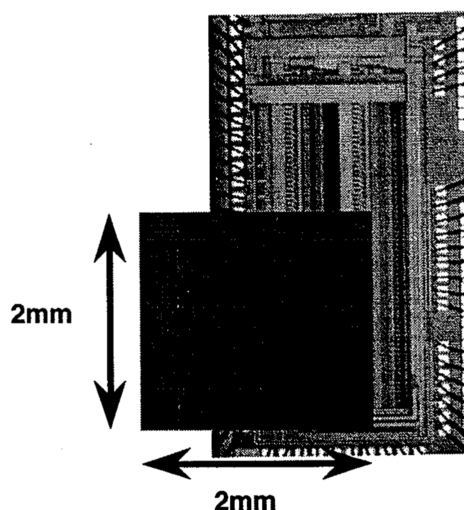

Figure 11 A photograph of the chip with the approximate shape and position of the proton beam indicated

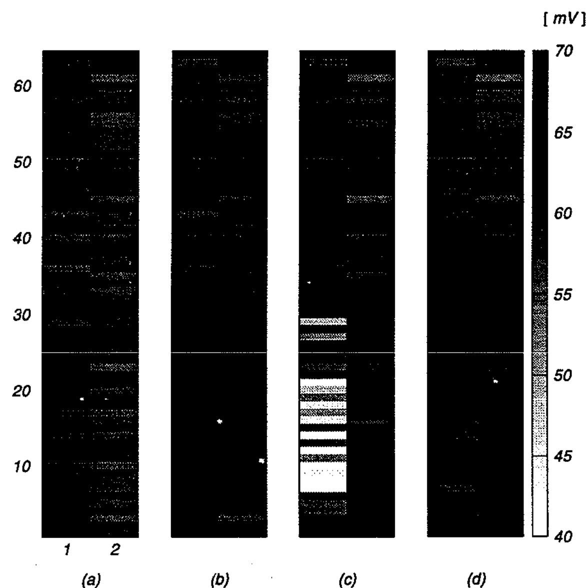

Figure 12 Pixel thresholds during and after the proton irradiation. (a) thresholds before irradiation, (b) thresholds after 8 x 10^{12} protons (c) thresholds after 6 x 10^{13} protons and 4 hour anneal (d) thresholds after 6 x 10^{13} protons and 20 hour anneal. 1 mV corresponds to 100 e^-.

Each readout cell comprises a preamplifier, a shaper filter, a discriminator, a delay line and readout logic. The circuit occupies 10mm^2, and contains about 50 000 transistors. The pixel demonstrator chip has been characterized electrically using the analog test input, and it is fully functional. The minimum discrimination threshold is 1500 electrons with a spread of 160 electrons rms. Channel electronic noise is about 220 electrons rms.

Radiation test performed with X-rays up to 30 Mrad showed no degradation of power supply current (analog and digital), and the chip remained fully functional. After the same total dose and annealing, electronic noise and threshold spread are slightly increased without affecting the overall analog performance of the chip. This result confirms the effectiveness of the radiation tolerant practices applied to 0.25 μm technology and the great improvement of radiation tolerance when compared to the result obtained with the 0.5 μm process chip last year. A further test was made with high energy protons at the NA50 experiment on the CERN SPS machine. Figure 11 indicates how the chip was placed in the high intensity beam of 450 GeV/*c* protons, with the beam focussed on a roughly square 2 mm x 2 mm area. In total, the chip received 3.6 x 10^{13} protons, over a 12 hour period, representing an equivalent of 9 x 10^{14} protons/cm^2 in the target area.

The chip was kept under bias the whole time and read out between spills of the machine. Figure 12 shows the evolution of the thresholds during irradiation and anneal. During irradiation the threshold of the hit pixels was reduced and the noise increased to ~1 000 e^- rms by the end of exposure. During anneal, at room temperature, the threshold recovered and even increased slightly, whilst the noise returned to its pre-irradiation value. The pixels outside the target region remained unchanged throughout the test. In addition, there was no increase in power consumption. No evidence of latch-up has been observed during the radiation test with high-energy protons.

3. Modelling of the enclosed NMOS transistor

The use of the enclosed geometry for the NMOS transistor is the core of the radiation tolerant technique developed by RD49. This technique eliminates radiation-induced transistor leakage current in a way which does not rely on the characteristics of the technology used, and is therefore process-independent. Since this layout technique is not a common practice in VLSI design, we have focused our work on issues related to the use of this type of device: geometrical modeling, output conductance characteristics and device matching.

3.1 Geometrical model of the enclosed device

We have developed a model to calculate the effective aspect ratio (W/L) of enclosed devices [8,9]. The transistor studied has a square layout with corners cut at 45° as recommended by manufacturers in order to avoid

"over-etching effects". In this case, the model is based on the decomposition of the MOSFET in three basic sub-transistors: 'edge', 'corner' and 'linear corner'. This modelling leads to the following expression for the aspect ratio:

$$\left(\frac{W}{L}\right)_{eff} = 4\frac{2\alpha}{\ln\dfrac{d'}{d'-2\alpha L_{eff}}} + 2K\frac{1-\alpha}{1.13\cdot\ln\dfrac{1}{\alpha}} + 3\frac{\dfrac{d-d'}{2}}{L_{eff}}$$

where d and $d' = d - 2\frac{c}{\sqrt{2}}$ are as shown in Figure 13, α is a constant equal to 0.05 and K is a geometry-dependent parameter set to 7/2 for short channel transistors ($L \leq 0.5\mu m$) and 4 in the other cases.

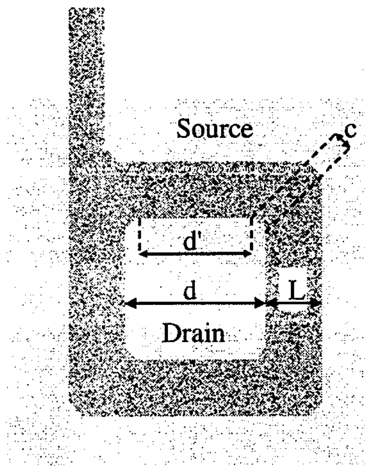

Figure 13 Basic shape of enclosed transistor used in the modeling study

The aspect ratio results therefore as a sum of three terms, the first is dependent on L and d, and the second is constant. The additional contribution comes from the linear corner transistor with channel width c and length $L\sqrt{2}$.

The calculated effective aspect ratio obtained using the above equation has been compared to the one extracted from measurement of the individual transistors in different technologies. The results for the quarter micron Technology B are summarised in Table 2 and are in good agreement with the values extracted from the measurement of the transconductance.

Table 2. Comparison between calculated $(W/L)_{eff}$, derived from the formula and extracted $(W/L)_{eff}$ derived from measurements of the enclosed NMOS transistors.

L_{drawn} (μm)	Calculated $(W/L)_{eff}$	Extracted $(W/L)_{eff}$
0.28	14.8	15
0.36	11.3	11.2
0.5	8.3	8.3
1	5.1	5.2
3	3	3.2
5	2.6	2.6

3.2 Output conductance of the enclosed NMOS

We have observed an asymmetry in the output conductance of the enclosed transistor. Since the gate topology is annular, the source and drain contacts can be chosen inside and outside the ring of the gate, or vice versa. Table 3 shows the measured values for the cases where the drain is inside (G_{di}) and where it is outside

(G_{do}). The fact that G_{di} is higher can be explained as follows: the distance between the pinch off point and the drain, due to the conservation of the space charge region for the same bias potentials, will be smaller when the drain is outside. An increase of V_{DS} will in this case increase less the drain current, resulting in a higher G_{di}. The asymmetry between G_{di} and G_{do} increases with L as the outer perimeter of the gate increases with L, while the inner does not.

Table 3. Output conductance for enclosed NMOS transistors of different gate length. G_{di} = inner diffusion as drain, G_{do} = outer diffusion as drain. Difference = (G_{di} - G_{do})/G_{di}.

L_{drawn} (μm)	G_{di} (μS)	G_{do} (μS)	Difference (%)
0.28	11.09	9.62	19
0.36	7.17	5.55	23
0.5	4.10	2.73	33
1	1.68	0.79	53
3	0.57	0.17	70
5	0.41	0.10	75

3.3 Matching characteristics of the enclosed NMOS

The matching proprieties of transistors of identical geometry are usually a key parameter for analog applications, as for example in amplifiers and comparators, where offset is determined by the matching of differential pairs, and in current mirrors. We have measured the statistical difference in V_{TH} (ΔV_{TH}) for pairs of identically laid out enclosed NMOS as a function of the gate area. Geometrical characteristics of these transistors are shown in table 4.

Table 4 Geometrical gate area (S_g)values for enclosed devices of different gate lengths. L_d is the drawn gate length.

L_d (μm)	S_g (μm^2)
0.36	1.368
0.5	2.253
1	6.693
2	21.573
5	114.213

A sample of 100 chips containing transistor pairs of these 5 different geometries has been measured, and standard deviation $\sigma_{\Delta V_{th}}$ is plotted in Figure 14 as a function of the square root of the geometrical gate area (S_g). These values can be fitted to the following equation

$$\sigma_{\Delta V_{th}} = \sqrt{\left(\frac{A_{V_{th}}}{\sqrt{S_g}}\right)^2 + \sigma_0^2}$$

In the matching formula, the parameter σ_0 generally takes the value zero. However, in our case $\sigma_{\Delta V_{th}}$ shows a good linear slope for small devices, but "saturates" for bigger devices. This behaviour is still being investigated, and new test structures are being designed for this purpose. Best-fit evaluation leads to the following values for the equation parameters: $A_{V_{th}}$ = (5.40 ± 0.38) mV·μm and σ_0 = (0.95 ± 0.12) mV. $A_{V_{th}}$ fits well its expected value based on the literature benchmark $A_{V_{th}} = Kt_{ox}$ were t_{ox} is the gate oxide thickness (5.5nm in this case) and K is a constant fixed at 1 mV·μm/nm [8,9]. The matching of the β parameter gave similar results.

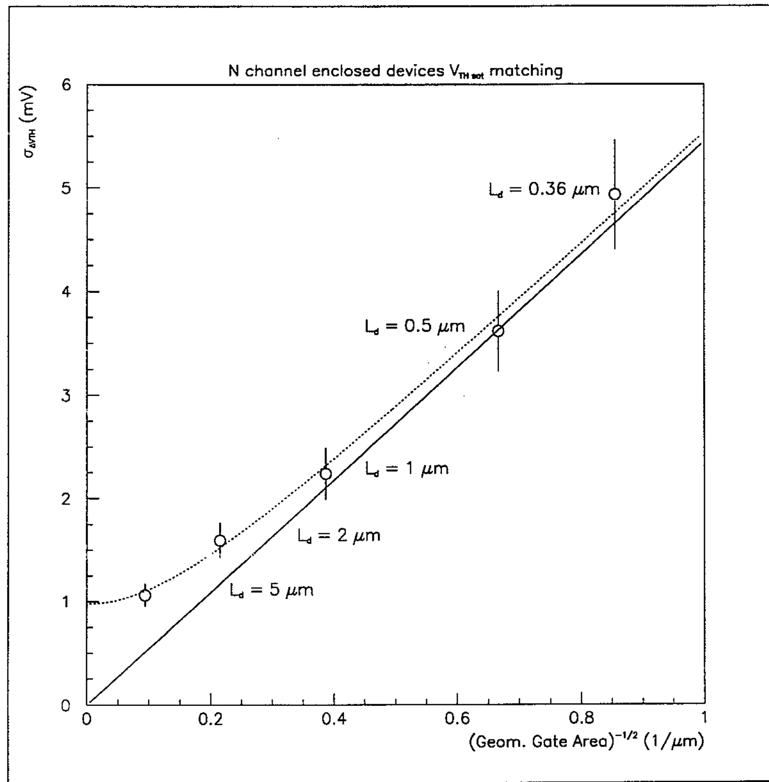

Figure14. $\sigma_{\Delta V_{th}}$ values for five pairs of enclosed n channel devices of different gate lengths, versus the inverse of the square root of the geometrical gate area.

4. Design issues for radiation tolerant mixed-signal circuits in 0.25μm technology

The use of commercial deep-submicron technology to implement digital mixed-signal ASICs creates new design challenges[10]. The low power supply voltage of 2.5V limits dynamic range of analog circuits. In our experience, the use of the BSIM3v3 model in the SPICE simulation of analog circuits has led to reasonable precision. However, in the case of transistors operated in moderate and weak inversion regime, discrepancies in the transconductance have been observed. Comparisons made with the EKV model developed at the EPFL (Lausanne) have shown that this discrepancy is a limitation of the existing BSIM3 model. However, apart from this one model imperfection, all other MOS device parameters obtained by simulations (output conductance, transconductance in strong inversion) that have been compared to parametric measurements of transistors showed an adequate precision for analog circuit design. However, a detailed model is needed for the use of enclosed transistors in analog design (this subject is addressed in section 3).

The increased number of available metal layers in the quarter-micron technologies (up to 5 in Technology B) can bring considerable advantages in terms of circuit density, signal shielding and series resistance of supply lines.

The use of edgeless devices and guard rings decreases substantially the device density capability of the technology. We estimate that the area penalty is a factor 3.5 in the worse case for a digital IC. However, if we compare device density for circuits designed with radiation tolerant practices in the quarter-micron process against a typical radiation hard process, we find that the radiation tolerant are still 8 times more compact than their equivalent in a typical 0.8 μm rad hard process.

4.1 Summary of the development the radiation tolerant library and the design kit

Building on the experience and results of the demonstrator chip, a radiation tolerant standard cell library has been developed in quarter micron CMOS technology [11]. The cell library includes 30 core cells and 10 I/O cells, and is designed with radiation tolerant layout techniques. Table 5 lists the standard cells included in the library. The combinatorial core logic consists of simple gates such as inverters and buffers with different driving strength, as well as NANDs, NORs and XNOR gates. More complex gates such as AND-ORs, OR-ANDs and multiplexers have been also included.

Latches and flip/flops are the basic building blocks of sequential digital circuits and, to a large extent, determine circuit speed and power dissipation. A static master/slave pseudostatic D-type Flip/Flop (D-F/F) has been included in the core logic of the library. A few other D-F/F cells based on this design that offer RESET, SET, and combined RESET-SET capabilities have also been included. A static 4-bit register with clear capability and a 1-bit adder have been included as well.

A dynamic True Single Phase Clock D-type Flip/Flop (TSPC D-F/F) has been designed and included in the library. It requires only one clock signal and is positive edge triggered.

A small set of I/O pads is included in the library. All pads offer ESD protection. Radiation Tolerant layout techniques have been applied also in the design of the ESD protection circuits. There are three types of output pads with different driving strength. Each type has a standard version and a version with a slew rate control output. A set of "glue cells" has also been developed to ease the design and enable the automated place & routing. These cells are "cap cells" that close the guard-rings at each end of the cell rows, corner cells for the chip power rings, power feed-through cells etc.

Table 5 List of standard cells in the rad-tol library

Core Logic	
Inverter 1X Drive	
Inverter 2X Drive	Buffer X4 Drive
Inverter 3X Drive	Buffer X8 Drive
Inverter 4X Drive	2 input XNOR
2 Input NAND	2 Input NOR
3 Input NAND	3 Input NOR
4 Input NAND	4 Input NOR
2-Wide 2-in AND-OR	2-Wide 2-in OR-AND
2-Wide 3-in AND-OR	2-Wide 3-in OR-AND
3-Wide 2-in AND-OR	3-Wide 2-in OR-AND
Static D-F/F	Static D-F/F, Set
Static D-F/F, Reset	Static D-F/F, Set, Reset
Dynamic TSPC D-F/F	Static D-F/F, Scan
2-Input MUX	4-Input MUX
D-Latch	D-latch RESET
4-Bit Register, Clear	1-bit Adder
I/O Pads	
Input pad, CMOS	
Output, 8 mA drive	Output, 8 mA, slew rate
Output, 16 mA drive	Output, 16 mA, slew rate
Output, 20 mA drive	Output, 20 mA, slew rate
I2C outpout	I2C outpout
LVDS driver	LVDS receiver

SPICE simulations of inverters indicate an improvement in speed of a factor 5, with a power reduction of a factor 25 and an increase in gate density of a factor 8 when compared with a less advanced 0.8 μm CMOS technology. The dependence of propagation delay of an inverter (50ps at 2.5V) and power dissipation (0.03 μW/MHz/gate) on total dose effects has been measured. After 30 Mrad there is no evidence of degradation in speed, or of increased power dissipation.

A design kit supporting ASIC development on the Cadence CAE platform is in development. This will support the design of both analog and digital circuits in quarter micron technology using the radiation tolerant standard cell library, and will be compatible with standard simulation and Place-and-Route CAE tools. Special physical design verification rules have been added to check for inconsistencies in radiation-tolerant designs (openings in the guard-rings around n^+ diffusions etc). Special device extraction routines have been inserted in the extraction rules file that enable a more precise extraction of the size (W/L) of the enclosed geometry transistors. The implemented cells were characterized through SPICE simulations and Verilog timing models have been developed to enable digital circuit simulations. Two sets of timing models of cells are available: one characterised at a supply voltage of 2.5V, and another one at a supply voltage of 2V. This will offer the possibility to use the library in applications where power consumption is an important issue.

5. Summary of the study of Single Events Effects (SEE) in 0.25μm Technology B

Full results of the SEE study on test structures integrated in technology B have been reported at the LEB conference held in Rome in September this year [5,12]. The SEU sensitivity of digital circuits designed in deep submicron CMOS technologies is recognized to be an important issue for the LHC experiments. All circuits tested are part of the demonstrator chip in technology B, which has been designed using radiation tolerant practices (enclosed NMOS and guard-rings).

We have used heavy ions to characterize SEU effects in three different versions of shift registers: one based on standard static DFF cells, another on dynamic DFF cells, and a third on a novel SEU-hardened static cell. SEU tests were run at a power supply voltage of 2V. Measurements in the absence of the clock signal (un-clocked mode) have revealed a threshold LET of 15 $MeVcm^2mg^{-1}$ for the standard static register. This relatively high threshold, which could be high enough to protect the cell content in the LHC radiation environment, is a consequence of the use of enclosed devices. For these devices, the minimum gate width is determined by the fact that the gate has to completely surround the drain diffusion. This means that minimum width devices cannot be designed. As a consequence, the capacitance of the nodes is higher than the minimum achievable in the standard layout geometry, and also the current drive of the transistors is higher than for the minimum size configuration. As a result, the critical charge for the cells to upset increases, and the LET threshold increases.

The SEU-hardened cell, with a measured LET threshold of 89 $MeVcm^2mg^{-1}$, is a very efficient solution to protect the content of memory cells, but is not adequate for clocked applications (as in shift registers) as its SEU tolerance decreases dramatically in that case. Solutions for clocked-circuit applications are under study. Finally, the dynamic cell is very sensitive to SEU, with a measured threshold LET below 3.2 $MeVcm^2mg^{-1}$.

The shift registers have also been used to measure the technology's vulnerability to Single Event Latch-up (SEL). No SEL was observed during the whole irradiation campaign, at an applied supply voltage of 2.5V, up to the maximum LET available of 89 $MeVcm^2mg^{-1}$. This result is representative of designs that make use of the radiation tolerant layout practices: the systematic use of guard rings assures a good local contact of the substrate to ground and is effective in decreasing the sensitivity to latch-up.

6. Study of the LHC Radiation Environment and SEE issues

6.1 SEU study with quarter micron technology

In 1997 the collaboration has started to study the radiation environment of the LHC experiments, and has performed preliminary Single-Event Latch-up (SEL) measurements on test circuits using heavy ion beams and a ^{252}Cf source. In 1998 we have started the evaluation of the risks associated with Single Event Upset (SEU), an issue that so far had not been addressed.

In the complex problem of radiation assurance of LHC electronics, upset effects present a particularly critical risk. If hardware failures caused by latch-up or component aging can be destructive, they are at least easily identifiable and can be localized in the overall electronic system and can therefore be repaired. However, in the case of single-event upset the effects may manifest themselves as intermittent corruption of physics data, or permanent corruption of calibration data, or loss of system control and synchronization functions, etc. The effects at the system level and the way in which SEU-induced software errors may propagate are hardly traceable (because the errors occur in random locations, are unpredictable and not reproducible). Debugging and fixing such problems is a nightmare scenario, therefore a proper evaluation of the risks, coupled with system design approaches that mitigate these risks is of capital importance. Due to the complexity of the problem, which is strongly dependent on the final system implementation and the precautions taken in the system design (redundancy, error detection and correction, etc.), we have only considered risks at device level in our study.

In our estimate of the SEU error rate in the LHC environment, we have limited the scope of the work to the radiation environment of the CMS tracker, but reasonable extrapolations of our conclusions could be made for ATLAS. Actually, there is essentially no difference between the radiation environment of ATLAS and CMS trackers, and the extrapolations of our results can be made for the other detector regions. Charged hadrons and neutrons dominate the radiation environment of LHC experiments. Therefore, the SEU rate is determined on the one hand by particle fluence and by the probability of nuclear reactions in material (silicon chip and surrounding material), and on the other hand by the SEU sensitivity of a given component. We have only considered in this study components in submicron technology.

The approach used to predict the SEU rate is the following:

1. The definition of a sensitive volume, which is CMOS technology dependent

2. The determination of the critical energy for SEU to occur. This can be evaluated with heavy-ion beam tests or can be approximated with a SPICE-like simulator.
3. Simulation of the radiation environment giving the probability of energy depositions by Monte Carlo simulations.
4. The integration of probabilities for the energy depositions above the critical energy leads to the evaluation of the probability of SEU.

In collaboration with CMS, this approach of SEU prediction has been developed using the FLUKA code as an event generator, and a modified version of TRIM for the energy deposition in silicon of the fragments. For a submicron technology with a critical energy of 1 MeV and a sensitive volume of $1\mu m^3$, the estimate for the upset rates in the CMS tracker regions was found to be in the range 8.10^{-7} to 8.10^{-10} upset/bit/s, depending on the distance from the beam line [12,13]. Our upset rate prediction does not yet include the contribution of thermal neutrons, which could play a major role in the outer detector regions.

6.2 SEL measurements made with the ALICE-128 chip

Standard ASICs and COTS components placed in the LHC radiation environment will be subjected to Single Event Latch-up (SEL). To derive a preliminary estimate of the SEL risk of standard components, we have studied in collaboration with ALICE the latch-up susceptibility of an ASIC that was designed, without special radiation tolerant precautions, in a standard 1.2 µm CMOS technology. The ASIC tested (Alice128C), was developed for the readout of the ALICE Silicon Strip Tracker and has a die area of 50 mm^2. The Latch-up measurement has been performed in collaboration with CNES, Toulouse using the 5 MV Tandem accelerator at IPN Orsay. The number of latch-up events occurring were recorded for different heavy ion species representing LET values ranging from 8 to 60 $MeVmg^{-1}cm^{-2}$. To prevent damage to the chip the latch-up current was externally limited to 500 mA. Table 6 shows the results of the latch-up test.

Table 6: Latch-up measurements made on the ALICE-128 chip

Ion species/angle	LET $MeVmg^{-1}cm^{-2}$	Ion Fluence ion/cm^2	Number of SEL observed	Cross-section [cm^2]
Br^{79}/60°	60.1	$2.0\ 10^4$	90	$5.14\ 10^{-3}$
Br^{79}/49°	55.3	$3.1\ 10^4$	105	$5.12\ 10^{-3}$
Br^{79}/0°	35	$5.0\ 10^4$	60	$4.34\ 10^{-3}$
Cl^{35}/60°	25.4	$2.34\ 10^5$	66	$5.6\ 10^{-4}$
Cl^{35}/0°	12.7	$1.3\ 10^5$	110	$8.4\ 10^{-4}$
F^{19}/60°	8.4	$1.5\ 10^5$	6	$8.0\ 10^{-5}$
F^{19}/0°	<8	10^5	0	0

The threshold LET is about 8 $MeVmg^{-1}cm^2$, with a saturation cross-section of 5 10^{-3} cm^2. The measured threshold LET of 8 $MeVmg^{-1}cm^{-2}$ is sufficiently low for this ASIC to suffer latch-up caused by nuclear reactions induced by high-energy protons and neutrons.

A preliminary Monte-Carlo simulation has been performed using the GEANT package to estimate the radiation background inside ALICE, and this has indicated that a significant latch-up risk exists for this component. More simulation work is needed (with Fluka code) to calculate the spectrum of the radiation background for a more precise estimate of the latch-up rate. ALICE presently envisages two options to circumvent the latch-up risk: the implementation of a latch-up protection circuit (current limitation and de-latching circuit), or the redesign of the circuit using radiation tolerant design practices.

This example shows that all LHC detector teams should seriously evaluate their SEL risk. The risk of hardware failure (supply short-circuit) without protection is too risky to be neglected, and potentially concerns all standard components including COTS and standard ASICs.

7. Development of a radiation tolerant voltage regulator

Most of the sub detectors of the LHC experiments such as, trackers, calorimeters, muons systems and in-cavern electronics may require local powering of their electronic boards and detector modules in order to ensure clean and accurate low supply voltages. Unfortunately, there is no commercially available radiation tolerant voltage regulator with low drop out voltage characteristics, and with a specification suitable for the LHC experiments. In 1998, three important steps have been taken towards the development of a suitable voltage regulator. The three steps were the selection and characterization of a suitable radiation tolerant bipolar technology, the definition of the specification of the voltage regulator with the LHC collaborations, and the design of the voltage regulator under a contract with ST Microelectronics.

7.1 Radiation test of the technology for the voltage regulator

In 1997, the study of a standard power technology showed that it exhibited an insufficient level of radiation tolerance to be successfully used for developing our voltage regulator. In collaboration with ST Microelectronics, a new effort has been pursued to select a bipolar technology tolerant to radiation, and suitable for the development of a radiation tolerant voltage regulator. The bipolar technology selected, RHBip1, is based on the monolithic integration of complementary vertical high-speed NPN and PNP transistors. The radiation tolerance to displacement damage is achieved by using transistors with a thin base width, which is uncommon for a power technology. The radiation tolerance to total dose effects has been maximized by improving the oxide quality over the emitter-base depletion region. In addition, based on preliminary radiation tests performed last year, the use of lateral pnp transistors has been excluded from the design.

The RHBip1 technology [14] has a maximum operating voltage of 12 volts, a minimum emitter size of 5 microns, the current gain Hfe in the range of 100 before irradiation for both transistors types, and a transition frequency of 2.5GHz and 6GHz for the vertical PNP and NPN respectively. The technology is a double metal level process, with double poly layer and an additional high poly resistance, and metal-poly capacitors.

Elementary components of the technology have been tested up to a total dose of 500 Krad, and to a neutron fluence up to 2.10^{13} neutrons/cm^2. The low dose-rate enhancement effect has been also measured on power devices.

Bipolar devices were irradiated with emitter, base and collector connected to ground. It has been verified that these connections corresponds to the worse case conditions. X-ray irradiations were performed at two dose rates, 100 rad/s and 10 rad/s. Gamma irradiation with a ^{60}Co source was performed with a dose rate of 4 rad/s. The low dose rate test has been performed at 0.02 rad/s with the ^{60}Co facility of ESA-ESTEC.

A summary of the radiation effects, including total dose and displacement damage effects is shown in Figures 15 and 16 for the power PNP and the power NPN transistors respectively. Power transistors are usually the most sensitive devices to total dose and displacement damage effects. For a typical operating condition, of a collector current above 10 mA, the maximum degradation of the current gain is less than 15% both for PNP and NPN devices after a total dose of 500 krad. Displacement damage induced by a fluence of 10^{13} n/cm^2 is smaller than the degradation induced by this total dose. This result indicates a very good robustness of the technology against displacement damage, which is the dominant radiation effect for the voltage regulators placed in the outer regions of LHC experiments (calorimeters, muons and caverns).

The results of the low dose-rate measurement indicate that the degradation of the current gain characteristic is smaller than 10% between the test at a dose rate of 4 rad/s and the test at a dose rate of 0.02 rad/s. However, this result has been obtained with only 2 samples and should be considered as preliminary. Resistors have been also tested to total dose, and results show no significant degradation after 500 krad <3%).

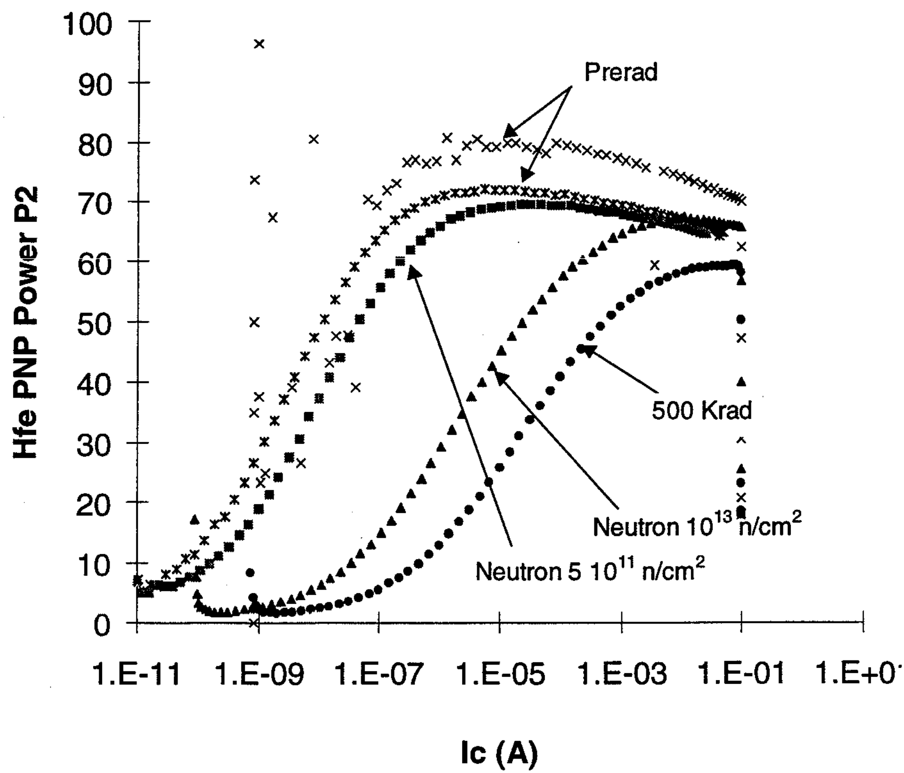

Figure 15 Degradation of the current gain characteristic of the power PNP transistor. Results are shown for total doses up to 500 krad, and for neutron fluences up to 10^{13} neutron/cm^2.

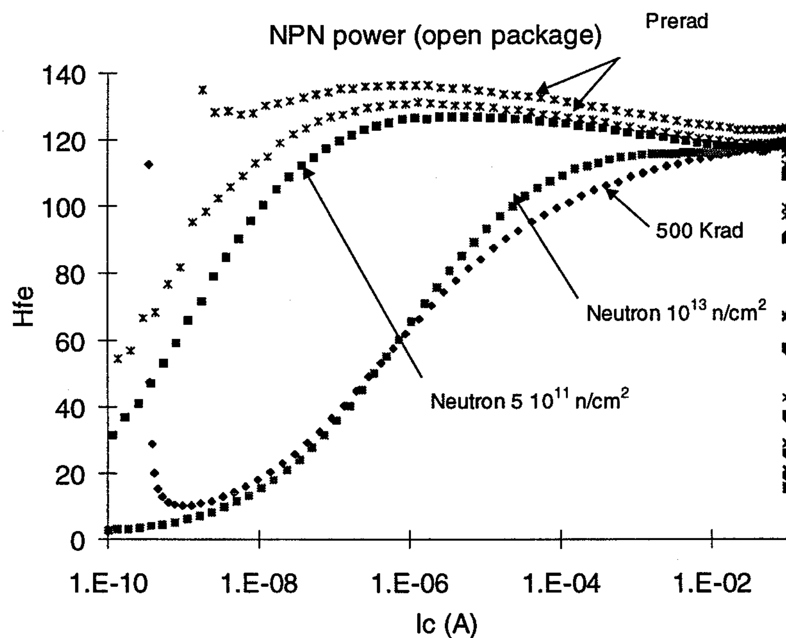

Figure 16 Degradation of the current gain characteristic of the power NPN transistor. Results are shown for total doses up to 500 krad, and for neutron fluences up to 10^{13} neutron/cm^2.

7.2 The rad-tolerant Voltage regulator

The radiation tolerant voltage regulator is based on the traditional series voltage regulator circuit. It consists of a reference voltage element, an error amplifier, and a series-pass element (ballast). Smart features have been included in the design to enable the remote monitoring and control of voltage regulators embedded in detector systems. Features are a remote sensing control, a digital signal output to monitor an over-current condition (OCM), and an inhibit input signal to switch off the regulator for de-latching electronic circuits. Standard protection features such as an over-temperature protection circuit are implemented to turn off the device and avoid damage in case of excessive junction temperature.

The circuit design of the voltage regulator has been especially conceived to enable operation with the minimum possible drop out voltage, which is particularly important to minimize the local power dissipation in powering modern VLSI circuits operating at low voltage supplies (3.3V, 2.5V). The maximum drop out voltage specification is 0.5 and 1.5 Volt respectively for 1 and 3A load current in the whole range of temperature.

Precautions in the design of the voltage regulator have been taken to minimize post-rad degradation and to preserve stable performance. A dedicated design and layout have been employed with a modification of standard design rules, in particular for spacing rules and biasing operating currents, in order to minimize post-rad leakage currents inside and between elementary devices.

The specification of the voltage regulator, established together with the LHC collaborations and agreed by ST Microelectronics, is a compromise between several different requirements. To cover a large fraction of the sub detector needs, several fixed output voltage values defined by 4 metal options have been foreseen (2.5, 3.3, 5, 8 Volt). In addition, another metal option is available for an adjustable output voltage from 1.25V to 10V. To allow the precise tuning of the current protection limit to the expected maximum current of the application the user can adjust the current limit from 1 to 4.5 A.

Several LHC sub detectors wish to have a higher maximum output current (>3A). Unfortunately, this has not been accepted by ST Microelectronics, a maximum power consumption of 5 W for a monolithic device for a small die of 4 mm^2 is the limit in order to keep the junction temperature within the operating limit.

Table 7 The basic specification of the voltage regulator

unless otherwise specified Vin=Vout+2.3V, Tj = 25°C, Ci = 0.1µF, Co = 10µF.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage accuracy	I_o=5mA, V_{in}=Vout+2V, 10°C<T_a<70°C	-2		2	%
V_o	Operating output Voltage	Io=3A 10°C<T_a<70°C	1.25		9.7	V
I_{out}	Output Current Limit	Adjustable from 1A to 4.5	1		4.5	A
$\Delta V_o/V_o$	Line regulation	Vout+1V<V_{in}<12V, I_o=5mA		1		%
$\Delta V_o/V_o$	Load regulation	V_{in}=Vout+1V, 5<I_o<3000mA		2		%
I_q	Quiescent current	Vout+2.3V<V_{in}<12V, ON mode				
		I_o=0mA		2		mA
				4.0	8	mA
		I_o=30mA		12	24	mA
		I_o=300mA		30	60	mA
		I_o=3A		50	110	mA
		V_{in} = Vout +2V, OFF mode		50		µA
SVR	Supply Voltage	V_{in}=Vout+2V ± 1V, Io=5mA				dB

	Rejection	f=120Hz		60		
		f=33KHz		30		
V_d	Dropout Voltage	I_o= 400 mA		0.25		V
		I_o= 1 A		0.5		
		I_o= 3 A		1.5		
		10°C<T_a<70°C				
V_{il}	Shutdown Control Input Logic Low	10°C<T<70°C			0.8	V
V_{ih}	Shutdown Control input Logic High	10°C<T<70°C	2			V
I_i	Shutdown Control Input Current	Vin=Vout+2, Vshutdown=6V		10		µA
C_o	Output Bypass Capacitance	ESR>=0.5Ω I_O = 0 to 1A		10(#)		µF
en	Output Noise Voltage(*) (10Hz to 100kHz) I=100mA				400	µV RMS
OCM	Over Current Monitor	Isink=24mA			0.36V	
DVo	Long Term Stability			25		mV/1000 Hr
Zout	Output impedance	100 mA DC 20mA rms Vout=5V		100		mOhm

8. Activities in the new Institute members of the collaboration

8.1 FERMI Lab (FNAL)

In 1998, a test chip was fabricated in the HP (Hewlett Packard) 0.5 µm process to study the inherent radiation tolerance of the process and the radiation tolerance that can be achieved when using enclosed transistors and guard rings. The test chip included:

- 15 standard and enclosed NMOS transistors with different sizes
- guarded and unguarded enclosed NMOS devices
- 1 PMOS device, standard and enclosed current mirrors
- Standard and enclosed differential pairs
- Standard and enclosed ring oscillators.

In addition, the chip had 10 different pixel cell designs, and a 1 x 20 pixel readout array.

Chips were exposed up to 1 Mrad using 6 MeV electrons. The threshold shifts were consistent with those found with other 0.5 µm processes. Enclosed NMOS devices exhibited somewhat smaller threshold shifts. Using enclosed devices and guard rings eliminated NMOS leakage current problems. There was no significant change in transconductance and subthreshold slope for 1 Mrad of radiation in the NMOS. There was no large difference between the performance of the same size standard and enclosed transistor current mirrors and ring oscillators either before or after radiation. A substantial change in differential pair current for both enclosed and standard transistors at 1 Mrad after annealing was observed. The cause is not yet understood. The PMOS devices were found to have larger parametric drift with radiation for Vth, Gm, and subthreshold slope than the enclosed NMOS transistors. This suggests that total dose tolerance of the HP

0.5 μm process may be limited by the PMOS device performance. SEU tests were not performed on this test chip.

FNAL Objectives for 1999

Based on SEU work carried out by RD49 collaborators last year, Fermi lab has undertaken a program to evaluate SEU for silicon strip readout chips used by the CDF and DO experiments at Fermi lab. Initial tests will be done on the SVX3 chip, which was built in the Honeywell 0.8 μm bulk CMOS process. Tests will be run in March 1999 using the University of California cyclotron. 60 MeV protons will be used for the test. Later tests may be performed using an ion beam to better understand Single Event Effects.

Fermilab has designed an 18 x 160 pixel readout chip using the HP 0.5 μm rad soft process. The current design is performing very well. In 1999 the design is expected to be moved to a 0.25 μm process utilizing enclosed and guarded NMOS transistors. After initial testing, the pixel readout chip will be irradiated and performance measured.

8.2 Montreal and Prague groups

Montreal in collaboration with Prague prepared during 1998 a program of studies on the interaction mechanisms of neutrons in silicon.

Montreal's and Prague's Objectives for 1999

For 1999 the proposal is to measure the occurrences, frequency and dependence on the neutron flux of SEE phenomena induced by neutrons hitting an electronic chip. To this end, the groups have to adapt existing system for neutron tagging at the Charles University Van de Graaff accelerator and for neutron induced reaction products spectroscopy. The occurrence of a SEE will be correlated with the presence of a neutron with known history [15]. The occurrence of SEE can be provoked by specific interactions of the neutrons with the silicon chip, such as (n,α), (n,p) and (n,n') reactions. In order to investigate these mechanisms, several comparative diodes of different sizes will be integrated on the chip [15]. The recorded pulse height distributions could indicate what types of reaction are taking place in the chip [16]. Pulse height distributions could also indicate a probability of the reaction per sensitive volume of the junction.

8.3 University of Rome II

1999 objectives: Characterization of VLSI circuits and COTS to total dose effects, and development of fault tolerant digital circuit architectures.

8.4 Brunel University

1999 objectives

1. To assist CERN in the formulation of COTS policy and guidelines for the application of COTS in the LHC and detector electronics. To advise on the selection and approval of COTS manufacturers including 'Best in Class' identification.
2. To assist CERN in defining the requirements for a COTS database and provide assistance in the setting up of such a database.
3. To provide advice and assistance, as required, to CERN staff and associates involved with COTS procurement.
4. To assist with the application of RADFET dosimetry for 'housekeeping' purposes in LHC and detector electronics, with a view to achieving a timely and efficient refurbishment plan compatible with maintenance plans for restricted access areas.

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