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DMILL, A Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Electronics

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Abstract

Particle detectors under preparation with the future LHC (Large Hadron Collider) require in their central trackers a fast, low noise, very rad-hard, mixed analog-digital microelectronics VLSI technology [3-4].

DMILL technology was developed between 1990 and 1995 by the CEA (French Atomic Energy Agency) for LHC and for applications in space and nuclear civilian industry. This technology was transfered between 1996 and 1998 in the 6'' silicon foundry of MHS (Nantes, France), an ATMEL company (USA). DMILL integrates mixed analog-digital very rad-hard (>10 Mrad and $>10^{14}$ neutron/cm^2) vertical bipolar, 0.8µm CMOS and 1.2 µm PJFET transistors on SOI substrate. At the end of June 1998, using the final DMILL process-flow, MHS completed the manufacture of several new batches dedicated to the Final Acceptance of the technology transfer. During summer 1998, the CEA and MHS carried out on these batches series of very thorough characterizations, whose results were entirely satisfactory. The compilation of these results with those from measurements made of all the preceding batches manufactured by MHS (43 batches were manufactured by MHS between spring 1996 and summer 1998) confirmed that all the parameters of the technology stabilized at MHS now fully satisfy the specifications based on the LHC requirements. These excellent results allowed the CEA to certify officially in September 98 the Final Acceptance of the industrial transfer and stabilization of DMILL at MHS [20].

DMILL is now a qualified process, manufactured and commercialized by MHS with a quality assurance, including radiation hardness and noise monitoring, which completely fulfils LHC requirements.

Numerous circuit developed since 1993 for the LHC by several laboratories with DMILL, show characteristics very close to their final objective [25-50]. Some of these circuits now fully comply with LHC detectors needs [35]. Various circuits are also under development for the space, nuclear civilian industry, and other applications.

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1. RECALLING OUR GOALS

The radiation hard microelectronics technologies that are now industrialized in the world were developed over the last 15 years for space or defense applications. They were designed for executing digital functions and for resistance to accumulated doses that do not exceed 1 Mrad for the most hardened technologies [1, 2].

The particle physics experiments which will be associated with the LHC require the use of VLSI *mixed analog-digital* microelectronics technologies which will have to resist, in the detector central sections, to ionizing doses exceeding *10 Mrads* accumulated over 10 years and to neutron fluences reaching 10^{14} n/cm^2 in 10 years [3, 4].

In addition, it appeared at the beginning of this decade that this type of technology was also required by the space industry for constructing medium hardened analog-digital circuits and by the civilian nuclear industry for very highly hardened analog-digital circuits. Medical instrumentation applications requiring slightly hardened analog-digital circuits have also been identified.

The objective of the DMILL program, which is now achieved, was to develop a mixed analog-digital technology, very highly hardened to ionizing radiation and to neutrons, capable of meeting all these requirements, and to make it industrially available not only for the High Energy Physics community but also for the space and civilian industries and other applications.

2. MAIN MILESTONES FROM R&D TO INDUSTRY

2.1. Origin and pre-industrial period [5-14]

2.1.1. Formation and carrying out of the DMILL program before its industrial transfer

At the beginning of 1990, engineers in the SEI Division of the CEA-DSM-DAPNIA[1] studied the preliminary proposals for the LHC experiments and realized that these necessitated a wide range of highly hardened electronics. They noted that there was no industrial solution that was really adapted to the LHC requirements anywhere in the world. This led them to the necessity of developing a new technology meeting these new requirements.

A market study made by the SEI also showed the need for highly hardened electronics in the civilian nuclear industry, hardened mixed analog-digital electronics in the space industry, as well as the CEA's other own requirements.

Contacts established in 1990 with the CEA-DTA-LETI[2] and the CEA-DAM[3] showed the SEI that there was an embryonic project for a rad-hard mixed analog-digital microelectronics technology. The SEI then proposed to form a consortium bringing together the three CEA's Directorates DSM, DAM and DTA-LETI for developing this technology in order to meet both the LHC requirements and those of the other industrial domains. The CEA management approved this project.

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[1] The CEA is the French Atomic Energy Agency ; the DSM is the Matter Science Directorate of the CEA, at Saclay ; the DAPNIA is the Department of Particle Physics, Astrophysics, Nuclear Physics and Associated Instrumentation of the CEA-DSM ; and the SEI is the Electronics and Computing Division of CEA-DSM-DAPNIA.

[2] The DTA is the Advanced Technologies Directorate of the CEA ; the LETI is the R&D microelectronics technologies laboratory of the CEA-DTA, at Grenoble.

[3] The DAM is the Military Application Directorate of the CEA, at Bruyères-le-Châtel.

From the start, the SEI, the project's prime contractor, has ensured that this development is associated with an industrial partner and carried out in close relationships with the LHC partner laboratories in order that the technology is correctly oriented.

In 1991, the CEA and the Thomson-TCS[4] company formed a consortium for the development and industrialization of DMILL[5] technology and signed an agreement defining the objectives, planning, fundings and human resources associated with this program.

At the start of 1992, to consolidate the forces required for the DMILL program, the CEA proposed to the IN2P3[6] laboratories of Marseille (CPPM) and Orsay (LAL) that they become associated with the development of this technology at the applications level. In May 1992, a consortium uniting the CEA, IN2P3 and Thomson-TCS presented DMILL for the first time to the DRDC[7] of CERN. CERN approved this project and made two recommendations: 1/ stabilize, then industrialize the DMILL technology; 2/ provide access to DMILL for the HEP community as soon as possible.

In 1993, due to the diversity and complexity of the work to be carried out, the CEA-IN2P3-TCS Consortium was reorganized by the vertical implementation of a Management Committee, a General and a Technical Coordination Committee and by horizontally distributing its forces in Working Groups covering all of the required actions for the development, stabilization and industrialization of the system. This new organization made possible and facilitated the circulation of information to the various decision-making proceedings for the DMILL program. It provided the required visibility and transparency for making concerted decisions. The same year, the Consortium updated the planning of development of the technology in taking account of the results already obtained and the foreseen plan for the LHC construction. The financial resources provided each year by the CEA partners remained identical to those decided in the initial formation of the Consortium.

In spite of numerous technical difficulties met in the 1992 - 1993 period, the results by the end of 1993 were sufficiently good to announce, in October 1993, before the CERN's DRDC Committee, the opening of the technology to the laboratories engaged in the development of circuits for the LHC. In December 1993, the DMILL Consortium organized a training course for facilitating access to the technology for the new users. At the start of 1994, the CEA organized the first MPW (Multi-Project-Wafer), which made possible the sharing the surface of a batch between numerous user Institutes. Due to the success of this first MPW at the laboratories, a second MPW batch was organized on the same principles in 1994; it was followed by three batches in 1995 and three other batches in 1996. Each of these MPW batches was accompanied by a backup batch started a few weeks later in order to avoid any technological failures. As requested by HEP laboratories, some of these back-up batches were used to correct design errors in the metal interconnections. Also as requested by certain laboratories, a few MPW batches were manufactured by an accelerated process. Between 1993 and 1996, 27 European, American and Japanese laboratories received the required tools and documentation for circuit designs. 21 of these designed and tested components or circuits manufactured with the 8 DMILL MPW batches. At the end of 1996, a number of architectures were close to their definitive version. Certain circuits reached 84 mm^2 and integrated up to 1 million transistors.

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[4] Thomson-TCS at Grenoble, France.
[5] In French: « Durci Mixte sur Isolant Logico-Linéaire » ; in English: « Rad-Hard Mixed Analog-Digital SOI ».
[6] The IN2P3 is the French National Institut for Particle Physics and Nuclear Physics, the CPPM is the Particle Physics Research Center of the IN2P3 at Marseille, and the LAL is the Linear Accelerator Laboratory of the IN2P3 at Orsay.
[7] Detector R&D Committee, the former LHC Electronics Board.

In parallel with this work, the Consortium followed a sustained information policy towards the Physics Community by presenting detailed progress reports of the project in 1993, 1995, 1997 and 1998 to CERN's DRDC and LEB Committees, by regularly reporting the DMILL Program advances in MUG[8] electronics seminars organized by CERN and by multiplying the presentations and communications in numerous international conferences [5-20]. These presentations contributed to tightening the links uniting the consortium and the HEP community and resulted, beyond this community, the initiation of developments of circuits for space and civilian nuclear industry applications.

2.1.2. Technical progression and stabilization of DMILL before its industrial transfer

The DMILL technology was constructed on the basis of knowledge acquired by the CEA-DAM, CEA-LETI and the Thomson-TCS during the decade 1980 - 1990 in the development and industrialization of preceding medium rad-hard (1 Mrad) digital microelectronics technologies.

DMILL started in 1988 by a feasibility study of a manufacturing process for analog circuits on an insulating substrate (SOI[9]) with components that were low-noise, rad-hard and capable of integration with logic elements. This feasibility study, started in collaboration by the CEA-DAM and CEA-LETI, made it possible to establish an initial process-flow for CMOS-compatible JFET transistors. The first structures were produced using mesa (silicon islands on SiO_2 insulator, obtained by gradient engraving of the surface silicon) technology in 1989 and gave encouraging results both from electrical and radiation viewpoints.

In spring 1990, the definition of a technology including three types of components, MOS, bipolar and JFET, was established. Each type of component was available in complementary N and P versions which led to a technology with 6 active components: NMOS, PMOS, NPN, PNP, N-JFET and P-JFET. The manufacture of the first batches integrating these 6 components was started in mid-1990, giving encouraging results in spite of numerous technological problems. The components were electrically functional but still imperfect and their hardening had to be optimized.

In 1991, LETI started the manufacture of new batches integrating all the corrections. These batches included complete circuits (microprocessors, operational amplifiers, OTAs, etc.), which were subsequently optimized and maintained in later batches for assessing performances of the technology in the development phases and then the industrial transfer. To accelerate the final development of the technology and in agreement with Thomson-TCS, it was decided to reduce the number of transistors from 6 to 4 and to keep only the NMOS, PMOS, NPN and P-JFET. This choice, whose pertinence had been verified with the designers, provided an appreciable simplification of the process-flow by reducing the number of stages.

1992 was the key year of the project: LETI decided in fact to go from the mesa technology, which was too specific, to a technology with insulation by vertical dielectric trenches. This evolution made possible the planar technology that is indispensable for the industrialization objective. This change resulted in a complete redefinition of the structures of each transistor accompanied by new design rules, soon followed by new simulation parameters.

At the start of 1993, from results obtained for batches for the development of the planar technology, the CEA and IN2P3 partners organized the first MPW batch inside the Consortium, in which they placed different study circuits and components. The components from this batch showed electrical properties and noise characteristics close to the targeted specifications; however,

[8] Microelectronics User Group organized by the CERN.
[9] Silicon On Insulator.

the hardness level of the MOS and bipolars, although respectable (> 1 Mrad), was still below the objectives. The OTA circuits showed electrical and noise characteristics close to those required for LHC type applications.

In 1993-1994, the CEA-DAM carried out, with the CEA-LETI, a major analysis of the connection between the fabrication process and the level of hardening to gamma-ray and neutron radiations. This work made it possible to obtain for batches, manufactured starting in 1994, a hardening level compatible with the objective of 10 Mrad and 10^{14} n/cm^2 required for the LHC experiments. At the end of 1993, the first results of this study, associated with the results obtained for the 1993 MPW, made it possible for the CEA to clearly identify the corrections to be made to the technology, and then to decide to provide access to the laboratories engaged in the construction of the LHC.

At the start of 1994, all of the acquired results and the maturity of the process made it possible to start the stabilization of the technology at LETI. The MPWs manufactured in 1994 and 1995 showed the robustness of the process-flow and provided all the required statistical data for the establishment of the industrial transfer files.

2.2. Industrial transfer and stabilization [15-20]

2.2.1. Organization and execution of the industrial transfer

In mid-1995, the DMILL technology was stabilized at LETI, it was thus time to undertake its transfer to industry. However, in 1994, due to problems of its own, Thomson-TCS withdrew from the Consortium. The CEA then entered into negotiations with several industrial companies interested by DMILL, which ended in mid-1995 with the selection of the MHS[10] company. The CEA and MHS signed, in September 1995, an industrial transfer agreement and DMILL operating license, in which MHS undertook to install this technology on its manufacturing line, to commercialize it and to maintain it in production until at least September 2005.

The main elements which led the CEA to select MHS are:

- MHS business: semiconductor foundry specialized in the production of hardened circuits ;
- MHS size which is well adapted to the market targeted by DMILL ;
- MHS interest in DMILL, not limited only to LHC applications, but also directed towards the space, civilian nuclear and defense industries ;
- *MHS aptitude for implementing DMILL on standard equipment of a manufacturing chain also used for numerous other technologies. Due to this, DMILL is entered, at MHS, in the mainstream of 0.8 µm technologies.*

The industrial transfer has required a new organization in which the CEA-DSM remains the prime contractor by being supported in this function by the DMILL Program Committee. This brings together at MHS the members of the Technical Management and the Operations Management and, at the CEA, the members of the former DMILL General Coordination Committee. This DMILL Program Committee meets every two to four months, or more frequently depending on the requirements.

[10] At this time, MHS, which is part of the TEMIC Group, was held by Lagardère (France) and by Daimler-Benz (Germany). MHS was purchased at the beginning of 1998 in totality by the US semiconductor manufacturer ATMEL. TEMIC/MHS is now the main center of expertise for ATMEL defence and space technologies. The MHS production plant is based in Nantes (France).

At the technical level, the CEA and MHS share the responsibilities as follows:

- LETI: transfer of knowledge concerning the elementary process-flow modules and the complete process-flow; assistance in the implementation of the elementary modules and the complete process-flow at MHS ;
- DAM: transfer of knowledge concerning the radiation hardness ; transfer of radiation hardness assurance procedures; assistance in obtaining at MHS the radiation hardness level obtained at LETI ;
- DSM: transfer of knowledge concerning noise of elementary transistors; transfer of noise monitoring; assistance in obtaining at MHS the low noise characteristics obtained at LETI ;
- MHS: Reproduction of individual modules; assembly and stabilization of the process-flow; implementation of quality assurance including radiation hardness assurance and noise monitoring procedures.

The industrial transfer and stabilization of DMILL at MHS was initially planned over 18 months (from October 1995 to April 1997). These operations were longer than foreseen due to a required apprenticeship period at MHS, which unlike Thomson-TCS, had not participated in the initial development of the technology.

In spring 1997, the stabilization of DMILL was, as noted in §.2.2.2, practically acquired: the obtained results were sufficiently good to allow MHS to open access to DMILL to the HEP community laboratories, so that they could continue and complete the development of their circuits before mass production. This anticipated opening was secured by MHS by its commitment to replace any non-conforming batch. However, in spring 1998, due to newly identified manufacturing yield problems and difficulties that MHS then had in manufacturing customer batches including bipolars with enough high pre-radiation and post-radiation gains, the CEA and MHS jointly decided to block all the customer batches until a process-flow that met all the specifications and was free from yield problems was obtained. This process-flow was finally obtained in June 1998; it made it possible to immediately restart the production of all the customer batches. These were completed in summer 1998 and were in complete conformity with the specifications.

At the end of June 1998, using the final DMILL process-flow, MHS completed the manufacture of several new batches dedicated to the Final Acceptance of the technology transfer. During summer 1998, the CEA and MHS carried out on these batches series of very thorough characterizations, whose results were entirely satisfactory. The compilation of these results with those from measurements made of all the preceding batches manufactured by MHS (43 batches were manufactured by MHS between spring 1996 and summer 1998) confirmed that all the parameters of the DMILL technology stabilized at MHS now fully satisfy the specifications based on the LHC requirements - specifications previously obtained for the technology stabilized at LETI.

These excellent results allowed the CEA to announce, during the September 1998 LEB Workshop at Rome, the Final Acceptance by the CEA of the industrial transfer and stabilization of DMILL at MHS.

The CEA and MHS partners are now undertaking the archiving of all the data relevant to the DMILL program.

2.2.2. Technical progression of the transfer and stabilization of DMILL at MHS

The reproduction of elementary modules, the manufacture and characterization of the first complete batches were carried out on the MHS 6" manufacturing line using an initial reticule containing the inspection patterns (technological test structures, individual transistors, different circuits including microprocessors, operational amplifiers and OTAs) which had been used for following the DMILL performances in its development and stabilization at LETI. The HPSALM[11] circuit, an analog memory developed for ATLAS calorimetry by the CEA and LAL in DMILL-LETI technology, was however not on this module. These first stages progressed as in the initial transfer planning.

The stabilization of the process-flow was carried out using a second reticule containing, in addition to the technological test structure, circuits and components of the first reticule, the acceptance circuit called DEMDSM (cf.§.4.5) [14, 51]. This is a self-testing derivative of the HPSALM circuit, developed for verifying the good adaptation of the DMILL technology to produce complete mixed analog-digital circuit for the LHC. The process-flow stabilization work, started in mid-1996, led, in end of spring 1997, to the control by MHS of practically all the parameters, with the exception of the following:

- too high resistivity and insufficient radiation hardness of the RSRHV high-value resistance (identified at end of 1997);
- pre-radiation and post-radiation gains of the bipolar frequently outside specifications ;
- insufficient Early voltage of the bipolar in some cases ;
- manufacturing yield problems identified at start of 1998, due to residual polysilicon filaments.

The RSRHV problem was solved in two ways: 1/ recentering of the resistivity, which resulted in an improvement of the radiation hardness; and 2/ addition of a new high-value resistance called Rextrins, significantly harder to radiations than RSRHV.

A major analysis was carried out by MHS, in collaboration with the CEA, to correct the bipolar gain and Early voltage. This work led in June 1998 to an Early voltage around 100 volts and a gain after 10 Mrad between 70 and 150 for Ic = 10 µA. Obtaining this gain at a low current after 10 Mrad was indispensable for guaranteeing a radiation hardness with respect to the *accumulated* effects of gamma rays (10 Mrads) *and* neutrons (10^{14} n/cm^2).

Finally, MHS identified the origin of the polysilicon filaments responsible for the insufficient manufacturing yield and made the corrections which then provided the normal yield.

The final acceptance of the DMILL transfer was decided by the CEA after compilation of all the exhaustive measurements made on all of the DMILL batches manufactured by MHS. The verification stages carried out by the CEA and MHS to decide this final acceptance are described and discussed in section 4.

3. RECALL OF THE TECHNOLOGICAL CHOICES.

DMILL uses an SOI substrate which significantly reduces the sensitivity of the circuits to transient irradiation effects such as parasitic currents or memory cell upsets [22-24] induced by the passage of single ionizing particles.

[11] HPSALM was developed in 1994 - 1995 in DMILL technology by Saclay and LAL for ATLAS liquid argon calorimeter. The improved version of this circuit is HAMAC, developed in DMILL technology by NEVIS, Saclay and LAL for the same detector.

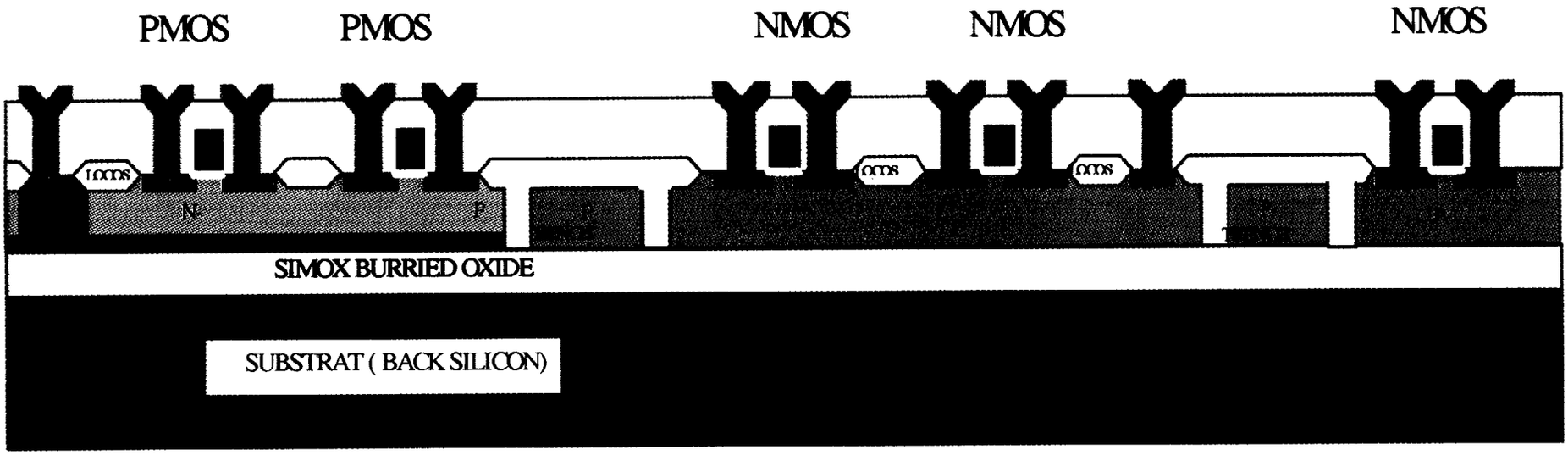

Fig. 1.a : Example of NMOS and PMOS cross sections.

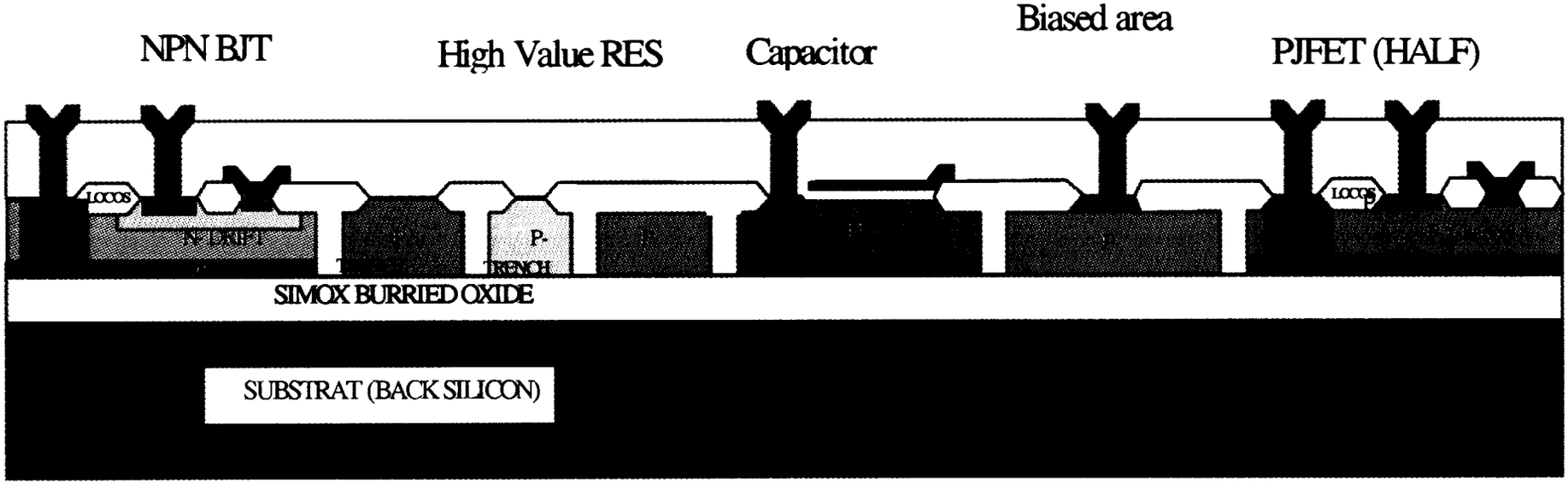

Fig. 1.b : Example of NPN, P-JFET, Capacitor and high value resistor cross sections.

The DMILL CMOS transistors are separated by a dielectric trench and by the buried oxide ; this dielectric insulation definitively eliminates any possibility of latch-up (triggering of a parasitic thyristor structure constitued by the juxtaposition of two complementary MOS transistors ; this phenomenon, initiated in standard technologies by the passage of single ionizing particles, results in circuit malfunctions and, in some cases, in their definitive destruction).

The 0.8-µm CMOS and the vertical bipolar transistor of DMILL provide the advantages of present BiCMOS technologies. The PJFET transistor is used for a number of low-noise or low-temperature applications.

The CMOS structure was designed to obtain very high hardness to total ionizing dose (> 10 Mrad) and a low noise level. This type of transistor, which uses majority carriers, is naturally hardened to neutrons.

The bipolar transistor uses a vertical structure which provides both high neutron hardness (> 1E14 n/cm2) and high speed operation. Its structure was also carefully optimized to obtain high hardness to ionizing radiation (> 10 Mrad).

The PJFET transistor, which uses majority carriers and whose intrinsic operation does not involve oxides, has low sensitivity to ionizing radiations and to neutrons. Its structure was optimized to obtain an extremely high hardness to these radiation types (>> 10 Mrad and > 1E14 n/cm2).

For analog applications, DMILL integrates two capacitor and two resistor families, both radiation hardened.

DMILL also integrates rad-hard anti-ESD devices, specifically designed for protection of either analog or digital circuits.

The interconnections can be made with two metal layers whose minimum dimensions are those of a 0.6-µm technology, and with a low resistivity polysilicon layer.

The design rules for the components and their interconnections were optimized to obtain a high integration density, which is comparable to that of present 0.8-µm non rad-hard pure-CMOS technologies.

Figures 1.a and 1.b. give schematic cross section of DMILL transistors, resistors and capacitors.

4. FINAL ACCEPTANCE OF THE INDUSTRIAL TRANSFER

The final acceptance of the industrial transfer is the last step foreseen in the contract signed by the CEA and MHS in 1995. This final acceptance is based on the results of extensive measurements made of several batches manufactured with the final process-flow, and on all the measurements made of all the previous MHS batches. The criterion used to analyse these results is the technical specification file, based on the complete set of measurements made on DMILL technology stabilized at LETI. The measurements and checking required to decide the final acceptance of the transfer are distributed in the 11 following steps :

1. Statistical Process Control (SPC);
2. Electrical parameters;
3. Radiation hardness;
4. Transistors and OTAs noise (pre-rad and post-rad);
5. Characterization and yield of demonstrator circuit ;
6. Characterization of anti-ESD devices ;

7. Electromigration tests ;
8. Hot carriers ageing tests ;
9. Oxide breakdown tests ;
10. Approval of the final process-flow ;
11. Approval of the final design kit.

In the following, all these measurements or checking steps are briefly described and the main results are summarized :

1. Statistical Process control.
SPC enables the verification and control of the critical technological parameters which govern the electrical, noise and radiation hardness characteristics. More than 120 parameters are measured during and after processing for each batch. All the SPC parameters obtained for batches made using the final process-flow are fully within the specifications.

2. Electrical parameters.
More than 90 electrical parameters are measured on several sites on each wafer, in each batch. All the parameters obtained for batches made using the final process-flow comply with the specifications. Figures 2 and 3 give an illustration of the stability of these parameters for successive batches, after initial adjustments made on the first batches.

LSL and USL are respectively the Lower Specified Limit and the Upper Specified Limit.

3. Radiation hardness.
The most sensitive static parameters of each active and passive device are measured before and after irradiation (10 Mrad, 1E14 n/cm2) ; values of the most significant of these for several batches are shown in figures 4 to 9 (arbitrary batch numbers are used in the X-axis).

For the bipolar transistor, to ensure that the final gain after 10 Mrad + 1E14 n/cm2 is sufficiently high, the specific minimum gain after 10 Mrad and before neutron irradiation is LSL@10Mrad = 70 (Ic = 10 µA). The left side of figure 7 corresponds to non optimized bipolars : the initial post-rad and pre-rad gains were below the specified values, respectively LSL@0rad and LSL@10Mrad. After several experiments, the difference between LETI and MHS equipment responsible for these insufficient gains was ascertained and the subsequent corrections gave the required pre-rad and post-rad gain, as shown in the right side of Fig.7 (final process-flow).

The new high value resistor R_{ext}, which was made available to users in Summer 1998, was also measured before and after 10 Mrad. This resistor has a high radiation hardness: $\Delta R_{ext}/R_{ext}$ = +6.5% after 10 Mrad.

It is not possible to describe all the results obtained in radiation hardness tests in this report. To summarize, here again all the values of the radiation hardness parameters measured on batches made using the final process-flow are within the specification limits.

4-a. Individual transistors noise.
Input noise spectral density is measured before and after irradiation on each type of transistor for various sizes and various biasing conditions [14]. Figures 10 to 17 show the pre-rad and post-rad noise spectral density ($nV/Hz^{1/2}$) versus Frequency (Hz) measured on the 4 types of DMILL transistors. The dotted lines correspond to the worst cases obtained with the stabilized DMILL-LETI process-flow. The noise spectral density measured on batches made with the stabilized DMILL-MHS process-flow is consistent with that measured on batches issued from the stabilized DMILL-LETI process-flow.

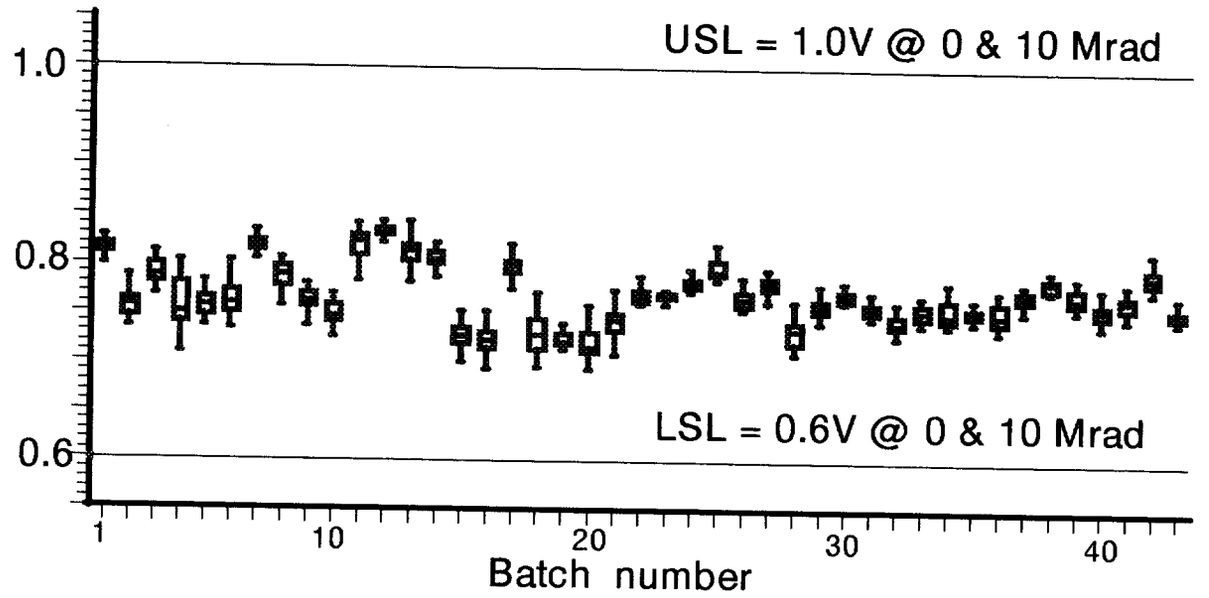

Fig.2 : NMOS Vt(V) versus batch number.

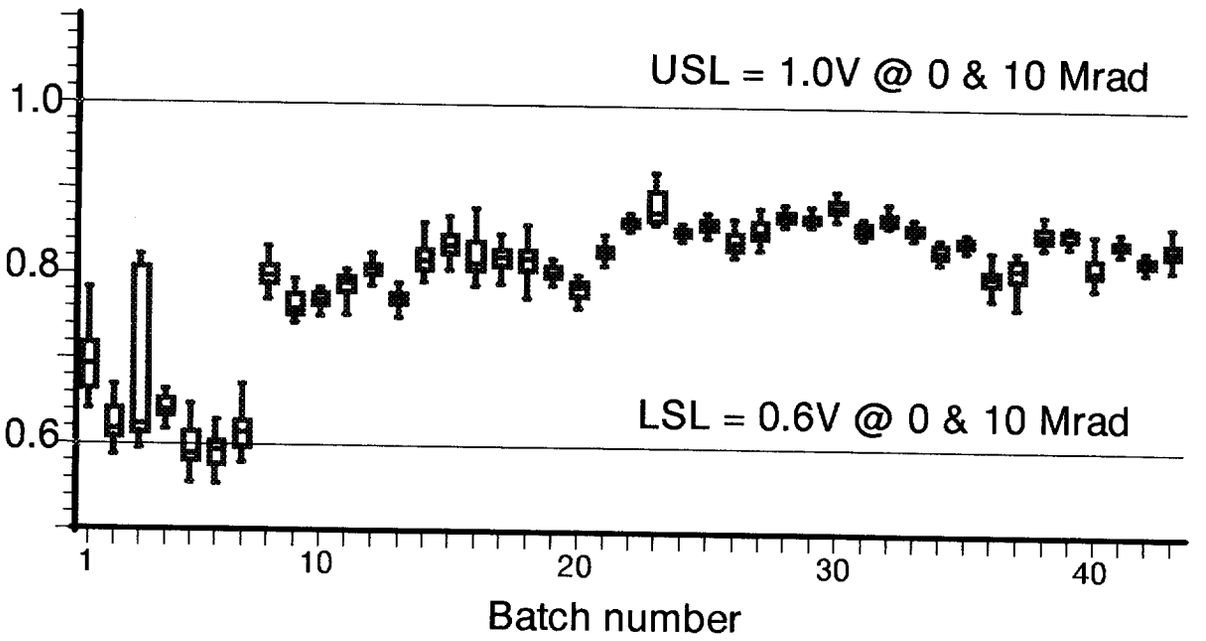

Fig.3 : PMOS |Vtl (V) versus batch number.

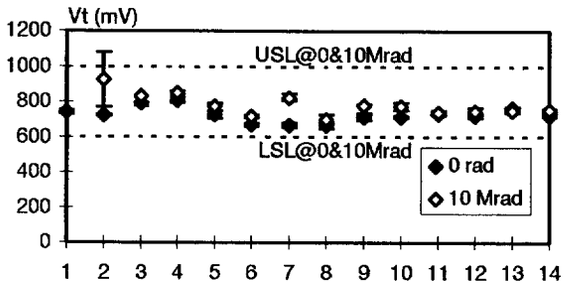

Fig.4. NMOS Vt(mV) versus batch number

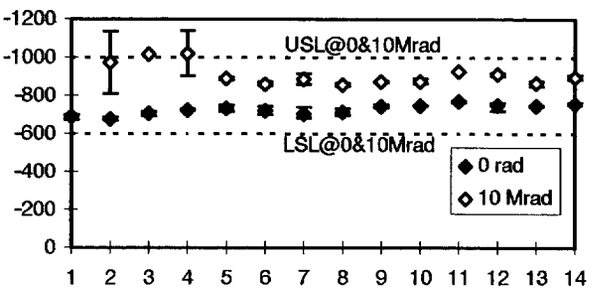

Fig.5. PMOS Vt(mV) versus batch number

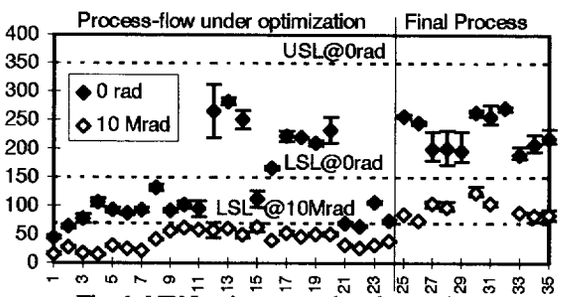

Fig.6. NPN gain versus batch number

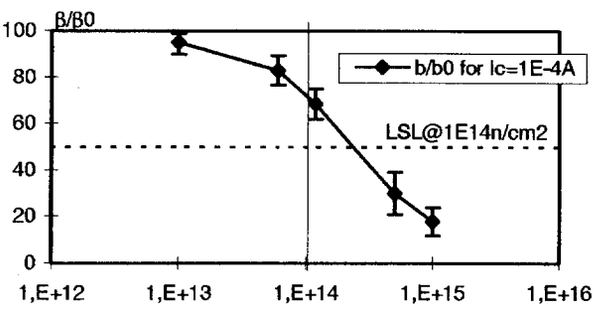

Fig.7. NPN β/β0 versus neutron fluence

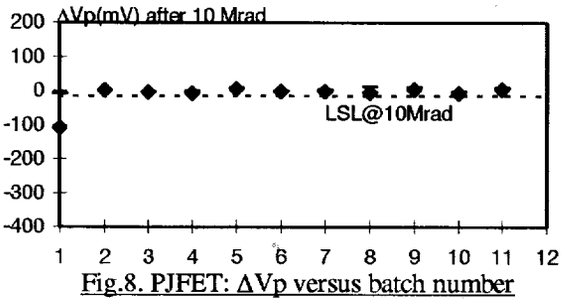

Fig.8. PJFET: ΔVp versus batch number

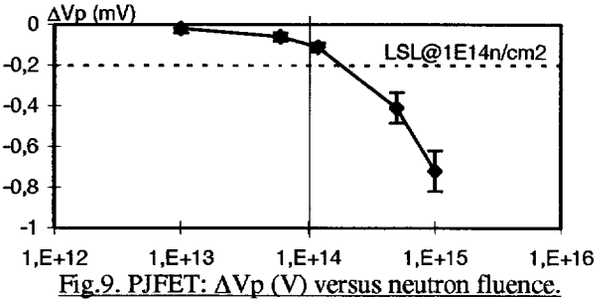

Fig.9. PJFET: ΔVp (V) versus neutron fluence.

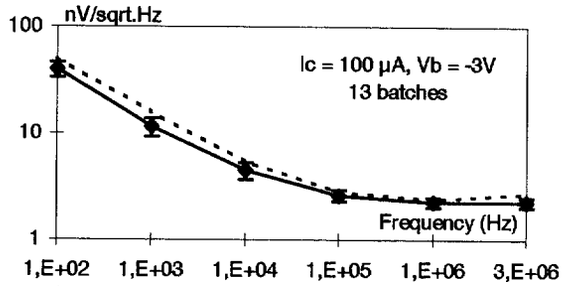

Fig.10: NMOS 5000/3, noise spectrum @0 rad

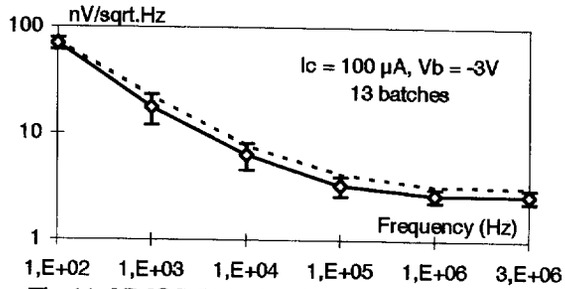

Fig.11: NMOS 5000/3 noise spectr. at 10 Mrad

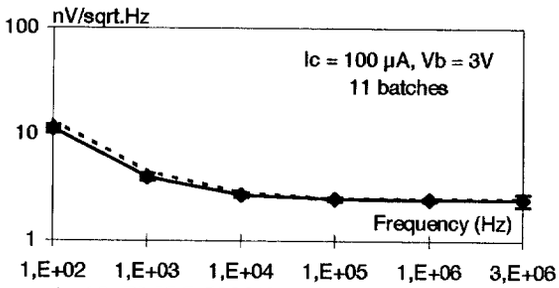

Fig.12: PMOS 5000/3, noise spectrum at 0 rad

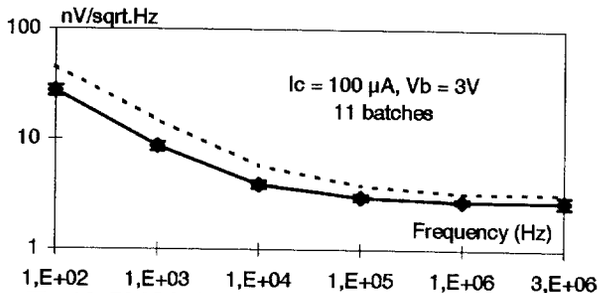

Fig.13. PMOS 5000/3, noise spectr. at 10 Mrad

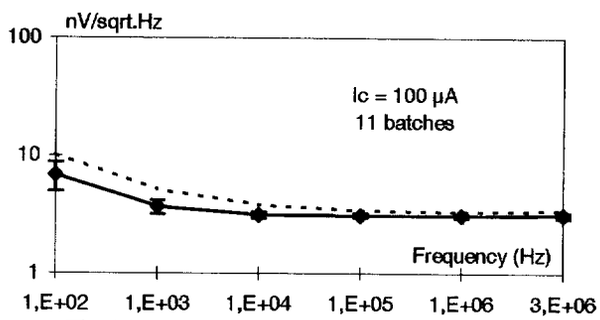

Fig.14. NPN 1.2x1.2 noise spectrum @ 0 rad

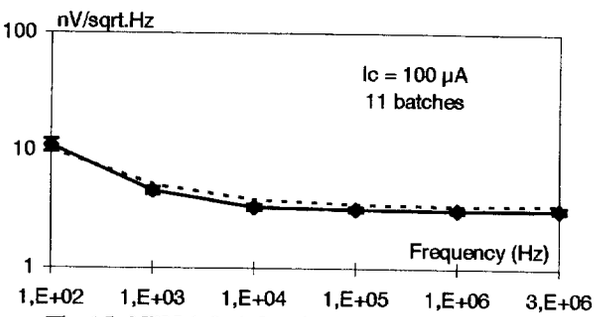

Fig.15. NPN 1.2x1.2 noise spectrum @ 10 Mrad

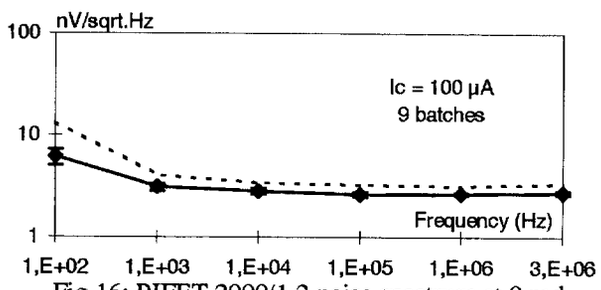

Fig.16: PJFET 2000/1.2 noise spectrum at 0 rad

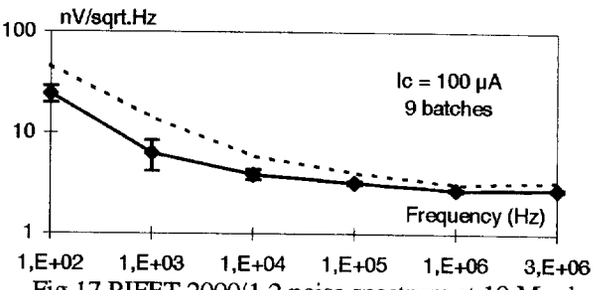

Fig.17 PJFET 2000/1.2 noise spectrum at 10 Mrad

4-b. Operational Transimpedance Amplifiers (OTAs) noise.
ENC[12] is measured on several OTAs designed with various input transistors (NMOS, PMOS, NPN and PJFET). Results obtained for batches from the final DMILL-MHS process-flow are fully consistent with those obtained for DMILL-LETI batches and with individual transistors noise measurements.

5. Characterization and yield of demonstrator circuits.
The goal of this step is to validate the technology by electrical characterization and yield measurement on a circuit as representative as possible of mixed analog-digital circuits developed for LHC applications. The demonstrator circuit DEMDSM (49,000 transistors, 28 mm2) [14, 51] used for this validation is constructed around a high dynamic range switched capacitor analog memory HPSALM initially developed for ATLAS calorimetry. Some extra-logic has been added to make it self-testable. Table I shows that the main characteristics of this circuit, manufactured using the final DMILL-MHS process-flow, are very similar to those obtained for the reference circuit made in 1995 using the DMILL-LETI stabilized process-flow. The typical yield obtained with this circuit manufactured with the final DMILL-MHS process-flow is about 60%.

Technology	**DMILL-LETI**	**DMILL-MHS**	**DMILL-MHS**
Total dose	0 rad	0 rad	10 Mrad
Max. Freq.	65 MHz	60 MHz	55 MHz
Consumption @40MHz	460 mW	420 mW	310 mW
Droop rate	20 mV/s	40 mV/s	260 mV/s

Table I.

6. Anti-ESD (Electro Static Discharges) devices.
Three families of rad-hard anti-ESD devices are available in DMILL : one for digital input, one for digital output, and one for analog input. Measurements based on the Human Body Model (HBM) show that these devices efficiently protect input or output pads up to 4000V.

7. Electromigration tests.
The goal of these tests is to assess the reliability of metal interconnections stressed by high current density. Their results are in conformity with MHS standards.

8. Hot carriers ageing tests.
The goal of these tests is to measure accelerated ageing of CMOS devices. Their results are in conformity with MHS standards.

9. Oxide breakdown tests.
The goal of these tests is to assess the reliability of CMOS gate oxide under a high electrical field. Their results are in conformity with MHS standards.

10. Approval of the final process-flow.
The DMILL-MHS process-flow is an exact copy of the initial DMILL-LETI process-flow, except for a few adaptations made to take into account certain specific features of the equipment used by MHS. These adaptations were studied by MHS in collaboration with the LETI in order to preserve the structure and properties of all the DMILL components. After an in-depth analysis of the final DMILL-MHS process-flow, the LETI found it to be in conformity with the initial DMILL-LETI process-flow and has approved it.

[12] Equivalent Noise Charge

11. Approval of the final design kit .

A new revision of the DMILL design kit (DDK) was completed by the CEA and MHS in summer 1998. It includes the following improvements :

- R_{ext} simulation parameters ;
- Extraction tools for R_{ext} ;
- Simulation parameters of the new NPN ;
- Extraction of buried oxide (BOX) capacitances ;
- Simulation of parasitic BOX capacitive couplings ;
- Guidelines for reducing the effects of these capacitive couplings;
- Device matching parameters.

Table 2 gives an excerpt of the matching parameters which illustrates the very good matching of the new R_{ext}. NPN and CMOS also exhibits good matching parameters. The values of sigma for the CMOS transistors are refered to transistors designed with a gate width W = 1 µm and a gate length L = 1 µm, and scale as $(WL)^{-1/2}$.

Device	Dose	Parameter	unit	sigma
R_{ext}	0 rad	resistance	%	0.24
R_{ext}	10 Mrad	resistance	%	0.22
NPN 1.2x10	0 rad	gain	%	4.0
NPN 1.2x10	0 rad	Vbe	mV	0.21
NMOS	0 rad	Vt	mV*µm	14.3
PMOS	0 rad	Vt	mV*µm	23.3

Table 2.

This new DDK is available immediately at MHS and will be available on CD-ROM via IMEC in November 1998.

5. QUALIFICATION AND QUALITY ASSURANCE

An initial qualification of DMILL technology was made by MHS in October 1997 [21]. To take into account the corrections made in the process from mid-1997 to mid-1998, an additional qualification was carried out by MHS in june 1998. DMILL is today a fully qualified MHS process.

The quality assurance performed by MHS for DMILL includes three procedures [18]:

1. The standard quality assurance procedures applied to each DMILL batch. These procedures are mainly based on the Statistical Process Control (SPC) tools, on the Process Traceability tools, and on the Control of Process Changes rules. These tools and rules are common to all MHS technologies.

2. The radiation hardness monitoring was specifically studied [17, 18] and developed by the CEA for DMILL, and transfered to MHS. This monitoring consists in ionizing irradiation and measurements made of test structures up to 10 Mrads using a 10-keV RX ARACOR irradiation machine, and in neutron radiation-hardness tests made on test structures through electrical measurements. These tests made on each batch enable MHS to guarantee that each delivered wafer has a radiation hardness of 10 Mrad and 1E14 n/cm2.

3. The noise monitoring was also specifically studied and developed by the CEA for DMILL and transfered to MHS. This monitoring consists in noise spectral measurements made before irradiation and after 10 Mrads on elementary test structures for various sizes and various biasing conditions [18]. These measurements made at least on three batches per year enable MHS to maintain the noise characteristics within the specified limits.

6. CONCLUSIONS

The DMILL rad-hard mixed analog-digital technology was developed between 1990 and 1995 by CEA with the collaboration of IN2P3, and transfered to TEMIC/MHS from 1996 to mid-1998. After stabilization of the process, series of thorough measurements made by the CEA and MHS show that all the parameters of DMILL stabilized at MHS completely fulfil the specifications. The compilation of these results together with those obtained for all the previous DMILL-MHS batches have enabled the CEA to certify officially in September 1998 the final acceptance of the industrial transfer and stabilization of DMILL at MHS.

DMILL is now a qualified process, manufactured and commercialized by MHS with a quality assurance, including radiation hardness and noise monitoring, which completely fulfils LHC requirements.

Numerous circuit developed since 1993 for the LHC by several laboratories with DMILL-LETI and then DMILL-MHS, give very satisfactory results which demonstrate the good adaptation of this technology to LHC applications [25-50]. Some of these circuits today fully complies with LHC detectors needs [35]. Various circuits are also under development for the space, nuclear civilian industry, and other applications. Recent tests made to evaluate the possibilities of DMILL for high temperature operations[13] also gave very good results which open new markets like automotive and oil industry for this technology.

7. ACKNOWLEDGEMENTS

We wish to thank all the laboratories of the HEP community which have contributed to the development of this technology by their circuit developments, by the studies they have made of this technology, and by their very usefull technical discussion and suggestions.
We especially wish to thank the CERN for the development of the first DMILL digital library.

We also are very gratefull to the following for the valuable assistance they provided in carrying out the DMILL-LETI MPWs in 1996 :

- IN2P3-CNRS (France) ;
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- CERN (Switzerland) ;
- University of Basel (Switzerland) ;
- Paul Scherrer Institut - PSI (Switzerland).

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