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SWITCHED MODE POWER AMPLIFIER WITH ACTIVE FILTER FOR LOW ENERGY CORRECTION MAGNETS

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Switched Mode Power Amplifier with Active Filter for Low Energy Correction Magnets

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Abstract

This paper presents a complete characterisation of a 400 W (± 40 V ± 10 A) switched mode power amplifier that will be employed in the area of particle accelerators. The results of the analysis of this converter have been verified in a 3U crate prototype built by CERN PS/PO [1].

1. Introduction

In particle accelerators, the beam trajectory is controlled by a precise magnetic field produced by a large number of dc magnets. These magnets require power supplies capable of providing smooth dc currents, with very little drift and low noise. To obtain fine tuning of the beam trajectory, low energy correction magnets are needed with a specification of 1000ppm. The correction field in these magnets could be either positive or negative, and so, bipolar power supplies are required. These converters have to provide smooth zero-crossing of the load current and fast response to generate the required current functions (300A/s).

Up to now, inefficient Class-AB Linear amplifiers have been powering these magnets. The maximum theoretical efficiency for a sinusoidal output to a resistive load is $\eta = \pi/4 = 78.5\%$. The practical upper limit is 70%. When driving a load with a power factor of 60^0 or more, the efficiency deteriorates to 55%. When high di/dt is required with inductive loads the disadvantage is even greater. Typical load is 3 Ω, 20 mH.

Still, the linear solution is valid as long as a high-bandwidth programmable unipolar AC/DC converter is added to feed the linear output so as to keep the voltage drop V_{ce} constant. If a ZVS (zero-voltage switching) topology is used for the AC/DC converter the most important source of high frequency noise is eliminated (classical Class D amplifiers are hard switching converters). Theoretically, with this scheme the maximum efficiency for a sinusoidal output to resistive load is for V_{ce} = 2 V and $V_{ac/dc}$= 42V:

$$\eta = \frac{1}{1 + \frac{4V_{ce}}{\pi\left(V_{ac/dc} - V_{ce}\right)}} = 94\% \qquad (1)$$

2. Structure and behaviour of the whole converter

The power converter is formed by a rectifier stage, a high frequency isolation section and a linear output stage that acts as an active filter. See Fig. 1.

The input section consists basically of four blocks: an RFI input filter, a non-controlled full-wave three-phase rectifier, a DC filter and an in-rush current limitation. The inductors and capacitors of the input section implement a low pass filter that help to satisfy the audio susceptibility specification with low voltage drop in the active filter.

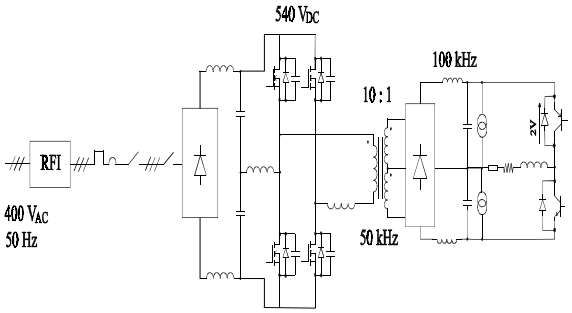

Fig. 1. *Bipolar ZVS Power Amplifier with Active Filter.*

The HF inverter section consists of a variation of the conventional zero-voltage-switched (ZVS) full-bridge converter [2] [3] with a positive and a negative output voltage. The introduction of soft-switching techniques is necessary in order to obtain a low noise operation. The operating frequency has been set to 50 kHz in order to trade off between losses, a reasonable size for the transformer and output filter and high reliability.

The linear output stage is a class A linear amplifier with a regulated voltage drop of 2 V. In this way, it is easy obtain a low output ripple, because this linear stage acts as an active filter, with relatively small losses. It also guarantees zero crossing without distortion.

3. ZVS DC/DC converter description

The diagram of this topology is shown in Fig. 2. ZVS is achieved in different ways in each one of the two legs. ZVS of leading leg switches (Q3-Q4) is achieved by using the stored energy in the output filter inductor. Therefore, we have ZVS in the leading leg switches for very wide ranges of the output current.

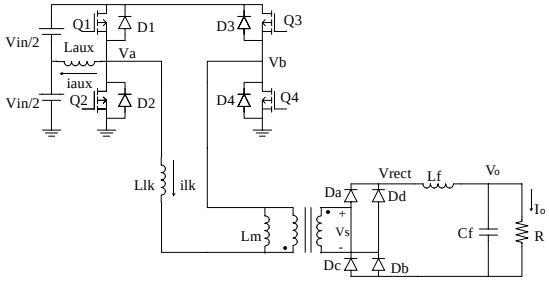

Fig. 2. *Full Bridge ZVS Converter with Auxiliary Inductor.*

However, ZVS of lagging leg switches (Q1-Q2) is achieved by using the resonant inductor added to the transformer leakage inductance (the addition is represented by L_{lk}) and an auxiliary inductor (L_{aux}). The current across the auxiliary inductor has a triangular waveform and aids the discharge of the output capacitors of the mosfets in each transition. L_{lk} and L_{aux} are selected to achieve ZVS transitions of the lagging leg above 60% load, with a maximum value of current across the auxiliary inductor of 60% primary current. In this way we obtain a low noise operation with relatively small losses in the auxiliary inductor.
Fig. 3 shows the typical waveforms of the converter. The operation is basically the same as for the normal ZVS. The only difference is that after t3 Q1 conducts current only when the current through the leakage inductance is bigger than the current through the auxiliary inductance.
An advantage is that the time to charge/discharge the output capacitors of the switches in the lagging leg is less than in a normal ZVS.
The study of the converter for the leading leg is exactly the same as that for the normal ZVS converter. There exist some differences, but only for the lagging leg, such as:

- Condition for Zero-Voltage Switching

$$\frac{1}{2}L_{lk}I_2^2 + \frac{1}{2}L_{aux}I_{apk}^2 \geq C_{MOS}V_{in}^2 \qquad (2)$$

- Dead time between Q1 and Q2

$$\tau_1 = \frac{T}{4} = \frac{\pi}{2}\sqrt{2C_{MOS}L_p} \qquad (3)$$

with $L_p = L_{lk} \,\|\, L_{aux}$

- Critical current for Zero-Voltage Switching

$$I_{crit} = \sqrt{\frac{2C_{MOS}V_{in}^2}{L_{lk}} - \frac{L_{aux}}{L_{lk}}I_{apk}^2} \qquad (4)$$

where I_2 is the current through the primary when Q1 turns off, I_{apk} is the current through the auxiliary inductance, Vin is the input voltage, L_p is the parallel between L_{lk} and L_{aux} and C_{MOS} is the output capacitor of the switch.

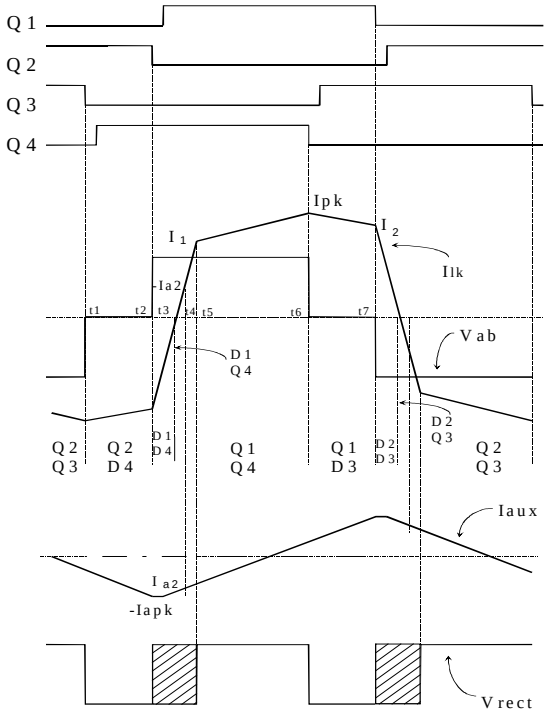

Fig. 3. *Typical waveforms of the converter.*

4. Design algorithm

The design algorithm has the following steps [1]:

1) Determination of the transformer turns ratio.

Inequality given in (5) can be used to obtain the transformer turns ratio:

$$n < \frac{V_{in,\min}}{V_0 + V_{s,drop}} \qquad (5)$$

where $V_{s,drop}$ is the voltage drop in the secondary rectifier diodes.

2) Auxiliary inductor current.

The maximum value of current across the auxiliary inductor (I_{apk}) is fixed at 60% primary current.

3) Determination of the equivalent inductance.

In equation (2) there are two unknown factors, L_{lk} and L_{aux}. In order to solve this equation, it can be supposed that, in an approximated numerical way, the parallel of the two inductors is fed with the sum of the two currents (I_2+I_{apk}) and $I_2 \cong I_{0,zvs}/n$ (without taking into account the magnetising current). To do this, a ZVS factor (F_{ZVS}) of 0.6 is fixed that provides us the value of $I_{0,ZVS}$. Equation (2) can be numerically approximated by:

$$\frac{1}{2} L_p \left(\frac{I_{0,ZVS}}{n} + I_{apk} \right)^2 \geq C_{MOS} V_{in}^2 \qquad (6)$$

and from this equation the value of L_p can be easily obtained:

$$L_p = 2 C_{mos} \left(\frac{V_{in,\max}}{\frac{I_{0ZVS}}{n} + I_{apk}} \right)^2 \qquad (7)$$

3) The delay time for the lagging leg is selected as follows:

$$t_d \leq \frac{\pi}{2} \sqrt{2 L_p C_{mos}} \qquad (8)$$

4)Choice of the operation frequency.

The maximum primary duty cycle is limited by t_d:

$$D_{\max} = 1 - 2 t_d f_s \qquad (9)$$

For the converter the primary duty cycle can be expressed as:

$$D = D_{eff} \left(1 + \frac{4 L_{lk} f_s}{n^2 R_0} \right) \qquad (10)$$

where $R_0 = \frac{V_{0\max}}{I_{0\max}}$ and $D_{eff} = n \frac{(V_0 + V_{s,drop})}{V_{in}}$

This value has to be lower than the maximum permissible value, $D < D_{\max}$, that is to say:

$$D_{eff} \left(1 + \frac{4 L_{lk} f_s}{n^2 R_0} \right) < 1 - 2 t_d f_s \qquad (11)$$

that gives us the following second order inequality in f_s:

$$16 n^2 R_0 t_d L_p I_{apk} f_s^2 - (8 L_p I_{apk} (1 - D_{eff}) n^2 R_0 + 2 n^2 R_0 t_d V_{in} + 4 L_p V_{in} D_{eff}) f_s + V_{in} (1 - D_{eff}) n^2 R_0 > 0 \qquad (12)$$

This inequality has two solutions. The frequency is selected with a value lower than the lowest of the two solutions for f_s.

4) Values of the auxiliary and leakage inductors.
The following equations have been used:

$$L_{aux} = \frac{V_{i\max}}{8 f_s I_{apk}} \qquad (13)$$

$$L_{lk} = \frac{L_p L_{aux}}{L_{aux} - L_p} \qquad (14)$$

5. Active filter description and regulation

Fig. 4 shows the implemented power amplifier. The amplifier has not been designed as an AB class because with this operation mode there would be continuous conduction which would produce higher losses. It is better to have a fast Class A amplifier with small voltage distortion considering that the inductive load will filter it out.

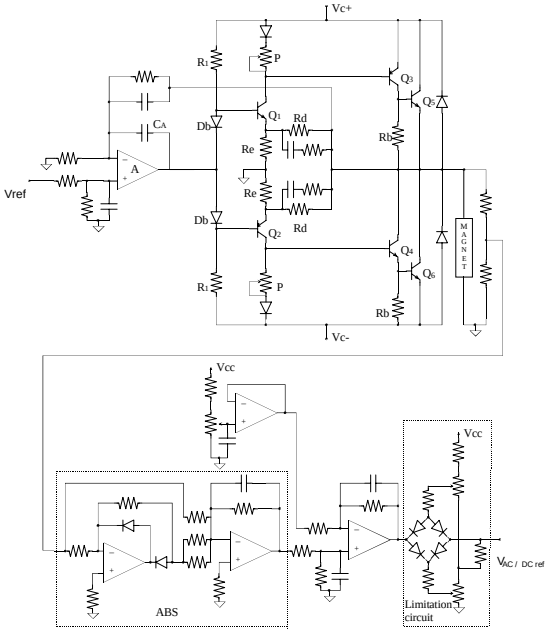

Fig. 4. *Active Filter.*

With Rd and Re, the voltage divider limits the stage gain to about 10. This limit is required for stability. The gain-bandwidth product available through the different driving stages (Q1/Q3/Q5) is quite high and not readily controllable. The local feedback reduces the gain-bandwidth product promoting stage stability.
The RC damping network across Rd provides heavy gain attenuation at very high frequencies, eliminating parasitic local loop oscillations in the MHz range.

Vc+ and Vc- are the outputs of the DC/DC power module and they can vary between 5 and 45 V. The linear output stage operates with a regulated voltage drop of 2 V and therefore the maximum value of the conduction losses is 20 W. In this way, it is easy to obtain a low output ripple, because this linear stage acts as an active filter, with low losses.
In the zero crossing, the output voltage of the DC/DC power module is maintained at 5 V while the output voltage of the linear stage varies its polarity. On the other hand, when a rapid change of the output voltage polarity takes place, the magnetic energy stored in the inductive load has to be absorbed. In this case, the linear output stage, that is placed before the load, is capable of dissipating this energy with a maximum power dissipation of 20 W.
The output voltage of the DC/DC power module has to be 2 V greater than the output voltage of the linear stage. The output voltage is measured to obtain the reference for the control of the DC/DC power module. As the output voltage can be positive or negative and a positive reference is needed, an absolute value circuit is used. It is necessary to add a voltage to the rectified output voltage to obtain the appropriated reference. This reference should never be lower than 1 V which corresponds to an output voltage of the DC/DC power module of 5 V. That it is the reason why the limitation circuit shown in Fig. 4 has been used.

6. DC/DC regulation. Average current control

Average current mode control (ACC)[4] has been used to regulate the converter. This method is easily applicable to a buck converter structure as is the case. The difference between ACC and the usual technique can be seen by examining Fig. 5.

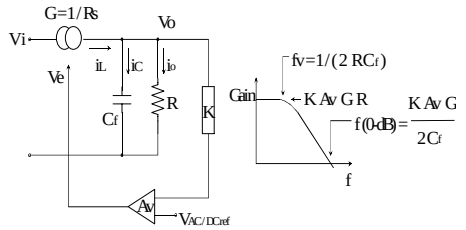

Fig. 5. *Conductance control.*

The main feature of ACC is the introduction of a current measurement (R_s) and a second error amplifier (A_c), forming an inner feedback loop, which controls the inductor current (i_L) as a direct function of the voltage error amplifier output signal (v_e). The elements shown inside the box in the figure represent the PWM conductance (A/V) module (G). In this way, we can consider the power stage as a voltage-controlled current source. This simplifies the control of the ZVS converter because the order of the system is reduced by one. Therefore, the dynamics is improved because the system has a first order behaviour. With this control method, it is easy to achieve a finer pulse to pulse modulation and also a greater value of the converter audio susceptibility than with the voltage control mode.
To maintain stability even at low load current when the output inductor enters into discontinuous mode, a current source of 200 mA has been added in each DC/DC output (see Fig. 1). At high load current, they are disconnected.

7. Precision current loop

A precision current loop, that provides the reference voltage to the active filter, has been added with the structure shown in Fig. 6.
HI = 1 V/A is the gain of the current loop (the voltage across the 50 mΩ shunt is amplified to obtain this gain).

$$Magnet = \frac{1}{R_M}\frac{1}{1+\tau_M\, s} \qquad (15)$$

with $\tau_M = \frac{L_M}{R_M}$.

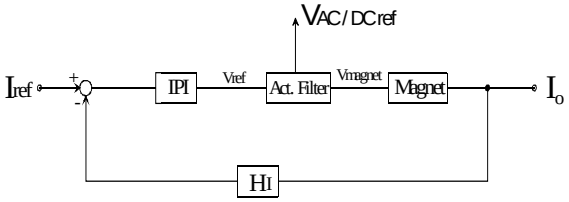

Fig. 6. *Precision current loop*

The power amplifier bandwidth is wider than that of the IPI, so we can suppose the power amplifier gain as a constant.
The open current loop gain is:

$$IPI \cdot Act\ \ Filter\ \cdot Magnet\ \cdot H_I \qquad (16)$$

To implement a first order system:

$$\frac{2\pi\, f_{CI}}{s} = IPI \cdot Act\ Filter \cdot Magnet \cdot H_I \qquad (17)$$

where f_{CI} is the bandwidth of the current loop. Therefore:

$$IPI = K\frac{1+\tau_M\, s}{s} \qquad (18)$$

with $K = \dfrac{2\pi\, f_{CI} R_M}{H_I \cdot Act\ Filter}$

8. Experimental results

Based on the design given in the previous sections, a prototype manufactured in a compact and modular 3U crate has been implemented and tested to verify the principle of operation.
Fig. 7 shows current and voltage in the primary and the voltage across the secondary for full-load operation.

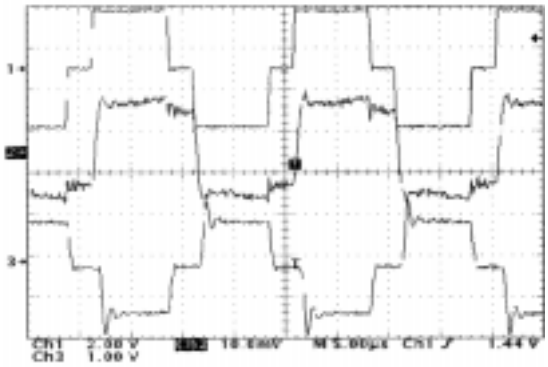

Fig. 7. Channel 1: Va - Vb (x200)
Channel 2: Primary current (1 A/div)
Channel 3: Secondary voltage (x50)

When the load current is decreased below 6 A, ZVS is lost in the lagging leg as predicted by the analysis [1]. Figs. 8 and 9 show the waveforms of the drain-source voltage of Q2 and the drain current for a load of 3.5 A and 6 A.
ZVS is lost in the leading leg when the current is decreased below 4.25 A. Figs. 10 and 11 show the waveforms for a load of 2.5 A and 4.25 A.

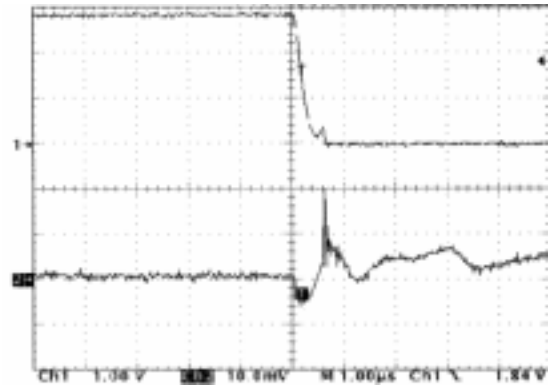

Fig. 8. Channel 1: V_{DS}(Q2) (x200) @3.5A
Channel 2: I_D(Q2) (500 mA/div) @3.5A

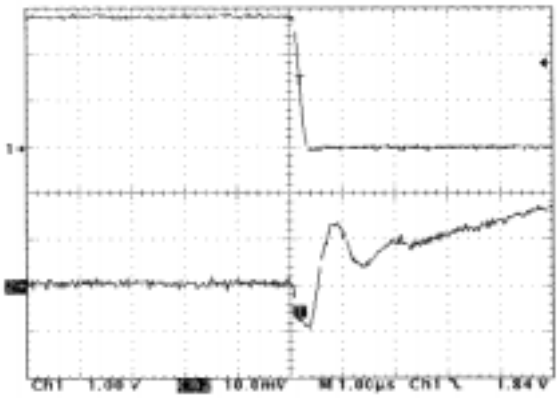

Fig. 9. Channel 1: V_{DS}(Q2) (x200) @6A
Channel 2: I_D(Q2) (500 mA/div) @6A

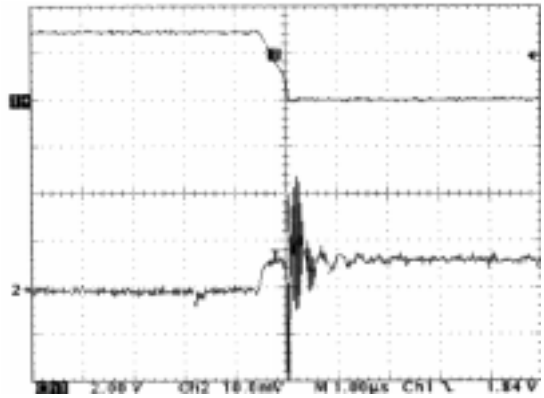

Fig. 10. Channel 1: V_{DS}(Q4) (x200)@2.5A
Channel 2: I_D(Q4) (200 mA/div) @2.5A

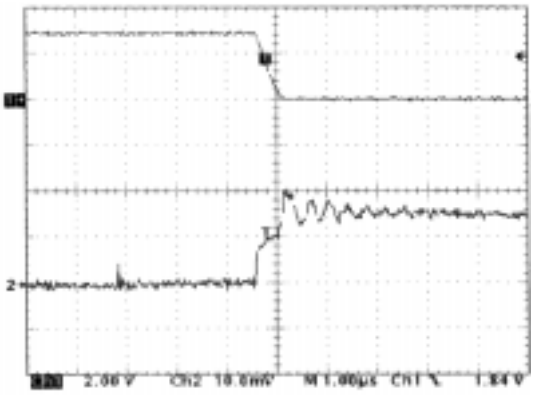

Fig. 11. Channel 1: V_{DS}(Q4) (x200)@4.25A
Channel 2: I_D(Q4) (200 mA/div) @4.25A

The whole system has an efficiency of 74% at full load decreasing to a value of 57% at 5 A of output current, that is between the limits determined by the specifications of the converter.
Fig. 12 shows the response of the system to a trapezoidal pulse of current between -10 A and 10 A with an slope of 300 A/s. The output current is indirectly measured by using a shunt of 0.1 Ω. Fig. 13 shows the detail of the zero crossing of the output current for an slope of 200 A/s. The delay of the output current against the reference voltage is defined by the IPI bandwidth.

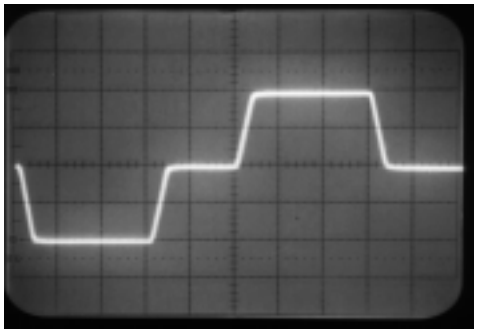

Fig. 12. Response of a trapezoidal pulse.
500 mV/div - 100 ms

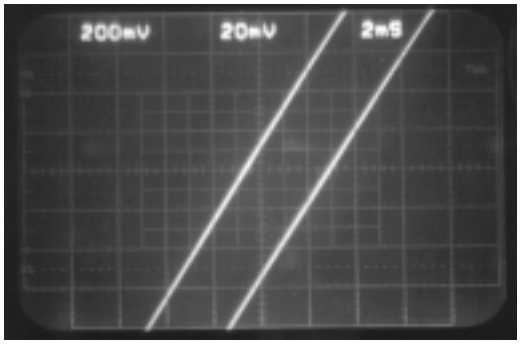

Fig. 13. Zero crossing.
Channel 1: Reference 200 mV/div - 2 ms
Channel 2: V_{shunt} 20 mV/div - 2 ms

The output current ripple is shown in Fig. 14, it is less than 1 mA (100ppm) at full load where the 540 V DC link ripple has a value of 2 Vpp at 300 Hz. Under these conditions, the active filter output ripple (at 300 Hz) has a value of 3 mVpp, that is to say, the system has an overall audio susceptibility of -56.5 dB.

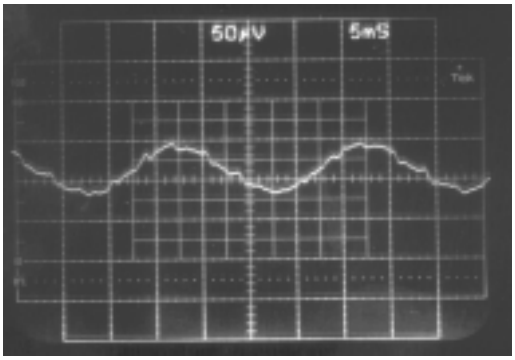

Fig. 14. Output current ripple.
V_{shunt} AC 50 µV/div - 5 ms

The different regulation loops have been designed for the following large signal (power) bandwidths: DC/DC voltage loop; 1 kHz, Active filter voltage loop; 500 Hz, Current loop; 50 Hz.
The system is capable of working with a current slope (dI/dt) greater than 300 A/s.

9. Conclusions

A complete study and design of a switched mode power amplifier is presented. The operation and behaviour features are illustrated and verified by the experimental results on a 400 W ($\pm$ 40 V $\pm$ 10 A) prototype. The main features of this system are:

- Low output current ripple (100ppm).

- Use of an auxiliary inductor that added to the resonant inductor allow ZVS transitions in the lagging leg of the high frequency isolation section, above 60% current load, without decreasing excessively the efficiency of the converter.

- Averaged current mode control, makes possible a greater large signal bandwidth and also a greater value of the converter audio susceptibility than with the voltage control mode.

- The use of soft switching techniques in the HF inverter section and a linear output stage allows a low noise and precise operation without zero crossing distortion, which are necessary in bipolar power supplies for correction magnets.

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[4] D. O’Sullivan, H. Spruyt and A. Crausaz, “PWM Conductance Control”, E.S.A. Journal 1989, Vol. 13.