CERN-LHCC-97-24

SCP

EUROPEAN ORGANISATION FOR NUCLEAR RESEARCH

CERN/LHCC 97-24
LEB P63 add.1
27 February 1997

# Addendum to P63 proposal for studying radiation tolerant ICs for LHC
## (radtol proposal)

F.Anghinolfi[13], G. Bonazzola[1], J. Casas[13], M. Campbell[13], P.L. Civera[2], P. O' Connor[3], W. Dabrowski[4], C.Dachs[12], C. Das[10], B. De Mey[10], P. Deremigis[1], F. Faccio[13], O. Flament[8], J. E. Da Franca[9], J. Gasiot[12], P. Giubellino[1], P. Gomes[13], E. Heijne[13]◊, P. Jarron[13]◊, J. Kaplon[13], K. Kloukinas[13], R. Klanner[6] , U. Koetz[7], J.L. Leray[8], C. Leme[9], M. Letheren[13], A. Marchioro[13], G.Mazza[1], O. Musseau[8] , A. Paccagnella[5]◊, J. Varela[6] , K. Hansen[7] , M. Labrunee[9] E. Pasero[2], F. Piuz[13], A. Rivetti[2], J.C Santiard[13], W. Snoeys[13], J. A. de Agapito Serrano[11], J. Vital[9]

1 University of Torino/INFN Italy

2 Politecnico di Torino Italy

3 BNL, Brookaven National Laboratory USA

4 Faculty of Physics and Nuclear Techniques, al. Mickiewicza 30, 30-059 Cracow, Poland

5 Universita di Padova/INFN Italy

6 LIP, Lisbon Portugal

7 Deutsches Elektronen Synchrotron DESY, Notkestr, 85 D-22603 Hambourg

8 CEA F-91680 Bruyeres le Chatel BP 12 France

9 IST Centre for Microsystems, Instituto Superior Tecnico, Torre Norte, Sala 9.12
Av. Rovisco Pais, 1 1096 Lisboa Codex, Portugal

10 IMEC Leuven Belgium

11 Departamento de Electronica, Facultad de Fisica. Universidad Complutense, Ciudad Universitaria, 28040 Madrid. Spain

12 Universite de Montpellier, CEM2 Unite de recherche 5507 CNRS-MEN France

13 CERN CH-1211 Geneva 23 Switzerland

◊Spokespersons

## Introduction

This addendum updates the P63 proposal following discussions with representatives of the LHC experiments and industrial partners. For the outer region of the LHC experiments, it clarifies the level of cost savings expected in the case of using radiation tolerant design, implemented on standard submicron CMOS processes instead of radiation hardened ASICs. The two primary goals of the radtol programme are to assess radiation tolerant design and layout techniques applicable to commercial submicron CMOS processes and make them available to LHC design teams, and to establish a close contact with Space agencies in order to profit from their experience in COTS.
The maps of radiation levels in LHC experiments indicate large variations of total dose and neutron fluence. One can identify 3 different categories for radiation tolerant ICs.

1. A low irradiation level corresponding to a total dose of few krad to 50krad and a fluence up to $2.10^{12}$n/cm$^2$ in 10 years of LHC operation. The detectors concerned are the ATLAS calorimeter, the TPC and outer detectors of ALICE and LHC-B, muons of all experiments and service electronics placed in the cavern.
2. A medium irradiation level corresponding to a total dose of 50 krad to 200 krad and a fluence up to $10^{13}$n/cm$^2$ in 10 years of LHC operation which covers the inner tracker of ALICE , and the H-cal of CMS.
3. A high irradiation level corresponding to a total dose of 200krad to 800 krad and a fluence up to $2.10^{13}$n/cm$^2$ in 10 years of LHC operation. The CMS ECAL electronics and some forward regions and trigger systems of all experiments are concerned by this irradiation level, which is close to the specification of radiation hard circuits.

Several readout chips are candidates for radiation tolerant design in standard commercial CMOS submicron processes, especially high density ASICs for complex digital processing functions. In addition to ASICs, several electronics instrumentation systems will require Commercial Off The Shelf (COTS) Ics.

Last month, the design team of the ATLAS Lq.Ar. calorimeter[1] has irradiated up to 2 $10^{12}$ neutrons/cm$^2$ a calibration module consisting of several commercial ICs. The module did not survive the irradiation test, and several ICs of the board were not functional after irradiation, especially voltage regulators and low offset voltage bipolar operational amplifiers. Burn-out of power regulator has also been observed in the DELPHI experiment This illustrates the risks associated to the use of COTS in LHC experiments.

Beside the total dose effect, single event effects such as latch up could also severely threaten the reliability of electronics systems in LHC experiments. NA50 has recently faced this problem[2]. The readout electronics of the silicon tracker, consisting of about 300 CMOS chips and 300 bipolar chips experienced a latch up every 2 hours during data taking. Because no automatic de-latcher circuit was implemented on detector modules, after detection of a high current (30 times the nominal consumption), the NA50 team manually switched-off and on power supplies to de-latch CMOS circuits.

---

[1] Private communication with C de la Taille.

[2] Private communication with P. Giubellino/Torino.

## Cost estimate of radiation tolerant and radiation hard circuits

The aim of the cost estimate is to give a picture of the cost benefit obtained in using radiation tolerant ASICs designed and fabricated in standard submicron CMOS processes. In order to make a cost comparison between radiation hard ASICs and rad tolerant ASICs, we have selected one vendor of a radiation hard process and one vendor of a submicron CMOS process, using the same wafer size of 6".
It must be noted that this cost estimate is approximate and reflects the actual semiconductor market, which evolves rapidly according to market pressures and technology advances, in particular for CMOS submicron processes. In addition, several factors entering in the cost estimate have been roughly estimated, in particular die size and yield. The three main factors entering in the cost estimate of Table 1 are die size, yield and number of manufactured wafers.

| | Rad hard process cost | | | 0.5µm CMOS process cost | | |
|---|---|---|---|---|---|---|
| #wafers | wafer KCHF | 25mm$^2$ die CHF | 50mm$^2$ die CHF | wafer KCHF | 25 mm$^2$ die CHF | 50mm$^2$ die CHF |
| 1 to 10 | 20 | 57 | 170 | 5.7 | 13 | 31 |
| 10 to 25 | 17 | 48 | 140 | 3.8 | 9 | 21 |
| 25 to 100 | 12 | 34 | 100 | 2.7 | 6 | 15 |
| 100 to 1000 | 8 | 22 | 67 | 2.0 | 5 | 11 |
| 1000 to 3000 | 5 | 15 | 42 | 1.6 | 3.5 | 9 |

**Table 1** Cost per wafer and cost per good die as a function of the number of wafers.The numbers in the table are indicative and not absolute. In particular, cost as function of the number of wafers is determined by commercial negociations, case by case. These costs do not include the cost of an engineering run (NRE).

*Assumptions for the cost estimate of radiation tolerant chips*
The cost estimate for rad tolerant chips manufactured in 0.5µm CMOS is based on a yield of 90% for a 25mm$^2$ die size and 75% for a 50mm$^2$ die size. For a 6" wafer we assume 250 x 50mm$^2$ dies, and 500 x 25mm$^2$ dies. After yield, this corresponds to 450 25mm$^2$ good dies and 185 50mm$^2$ good dies. The price estimate of an engineering run is 130KCHF, and for a MPC run it is 20 KCHF for a 25mm$^2$ die and 40KCHF for a 50mm$^2$ die.

*Assumptions for the cost estimate of radiation hard chips*
The cost estimate of rad hard chips manufactured in the rad hard process (order 1µm) is based on a yield of 70% for a 25mm$^2$ die and 45% for a 50mm$^2$ die. For a 6" wafer we assume 250 x 50mm$^2$ dies, and 500 x 25mm$^2$ dies. After yield, this corresponds to 350 25mm$^2$ good dies and 120 50mm$^2$ good dies. The price estimate of an engineering run is 230KCHF, and for a MPC it is 40 KCHF for a 25mm$^2$ die and 80KCHF for a 50mm$^2$ die.

This costing does not include any test on wafer and die, dicing, handling, bonding and mounting operations because we assume that these costs are in both cases. We also assume that a 0.5µm CMOS process with radiation tolerant design techniques has an identical size as a radiation hard chip.This can be explained by the fact that the higher device density of submicron process almost balances the increase of die area due to the larger layout of radiation tolerant devices. This assumption is based on a preliminary layout study of a pixel readout chip using rad tolerant design rules.

*Availability of commercial radiation tolerant processes*
Some semiconductor vendors intend to offer qualified radiation tolerant CMOS processes for total dose up to 200 krad. So far, we did not consider this option because these CMOS processes are proposed for analog circuits and not for the high density digital circuits which

are needed for radiation tolerant circuits at LHC. Furthermore, these processes will not be available before the middle of 1998. In addition, their cost benefit compared to radiation hard technology is only marginal, mainly because of their low volume production. Most of the design teams in ATLAS(muons), CMS (ECAL) and ALICE (inner tracker) plan to use standard submicron CMOS processes for their radiation tolerant chips in order to maximize the cost benefit.

## ASICs in LHC experiments

The tables 2, 3, 4 presented here concern the ASICs planned to be developed for the LHC experiments with radiation tolerant characteristics. These tables are not exhaustive and are based on the available specifications of the experiments and on the cost estimate presented in the previous section of this addendum. The columns *Devel. cost* (development cost), vol. cost (volume cost) and *Total cost* present cost estimates for radiation hard and submicron CMOS processes on the same line. The colum *Cost diff.* (cost difference) expresses the expected cost benefit obtained by the use of submicron CMOS processes.

| Detect | Chip count | Function | Devel.cost hard/tol KCHF | Vol. cost hard/tol KCHF | Total cost hard/tol KCHF/ MCHF | Cost diff. KCHF | # wafers hard/tol |
|---|---|---|---|---|---|---|---|
| Muons | | | | | | | |
| MDT | 40 000, | 8ch FE, 25mm$^2$ | 270/150 | 920/243 | 1170/393 | 777 | 115/90 |
| | 10 000 | TDC 50mm$^2$ | 310/170 | 996/150 | 1300/415 | 885 | 83/55 |
| CSC | 10 000 | 4ch CMOS FE | 270/150 | 360/62 | 630/212 | 420 | 30/23 |
| | 2500 | 16ch Ana. pipe 50mm$^2$ | 310/170 | 360/60 | 670/230 | 440 | 21/14 |
| RPC | 2500 | trigg. matrix 50mm$^2$ FE 25mm$^2$ | 310/170 | 175/40 | 670/230 | 440 | 21/14 |
| TGC | 200 000 | 4ch FE | 270/150 | 5.5M/0.9M | 5.7M/0.8M | 4.9M | 570/445 |
| | ? | trigg. matrix | | | | | |
| | ? | | | | | | |
| Liq Ar | | Analog FE :DMILL | | | | | |
| Cal | 4000 | Analog summation 50 | 310/170 | 396/90 | 700/260 | 440 | 33/22 |
| | ?COTS | Calibration:64 cards | | | | | |
| | 2000 | Fast digital link (1Gb/s) | | | | | |
| | ?COTS | ADC Analog Devices? | | | | | |
| | ? | TTC RX | ? | | | | |
| H-Cal | ? | FERMI design | ? | | | ? | |

**Table 2** Cost estimate of ATLAS rad tolerant ASICs.

The cost saving by using rad tolerant design for the ATLAS muons is 4.9 MCHF for the TGC and 2.96 MCHF for the muons electronics. For the Lq. Ar calorimeter it is 440 KCHF. Fast digital optical links, for which no existing rad hard or rad tolerant system exist, have been excluded from this cost estimate because there is no clear technology choice yet .

| Detector | Number | Function | Devel. cost hard/tol | Vol. cost hard/tol | Total cost hard/tol | Diff. cost | # of wafers |
|---|---|---|---|---|---|---|---|
| Pixel | 3000 | FE 2x50mm$^2$ | 310/170 | 600/90 | 910/260 | 650 | 50/33 |
| Si-Drift | 5000 | FE 50mm$^2$ | 310/170 | 500/75 | 810/245 | 565 | 42/27 |
| Tracker | 10000 | FE 50mm$^2$ | 310/170 | 1M/150 | 1.3M/320 | 1M | 84/54 |
| Pad-Rich | ? | | | | | | |
| TPC | 50 000<br>50 000 | 8chFE25mm$^2$<br>8ch ADC+dig | 270/150<br>270/150 | 1.15M/225<br>1.15M/225 | 1.4M/375<br>1.4M/375 | 1M<br>1M | 143/111<br>143/111 |

**Table 3** Cost estimate of ALICE rad tolerant ASICs.

The cost saving estimate for ALICE in the case of using rad tolerant ASICs should be of the order 4.2MCHF in total. Several subdetector are still missing in this estimate

| Detector | Number | Function | Devel. cost hard/tol | Vol. cost hard/tol | Total cost hard/tol | Diff. cost | # of wafer |
|---|---|---|---|---|---|---|---|
| Muons | | | | | | | |
| FE | 25 000 | Frontend 25mm$^2$ | 270/150 | 865/151 | 1130/480 | 650 | 72/56 |
| BTI | 50 000 | Trigger 25mm$^2$ | 270/150 | 1150/225 | 1420/375 | 1.04 | 144/112 |
| TRACO | 4 500 | Trigger 25mm$^2$ | 270/150 | 240/70 | 590/175 | 415 | 14/11 |
| TSS | 1 600 | Trigger 50mm$^2$ | 310/170 | 240/42 | 550/210 | 340 | 14/9 |
| TSM | 480 | ? | | | | | |
| TDC | 6 250 | Readout 50mm$^2$ | 310/170 | 624/100 | 930/270 | 660 | 52/34 |
| ROC | 1 600 | Readout 50mm$^2$ | 310/170 | 240/42 | 550/210 | 340 | 14/9 |
| ROS | 480 | readout 50mm$^2$ | | | | | |
| ECAL+ Hcal | | | | | | | |
| FPU | 150 000 | DMILL | _____ | _____ | _____ | ____ | |
| Preamp | 150 000 | DMILL | _____ | _____ | _____ | ____ | |
| ADC | COTS | ADC | _____ | _____ | _____ | ____ | |
| lineariser | 150 000 | Look-up+ 50mm$^2$. | 310/170 | 6.25M/1.6M | 6.5M/1.77M | 4.7 M | 1250/810 |
| pipeline | 150 000 | Pipeline 50mm$^2$ | 310/170 | 6.25M/1.6M | 6.5M/1.77M | 4.7 M | 1250/810 |
| Adder- | 25 000 | Trigger sum 50mm$^2$ | 310/170 | 1.6M/270 | 1.9M/440 | 1.5 M | 208/135 |
| Trigger | 25 000 | feature ext. 50mm$^2$ | 310/170 | 1.6M/270 | 1.9M/440 | 1.5 M | 208/135 |
| Filter1 | 25 000 | Back end 50mm$^2$ | 310/170 | 1.6M/270 | 1.9M/440 | 1.5 M | 208/135 |
| Filter2+RO C+CLM | 25 000 | Back end 50mm$^2$ | 310/170 | 1.6M/270 | 1.9M/440 | 1.5 M | 208/135 |
| VFCAL | | | | | | | |
| Fast Optolink | 15 000? | Data and Trigger trans | ? | ? | ? | ? | |

**Table 4** Cost estimate of CMS rad tolerant ASICs.

The cost saving estimate for CMS in case of rad tolerant ASICs should be 3.445MCHF for muons and about 15MCHF for the calorimeter. Fast digital optical links, for which no existing rad hard or rad tolerant system exist, have been excluded from this cost estimate because there is no clear technology choice yet .

## Availability of submicron CMOS processes and industrial partners

Semiconductor foundries are now currently running 0.5μm CMOS processes, and based on promising initial results[1,2] we have already obtained on test structures, we intend to complete the study in 97. In parallel, we plan to develop a prototype radiation tolerant chip for ALICE pixel detector, and a prototype chip for the ALICE TPC detector which consists of ADC and binary memory. The development of this type of radiation tolerant chip in 0.5μm CMOS is easily compatible with the present schedule of the LHC programme.
For high speed and high density digital circuits and pixel readout, deeper submicron CMOS technology would be beneficial. In large semiconductor foundries, 0.35μm CMOS processes are already in volume production, and 0.25μm will be available next year. We will receive soon from these semiconductor companies, free of charge, 0.35μm and 0.25μm samples to perform preliminary measurements of their radiation tolerance.
For the end of 1997, we propose the following 2 main milestones:

- assessement of the radiation tolerance of 0.5μm CMOS process, based on the results on specifically designed radiation tolerant test structures, and on the design and evaluation of prototype chips for the ALICE pixel and TPC detectors.
- preliminary study of the radiation tolerance of 0.35μm and 0.25μm CMOS test structures and decision on the choice of the technology and foundries.

For the year 1998, only 2 processes will be kept for the study, 0.5μm CMOS and one deep submicron, 0.35μm or 0.25μm CMOS selected according of their radiation tolerance performance.

## Ressources at CERN and the external collaborating institutes

The CERN MIC group has recently installed an automated test set up which can efficiently measure and irradiate with 10/20KeV X-ray, submicron CMOS samples. This automated testing system will perform very rapidly the series of tests and irradiations that we propose for the study of the radiation tolerance of submicron processes. In 1997, one CERN staff member would be in charge of the project (F. Faccio) with 2 students visitors from Uni of Padova and Uni of Torino and one visitor for 6 months from Uni of Montpellier, who is experienced in single event effects and power MOS burnout. Chip design will be carried out by MIC designers who are already committed to related projects (pixel and TPC-PAD ALICE).
The other tasks proposed in the radtol programme will mainly be supported by external institutes

- Time-temperature modelling and qualification protocol: CEA Bruyeres le Chatel, Uni of Montpellier and CNES/Toulouse.
- COTS: ESA and CNES.
- Latchup and SEU: CEA Bruyeres le Chatel, ESA, Uni of Montpellier and CNES/Toulouse,
- Development of radiation tolerant standard cells libraries: IMEC/Leuven
- Rad tolerant design technique, self calibration, error code correction: IST/Lisbon

## COTS issues

Following the discussions with ESA and CNES, it seems possible than CERN can have access to databases of COTS components existing in these Space agencies. ESA has also agreed (Len Adams) than in the framework of the RADTOL projects CERN representatives

could participate in meetings of the Space communiy related to the COTS issue and radiation tolerance of submicron CMOS technologies.

**Annex**

1 Radiation tolerant design using commercial VLSI technologies
2 Test of the radiation tolerance of two commercial submicron technologies

# Rad-Tolerant Design using commercial VLSI Technologies

*G. Anelli , F. Anghinolfi , M. Campbell, J. Christiansen, W. Dabrowski, F. Faccio, E.H.M. Heijne, P. Jarron, K. Kloukinas, M. Letheren, A. Marchioro, P.M. Signe, W. Snoeys*

*CERN, ECP-MIC*
*CH-1211 Geneva 23*
*Switzerland*

## Motivation and objectives

The electronics associated with the LHC detectors in both ATLAS and CMS experiments will be exposed to very high secondary particle fluxes from the proton beam collision. These fluxes, and therefore the total dose deposited, will change significantly as a function of the position in the detector. The requirements for the survival of the electronics in such an environment are different according to its actual installation, varying in terms of total dose from tens of Mrad (inner detector) to a few Krad. All the ICs will have to be latchup free and techniques to reduce the upset rate will have to be applied.

Due to the reduction of the defense market, the number of available radiation hard processes is decreased in the last few years. Some of those still existing are in fact one or more generation behind commercial technologies, not matching with the low power and high density needs of the complex circuit architectures planned to be used in LHC. Rad-Hard technologies developed for the military market also have a significantly higher cost than regular technologies, even comparing to more advanced commercial counterparts, and their future availability is sometimes doubtful.

An alternative approach to the radiation resistance problem is to take advantage of the reduction in gate oxide thickness which accompanies the scaling down of the device size in deep submicron technologies, and renders transistors naturally less sensitive to irradiation. Due to the impressive density of these modern processes, it is conceivable to implement layout techniques and architectures to harden the design to irradiation and still achieve higher density than with rad-hard processes. Better performance in terms of speed and low power could also be reached. Other significant benefits would come from the easy access, high reliability, high stability and lower cost of the commercial products. For all these reasons, even the space community is increasingly looking for COTS (Commercial Off The Shelf) components.

Objective of this work is the development of layout techniques to increase the radiation resistance of submicron VLSI technologies, and the evaluation of the maximum level of hardness achievable in different technologies by their application. The result of this study will tell if and in which regions of the experiments ICs manufactured in commercial technologies could be used in LHC.

## Methodology

The hole trapping in the gate oxide, which is responsible for the negative threshold shift of transistors during irradiation, decreases following a square law as a function of the oxide thickness. For oxide thickness less than about 10nm, the dependence becomes a $Tox^{-3}$. Therefore, thin gate oxides typically used in a submicron process experience almost negligible hole trapping. Moreover, the quality of the Si-SiO2 interface in such advanced technologies is very high, and the activation of interface states due to irradiation should be very limited. The overall threshold shift in a radiation environment does not seem to be of great concern, but in some technologies it can cause (coupled with the degradation of the sub-threshold slope) a small source-to-drain leakage current.

The hole trapping in lateral and field oxides, which are typically thick, is the main failure mechanism in commercial technologies. It is at the origin of leakage paths between n-

channel source and drain, neighbor n-channel transistors, and between ground and VDD biased diffusions. A careful layout of the transistors is effective in preventing the formation of these paths.

The source-to-drain leakage which occurs at the edge of the n-channel transistor (bird's beak) prevents it to be switched off, and this can happen already after a total dose as low as 20 Krad. The easiest way to solve this problem is to eliminate the edges, and this is possible by using edgeless n-channel transistors, like the one depicted in Figure 1. P-channel transistors do not need this care, as they typically do not have any leakage after irradiation.

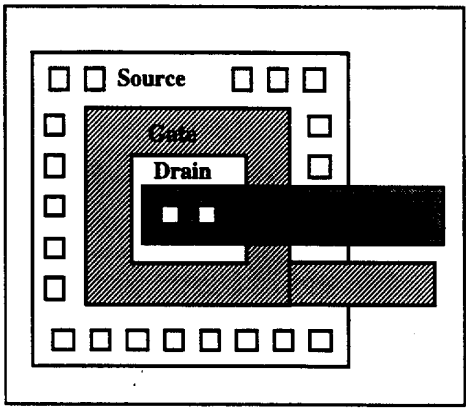


*Figure 1: Edgeless transistor*

The leakage paths that, under the field oxide, carry current between neighbors n-channel transistors and between different biased n+ diffusions (including the n-well) can be cut by the use of channel stops. All the n-channel transistors should so be surrounded by a p+ guard-ring.

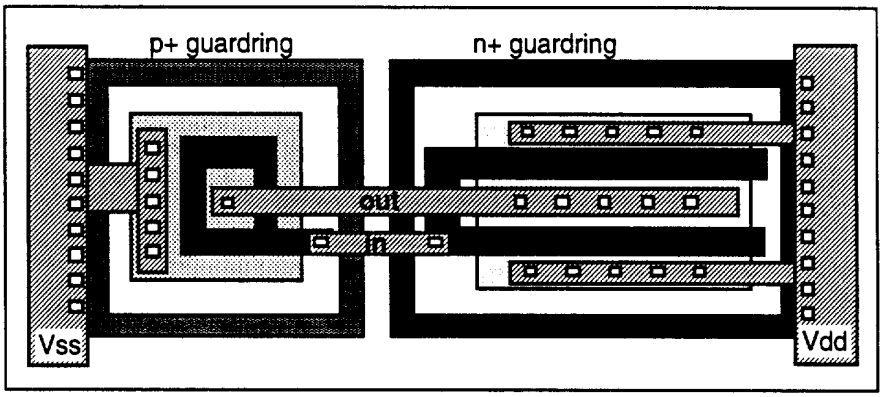


*Figure 2: Example of an inverter drawn using the techniques to reduce total dose effects and latchup.*

Channel stops around n-channel transistors can also be effective as guard-bands to decrease the latchup sensitivity. The use of n+ guard-bands around p-channel transistors is not useful

to reduce leakage, but the use of an n+ diffusion at the edge of the well increases further the latchup immunity. This happens because the n+ and p+ guard-bands keep the base potential of the bipolars responsible for the latchup at, respectively, VDD (well) and VSS (substrate). Moreover, they reduce the gain of any lateral surface PNP or NPN bipolar transistor.

As evident from Figure 2, the area penalty introduced by the use of complete guard-bands is high. Nevertheless, the use of deep submicron technologies in integrating such techniques can lead to ICs whose density is still higher than the one obtainable with available two generation older rad-hard processes.

## Technologies

A small change in a process step could result in a big change in the radiation response of the devices. Therefore, speed degradation, source-to-drain leakage due to interface states, SEU and SEL sensitivity could be different in different technologies. Moreover, the spacers used for LDD could have an important impact on the radiation response, and this is very technology dependent.

To have a significant comparison and understand which technology best fits our needs, the same structures, corrected for the specific design rules, should be integrated in a set of interesting commercial submicron technologies. Amongst those, the most advanced and attractive nowadays available is a 0.25 μm. Other technologies of interest are three 0.5 μm which are available, and a 0.35 μm which will be accessible soon.

Of course, the more information available on the specific process, the easier will be to evaluate its radiation resistance potential and, most of all, to interpret the measurement results. A list of information which should be asked from the manufacturers would be very useful in this respect and should possibly include the following:

- thickness of the epitaxial layer
- thickness and nature of the gate oxide (oxi-nitride?)
- lateral isolation technology
- composition of the metal layers (heavy metals ?)
- spacers technology
- information useful to study SEU with simulation codes (doping levels of substrate and well, thickness of the well, well technology, ...)

Some foundry might not agree to give details about all this, but at least a general idea of the basic technological steps of the process would already be precious. Moreover, it is crucial to know whether some change occurs in the technology after the qualification procedure has been completed. Even a small modification which do not affect the pre-irradiation transistor behaviour could change significantly the radiation response. These modifications tend to happen without any notice to the customers, and could represent a big risk for radiation tolerant applications.

## Test structures

The structures to be implemented in a test chip should be able to give complete overview on the effectiveness of the hardening techniques applied in each specific technology. The essential parameters to monitor at the transistor level are:

- threshold shift
- subthreshold slope
- source-to-drain leakage
- leakage between neighbor transistors
- junction leakage
- mobility degradation, hence transconductance
- noise
- matching

At the cell level, it is interesting to monitor the transition time and the propagation delay, together with the latchup sensitivity.

To be able to get answers in all these issues, the list of the test structures should include:

**n- and p-channel elemental transistors integrated with standard layout.**
The aim of these structures is to give an idea of the natural tolerance of the technology without applying any specific hardening technique: it is useful to know the actual starting radiation resistance. n-channel transistors should be arranged close to each other to monitor transistor-to-transistor leakage.

The n-channel structures are used also as a reference for the behavior of the less-known edgeless transistors, and to evaluate their effective W. Therefore the same gate length should be used in the normal and edgeless L-arrays. For all these reasons, the following standard transistors are needed:

- 3 n-channel: W=10 μm, L=5 μm, minimum size and slightly more than minimum size
- 3 p-channel: W=10 μm, L=5 μm, minimum size and slightly more than minimum size

**n-channel edgeless transistors with channel stops**
Each transistor is surrounded by a p+ channel stop. Measurement of its effectiveness in stopping the leakage between neighbor transistors and between transistors and n-well have to be possible (some of the edgeless transistors should have separate source contact and an n-well should be at minimum distance from the p+ guard-ring). The effectiveness of the edgeless structure against source-to-drain leakage for different gate length is investigated with these structures. As the edgeless transistors behavior is not well known, at least a couple

of matching pairs should be included. This increases the number of edgeless transistors to be integrated in the test chip, to a minimum of 6:

- 4 different gatelengths (drain minimum area, so the W is determined by the L), starting from minimum size up to 5 μm; 2 of these transistors are repeated to study the matching. For example, for a 0.5μm technology, the following L should be chosen: 0.5, 0.7 (2 identical transistors), 1.5, 5 (2 identical transistors).

**Field transistors**
These structures, made up of two n+ diffusions and a polysilicon or metal_1 gate between them, are useful to measure the field leakage after irradiation. The gate length of the field transistors should be the minimum allowed by the design rules, for a W of 10 μm. 2 of such transistors should be integrated, with polysilicon and metal1 gate respectively.

**Transistors for noise measurement**
One n-channel and one p-channel transistors aimed to measure the noise should be integrated. The size of such devices is: W=2000 μm, L = slightly more than minimum. The n-channel is layed out without edges and with full channel stop around it.

**Ring oscillators**
They are used to measure the timing and its change with irradiation. Moreover, they can be used to monitor the latchup sensitivity of a design (in both standard and hardened layout) in the studied technology. To do so, the VDD of each ring oscillator has to be separated from all the others. Each oscillator is made up of 51 basic elements, and the following oscillators are required:

- INVERTER chain, hardened layout
- NAND chain, hardened layout, where each NAND has its 2 inputs short circuited
- NOR chain, hardened layout, where each NOR has its 2 inputs short circuited
- NAND chain, standard layout (in aim to compare)

The output buffer, made of a chain of 4 inverters, should be made with hardened layout as well in all cases, and should have a separate VDD (but all the output buffers can have a common VDD).

**Shift register**
A shift register made up of master-slave flip-flops can be useful to assess the behavior of clocked circuits, and eventually used for single event upset tests. All the n-channel transistors have to be design-hardened.

## Work programme

### Integration phase

During this phase, the test vehicles containing the above listed structures will be integrated in a number of accessible submicron technologies. This activity starts in November 1996, the first test chips are foreseen to be delivered to CERN around March 1997. Hopefully, by summer 1997 the test vehicles in all the interesting technologies will have been delivered.

### Measurement phase:

This phase will begin around April 1997, and will go on until the autumn of the same year. It will consist in the full characterization of the test chips, their irradiation with an X-ray and $^{60}Co$ irradiation source with consequent new characterization. An high temperature annealing on the test chips will follow (100° C for 168 hours), after which they will be fully measured again. If possible, test at an heavy ion beam facility will be part of the measurement phase and will give useful information concerning latchup sensitivity.

This calendar does not prevent from submitting before autumn 1997 other circuits in the studied technologies and using the hardened design rules. On the contrary, it is recommended the integration of both analog and digital building blocks of growing complexity as soon as the first experimental feedback will come from the measurements.

X Federico

# Test of the radiation tolerance of two commercial submicron technologies

**G. Anelli, F. Faccio, E. Heijne, P. Jarron, W. Snoeys**
**CERN - ECP Division**

## Introduction

While there is appropriate emphasis on the introduction of special radiation-hardened technologies in particle physics, several considerations make it useful to study a complementary or maybe even alternative approach. The most important reasons for using commercial, submicron technology are the considerable cost advantage and better availability. This certainly triggered the similar interest in the military and space communities for Commercial-Off-The-Shelf (COTS) devices. A positive factor is the reduction of some adverse effects, e.g. threshold shift, if the oxide thickness is reduced and technology dimensions reach the 0.5 to 0.1 μm domain. A denser layout may allow the use of design solutions for improvement of radiation performance, while an additional advantage is the implementation of several (3-5) contact metal layers, not generally available in the 'less sophisticated' radiation-hard technologies.

## Description of the work

Several transistors of the Mietec 0.7μm and 0.5μm technologies have been irradiated up to two different total doses, 1 Mrad and 3 Mrad, and the evolution of the static parameters of the devices has been measured. The devices measured were kindly provided by Mietec, and we tested mainly transistors and couples of matched transistors. For some N-channel devices of the 0.7μm technology the worst case bias conditions were applied (that is maximum electric field across the gate oxide), and these devices showed an important shift of the threshold voltage and high leakage after irradiation. In general, the leakage current was a problem for N-channel devices and therefore some edgeless structures have been designed in the Mietec 0.7μm technology and tested; the first results show that these devices have low leakage after irradiation. More work is needed however, to understand the large parameter spread from chip to chip. The threshold voltage shifts were more important for the 0.7μm than for the 0.5μm, as expected for the thinner oxide of the latter technology, and for the transistors irradiated under

worst case bias the shifts reached 600mV. The other parameters like transconductance and subthreshold slope were degraded but not causing concern. In the following sections we give a summary of the measurements results. We did not yet carry out noise measurements.

## Threshold voltage shifts

The W of the transistors measured was comprised between 10 and 50μm, the L between 20 and 0.5μm. The threshold voltage was extracted from the intersection with the X-axis of the line fitting tangentially the curve of the drain current versus the gate voltage in the linear region (Vds=50mV). Table 1 summarises the results. All the shifts, as expected, were negative, and no significant variation between the different transistors was found.

| ABSOLUTE VALUE OF THE THRESHOLD VOLTAGE SHIFTS | | | | |
|---|---|---|---|---|
| **Technology and kind of bias** | **Kind of transistor** | **Total dose** | **Shifts for normal transistors** | **Shifts for matched transistors** |
| 0.5μm normal bias | N-channel | 1 Mrad | ~ 60 mV | ~ 50 mV |
| | N-channel | 3 Mrad | ~ 100 mV | ~ 90 mV |
| | P-channel | 1 Mrad | ~ 80 mV | ~ 100 mV |
| | P-channel | 3 Mrad | ~ 155 mV | ~ 165 mV |
| 0.7μm normal bias | N-channel | 1 Mrad | 285-415 mV | 220-250 mV |
| | N-channel | 3 Mrad | ~ 420 mV | 230-300 mV |
| | P-channel | 1 Mrad | 200-220 mV | 220-230 mV |
| | P-channel | 3 Mrad | 310-370 mV | 260-270 mV |
| | P-channel low $V_T$ | 1 Mrad | 170-250 mV | 390-400 mV |
| | P-channel low $V_T$ | 3 Mrad | 190-340 mV | 350-360 mV |
| 0.7μm worst case | N-channel | 1 Mrad | ~ 300 mV | ------- |
| | N-channel | 3 Mrad | ~ 600 mV | ------- |

**Table 1:** Threshold voltage shifts of N and P-channel devices of the two technologies for different bias conditions and total doses

We believe that the accuracy of our measurements is sufficient, and though we do not have large statistics, we have not observed significant matching degradation of the matched pair after irradiation.

Figure 1 shows the circuit we used to bias the N-channel transistors. The complementary circuit is used for the P-channel. For the worst case bias of the N-channel, we kept the source, substrate and drain at zero V and the gate at $V_{DD}$. Figure 2 shows the evolution of the drain

voltage of an N-channel device during irradiation and during three weeks of annealing at room temperature. The drain voltage is strictly related to the threshold voltage. A first order expression for $V_T$ holds: $V_T = V_D-(B-A\cdot V_D)^{1/2}$, where $A=2/\beta\cdot R$ and $B=A\cdot V_{DD}$. The value of the square root in the expression changes very little after irradiation compared to the linear term: assuming $\beta$ constant during irradiation (the maximum degradation found was 20% after 3 Mrad), and taking its average value ($\beta$=0.0041) before and after irradiation to calculate A and B, for the device measured we have $A=1.1\cdot10^{-2}$ and $B=5.6\cdot10^{-2}$. So the square root in the previous formula varies of only 11mV from before to after irradiation, while $V_D$ varies by 430mV. This means that the curve in figure 2 showing the drain voltage evolution is roughly the threshold voltage evolution shifted in the vertical direction by around 220mV. The 3 Mrad total dose was reached in 65 hours. It is interesting to note the quasi logarithmic shape of the plot during the annealing, and that after 1 Mrad the 90% of the change had already happened, indicating a saturation effect at higher doses.

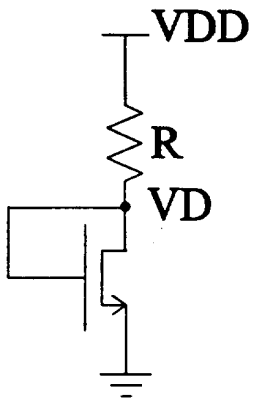


**Figure 1**

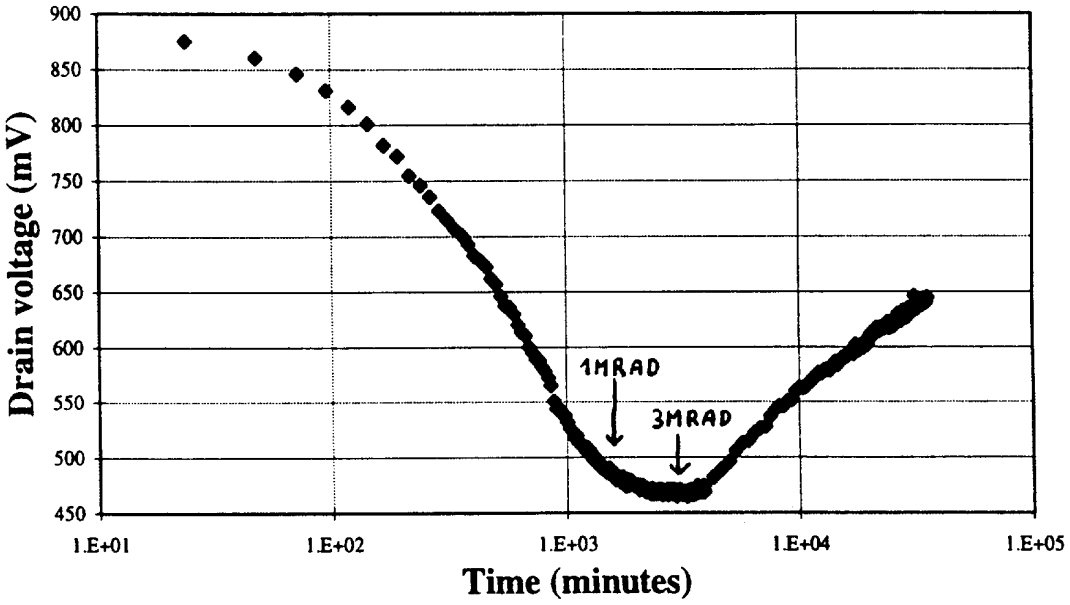


**Figure 2:** Drain voltage versus time (in logarithmic scale) during irradiation and annealing

## Mobility and transconductance

The mobility degradation (i.e. transconductance) is summarised in table 2. Figure 3 shows an example for an N-channel device: the transconductance was calculated from the measurement of the drain current as a function of the gate voltage with a fixed Vds value (600mV). The

transistor was still in saturation. The curve after irradiation goes up to higher currents because we kept the same voltage sweep for both measurements while the transistor threshold was lower after irradiation.

| Technology | Device type | Mobility degradation |
|---|---|---|
| 0.7μm | N-channel | 5-20% |
| | P-channel normal and low Vt | 5-15% |
| 0.5μm | N-channel | 5-15% |
| | P-channel | <5% |

**Table 2:** Mobility degradation for N and P channel devices of the two technologies tested

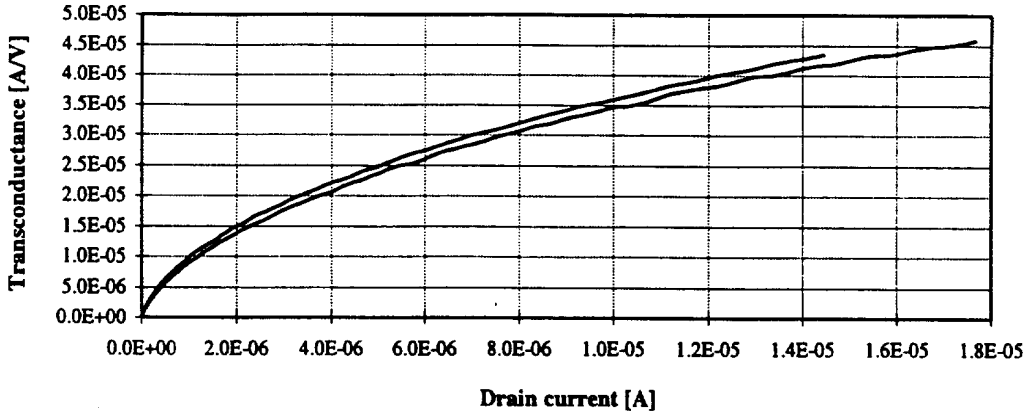


**Figure 3:** Transconductance as a function of the drain current for a N-channel device of the 0.7μm technology before irradiation and after 1Mrad

## Leakage currents

The problem of increased leakage currents[1] after irradiation in N-channel devices is ascribed to the turning-on of a parasitic transistor at the bird's beak or in the field because of positive charge being trapped in the oxide. Other contributing effects are the change of the threshold towards the depletion mode, and the degradation of the subthreshold slope. In figure 4 it is possible to note all these effects. The two plots show the drain current versus the gate voltage in the linear region (i.e., Vds=50mV) before and after

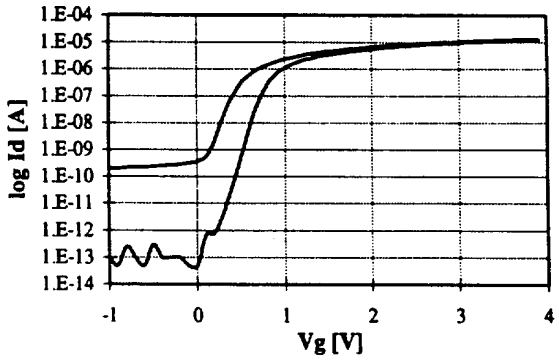


**Figure 4:** Subthreshold currents before irradiation (lower curve) and after 1 Mrad. Vds=50mV

[1] Leakage current is the current flowing through the drain contact, measured with gate, source and substrate contacts at 0V.

irradiation. In the plot after irradiation one can note the "plateau" for Vg between -1 and 0V: this could be due to the turning on of the parasitic transistor at the bird's beak. We tried to look for the threshold of this parasitic transistor, but we did not find it down to -8V (figure 5). So, either the threshold is lower in value, or the leakage current does not flow at the bird's beak but rather under the field oxide, escaping from the control of the gate.

For each transistor the leakage current was measured sweeping the drain voltage from 0 to 3.5 V for the 0.5µm and 7 V for the 0.7µm. For each transistor we generated two graphs, one plot shows the drain current versus the gate voltage in the linear region before and after irradiation, the other shows the leakage current after irradiation as a function of the drain voltage. The leakage current values given are for the highest drain bias applied (3.5V for 0.5µm and 7V for the 0.7µm.

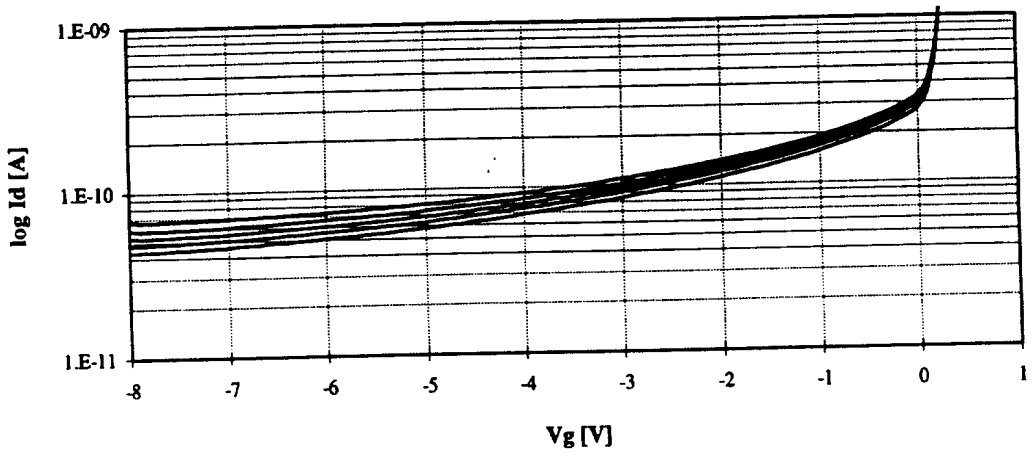


**Figure 5:** Subthreshold currents for Vds from 1 to 5V after 1 Mrad of the same device of figure 4. The threshold voltage of the hypothetical parasitic transistor is still not visible

For the 0.5µm, all the technology samples were biased with roughly the same voltage on gate and drain, not in the worst case (Vg varying from 0.9 to 1.1V). The first two values are concerning two devices of the same dimensions. From the results there seems not to be a relationship between the dimensions of the devices, the total dose and the value of the leakage. The leakage currents were always less than 400pA, except for 3 cases, in which the values were 124nA, 26nA and 1nA. Figure 6 and 7 show the worst case found.

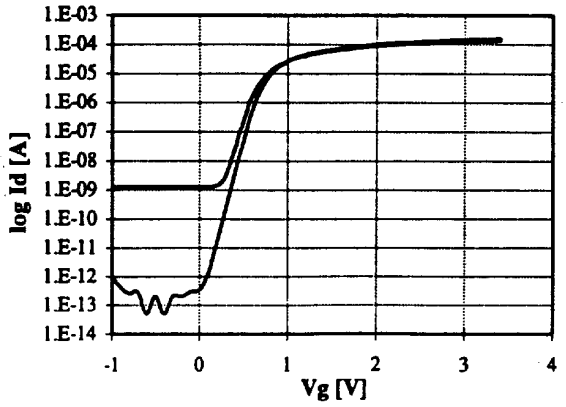


**Figure 6:** Subthreshold currents before irradiation and after 1 Mrad. Vds=50mV

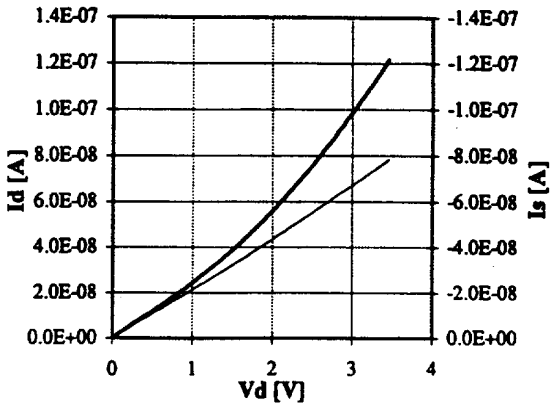


**Figure 7:** Leakage current after irradiation (1 Mrad) versus drain voltage. (Vg=0)

In the picture 7 the two plots represent the drain and the source currents, and this is done to separate junction from transistor leakage. It can be noted that the shape of the curve is not the usual one for the leakage currents (see for example figure 9), and this was true for all the three transistors that showed such high leakage. In this case the junction leakage was an important fraction of the total leakage, as was not generally the case. Figure 9, for example, shows the usual leakage current shape: drain and source current are coincident indicating that there is no junction leakage.

The leakage current for the transistors in the 0.7μm irradiated with a Vg between 750 and 850mV was comprised between 1 and 120nA. The devices irradiated with the worst case biasing showed leakage up to 20μA, figure 8 and 9 show the results concerning one of these: in figure 8 there are 3 plots, before irradiation, after irradiation and after 3 months of annealing at room temperature (the plot in the middle).

In conclusion, it seems from these measurements that one can not easily predict post-irradiation leakage. We found large spreads for similar transistors irradiated under similar conditions. It has to be noted that we do not have a large statistics, and that we did have some problems with packaging and bonding. To save time we used test structures provided by Mietec which are used for process characterisation, but of which the layout is not really optimal to carry out these radiation tests.

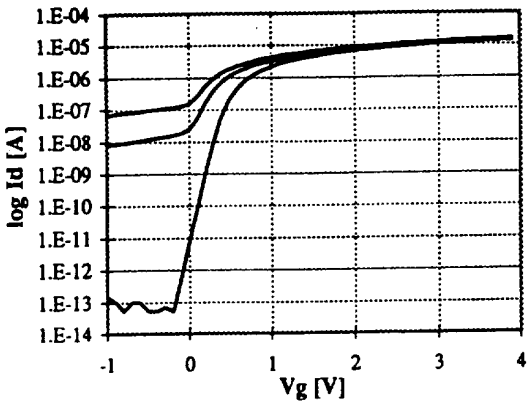


**Figure 8:** Subthreshold currents before irradiation and after 3 Mrad. Worst case bias .Vds=50mV

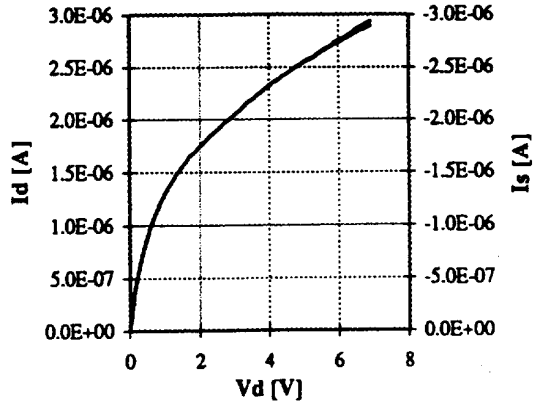


**Figure 9:** Leakage current after irradiation (1 Mrad) versus drain voltage. Worst case bias

## Subthreshold slope

Table 3 summarises the measurements results. It has to be noted that in some cases the post irradiation leakage was so high that it was impossible to extract a subthreshold slope.

| Technology | Device type | Subthreshold slope degradation |
|---|---|---|
| 0.7µm | N-channel | 15-30% |
| | P-channel | 5-15% |
| | P-channel low Vt | <5% |
| 0.5µm | N-channel | 10-20% |
| | P-channel | <4% |

**Table 3:** Subthreshold slope degradation for N and P channel devices of the two technologies tested

## Statistics

We have measured, in total, 180 transistors, 60 of the 0.5µm technology (30 n-channel and 30 p-channel) and 120 of the 0.7µm (40 n-channel, 40 p-channel and 40 p-channel low $V_T$). The idea was to have at least two transistors of each kind irradiated in the same conditions (total dose, bias). Unfortunately this at the end was difficult to achieve, for the already mentioned packaging and bonding problems. All the measurements were done manually, that is in a quite time-consuming way, and for the future measurements an automatic system that uses a switching matrix connected to a computer is currently being prepared, in order to have the necessary statistics with less effort.

## Conclusions

The principal conclusion from our measurements is that the leakage current of the N-channel devices is the most important problem for post-irradiation transistor operation. Usually the cause is a parallel leakage path (at the bird's beak or in the field), but for worst case bias conditions the threshold voltage can degrade sufficiently to become a major factor in the leakage. The degradation of the other parameters was observed but would not prevent post-irradiation operation. Another conclusion is that the 0.5μm technology showed in general much better results than the 0.7μm (even though unfortunately we do not have irradiated any transistors of the 0.5μm under worst case condition) and this allows us to think that combining the use of this technology with some layout techniques like the design of edgeless devices and guard rings could allows its use in radiation tolerant applications. For this reason our future work will focus in more irradiation test and measurements on the 0.5μm technology. We will design edgeless devices and simple circuits with adapted layout in order to study the possibilities and limitations of using this submicron technology in the radiation environment of LHC.