EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN / LHCC 97-15
LEB Status Report / RD29
11 March 1997

SCP

RD 29 Status Report, 1997

DMILL, A Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Electronics

Ph.Abbon, P.Borgeaud, E.Delagnes, M.Dentan, N.Fourches, D.Lachartre, F.Lugiez, B.Paul, M.Rouger
CEA-DSM-DAPNIA Saclay, F-91191 Gif-sur-Yvette, France.

A. Baudrant, J.P.Blanc, E.Delevoye-Orsier, JL.Pelloie, J. de Pontcharra, R.Truche
CEA-DTA-LETI, F-38041 Grenoble, France.

O.Flament, JM.Guebhard, J.L.Leray, J.Montaron, O.Musseau, M. Rouméguère, A.Vitez
CEA-Centre d'Etudes de Bruyères le Châtel, F-91680 Bruyères-le-Châtel, France.

M. Carcaud, T. Corbière, A. Dantec, G. Festes, J. Martinez, C. Le Mouellic, K. Rodde
Matra-MHS S.A., BP 70602, La Chantrerie, 44306 Nantes Cedex 03, France.

J.J.Aubert[1], L.Blanquart[1], V. Bonzom[1], P.Delpierre[1],
A. Mekkaoui[1], R.Potheau[1], A.Hrisoho[2]
IN2P3: (1)CPPM, F-13288 Marseille, France, (2) LAL, 91405 Orsay Cedex, France.

Spokesman : M.Dentan

Abstract

Particle detectors under preparation with the future LHC (Large Hadron Collider) require in their central trackers a fast, low noise, very rad-hard, mixed analog-digital microelectronics VLSI technology [1 - 3].

The DMILL (RD29) collaboration (a Consortium gathering CEA-Saclay, CEA-LETI, CEA Bruyères-le-Châtel, IN2P3/CPPM-Marseille and IN2P3/LAL-Orsay) has developed during the period 1991 - 1995 the rad-hard mixed analog-digital technology DMILL for to the production of electronic circuits for civil and military applications [5- 15]. The features of this technology were adapted to fit the needs of High Energy Physics (HEP) experiments.

DMILL uses an SOI substrate and integrates monolithically rad-hard analog-digital CMOS (0.8 µm), PJFETs and NPN vertical bipolar transistors. These complementary components were chosen to enable the design on the same chip of both analog and digital fast rad-hard circuits.

The typical characteristics obtained with individual transistors or with different mixed analog-digital circuits integrating up to more than 1,000,000 transistors have shown that the DMILL technology fully satisfies the various HEP circuit requirements, in terms of radiation-hardness as well as in terms of dynamic electrical performance, noise, power consumption and integration density [16 - 20].

To make possible the development by laboratories involved in LHC experiments of prototype circuits dedicated to ATLAS or CMS, a first MPW (Multi Project Wafer) was organized in 1994 with DMILL technology. Seven other MPWs have been organized in 1995 and 1996, to allow laboratories to carry out their work with DMILL until it is commercially available. 27 laboratories, most from the HEP community, have now received the DMILL design kit, and owing to the MPWs, 21 of them have designed and/or tested DMILL components or circuits up to 84 mm^2 in size and integrating up to 1 million transistors.

The stabilization of DMILL process was completed at the beginning of 1995 within LETI (Grenoble, France), which is the microelectronics development laboratory of the CEA. In September 1995, TEMIC/Matra-MHS, a subsidiary of the German Daimler-Benz group and of the French Lagardère Group, signed with the CEA a licensing agreement for the transfer of DMILL to its 6" silicon foundry at Nantes. The industrial transfer is currently in progress and will be completed by March 1997. DMILL will be qualified on the MHS production line for the fabrication of mixed analog-digital circuits requiring a radiation hardness up to 10 Mrads (SiO_2) and 10^{14} n/cm^2. DMILL will be commercialized by TEMIC, starting in 1997, in accordance with the schedule of development of the LHC detectors. DMILL MPWs will also be available for the development of prototype circuits in the frame of Europractice, from 1997 onwards [23].

CONTENTS

1. RECALLING OUR GOALS

The next high energy Physics experiments will require a very rad-hard mixed analog-digital microelectronics VLSI technology [1-3]. This type of technology will also meet needs in other different domains (aerospace, defense, nuclear power) [4].

During the last ten years, there has been a significant reduction in the number of industrial companies throughout the world manufacturing rad-hard microelectronics components. Rad-hard microelectronics technologies can no longer be suported financially only by one domain of applications. The variety and extent of the markets for such a technology are important guarantees for its longevity.

On the basis of work started in 1989, three branches of the CEA (DSM-Saclay, Centre d'Etudes de Bruyères-le-Châtel, and DTA-LETI) formed, in 1992, a Consortium which the IN2P3 is associated at the technical level. This Consortium has the objective of developing and industrializing a very rad-hard microelectronics technology called DMILL, and to make it available for different analog and/or digital applications for which the radiation constraints include ionizing dose effects up to 10 Mrads or more or neutron fluences up to 10^{14} n/cm^2, latch-up effects, or SEU*-type transient irradiation effects.

DMILL's main application fields are summarized in table 1:

Application Field	Required Radiation hardness to cumulative effects	Required Radiation hardness to transient effects	Signal to be processed
High Energy Physics [1,2,3,6,10,13]	1 - 10 Mrads (10 years) 10^{14} n/cm^2 (10 years)	- no-latch-up; - low sensitivity to SEU*	- low noise analog - digital
Aerospace Industry [4]	50 - 400 krads/year 10^{12}p/cm^2.year	- no-latch-up; - low sensitivity to SEU*	- analog - digital
Nuclear power [4]	1 - 100 Mrads neutrons		- analog - digital

* SEU: Single Event Upsets.

Table 1

With DMILL's electrical and rad-hard properties most of the markets requiring a hardened microelectronics technology, both for analog and digital applications can be covered. This broad applications field justifies the work made in developing the process, in its industrial transfer then the work to be made in the development of libraries of basic cells and circuits.

The industrial longevity of DMILL technology is one of the project essential objectives. This objective is ensured both by the extent of the market for DMILL technology and the contractual undertakings signed by TEMIC/Matra-MHS, the industrial partner of the project, to maintain DMILL on its production line until at least September 2005 (cf. §.4.1.).

2. FINAL RESULTS OBTAINED FOR THE STABILIZED PROCESS AT LETI.

In march 95, in the presentation of the latest written Status Report of RD29 to the LEB, the stabilization of DMILL at LETI (R&D microelectronics laboratory of the CEA) was nearly completed. The "Fermion" batch contained the splits of the technology which supplied the desirable electrical and radiation hardness results. All that remained was to verify the reproducibility of these results using complementary stabilization batches, which was successfully done at the end of 1995 with "Hadron", "Higgs" and "Lepton" batches and their back-ups. As DMILL technology gave the targeted results reproducibly, the stabilization phase of the process at LETI was declared to be complete. The batches manufactured subsequently in 1996 by LETI as part of the MPWs ("Muon", "Gluon", "Electron", "Top" batches and their back-ups) have all therefore benefited from stabilized DMILL process.

The main obtained electrical performances, radiation hardness and noise for the DMILL batches stabilized at LETI are given sections 2.1 to 2.4 below.

2.1. General electrical characteristics.

A number of typical characteristics of the DMILL technology stabilized at LETI are given in Table 2.

Parameter	Typical Value	Unit	Comments
MOS TRANSISTOR			
Leff N	0.62	µm	Electrical length of a 0.8µm N-channel device
Leff P	0.78	µm	Electrical length of a 0.8µm P-channel device
VTN	0.80	V	Threshold voltage of a 25/0.8 N transistor
VTP	-0.80	V	Threshold voltage of a 25/0.8 P transistor
IDSN (0.8 µm)	7.5	mA	Drain current of a 25/0.8 N transistor with VGS = VDS = 5.0V
IDSP(0.8 µm)	4.25	mA	Drain current of a 25/0.8 P transistor with VGS = VDS = 5.0V
NPN-BIPOLAR			
Beta (1.2*1.2)	150	NU	NPN 1.2µm*1.2µm ideal forward beta
BVCE0	15.0	V	Breakdown of collector/emitter junction with base open
BVCB0	17.0	V	Breakdown of collector/base junction with emitter open
P-JFET			
VPPJ (1.2 µm)	1.2	V	Pinch-off voltage of a 100/1.2 P-JFET
GDPJ (1.2 µm)	1.135	µS/µm	Drain transconductance of a 100/1.2 P-JFET (VGS=0V; VDS=-3V)
Anti EDS structures			
	4 000	V	ESD maximum voltage protected.

Table 2.

2.2. Ionizing radiation hardness

Hardness tests were carried out systematically up to 10 Mrads (SiO_2) with different transistor geometries using several batches produced at LETI with the stabilized DMILL process. The irradiations were made with an ARACOR generator giving 10 keV X-rays with a dose rate of 3.6 Mrads/hour. During the irradiation, the components were biased as indicated in table 3:

Component	Size	Biasing during irradiation
NMOS	W/L = 25µm/0.8µm	Vgs = Vgd = 5V; Vps = Vbs = 0V
PMOS	W/L = 25µm/0.8µm	Vgs = Vgd = Vbs = -5V; Vps = 0V
NPN	emitter 1.2µm*1.2µm	all pins grounded
P-JFET	W/L = 2000µm/1.2µm	Vgs = +5V, Vds = -5V

Table 3: Biasing of DMILL test transistors during irradiation.

The following results show, for these transistors, the typical distribution obtained for a wafer, then between wafers of the same batch, then between batches, for the shift under irradiation of the main parameters sensitive to ionizing irradiation. All these measurements were made within one hour after the irradiation.

2.2.1. NMOS:

ΔVt scatter in a wafer:
The distribution of the threshold voltage shift ΔVt after 10 Mrads (SiO_2) as a function of the position of the test transistor on the wafer is shown in figure 1. ΔVt goes from a minimum of around -65 mV at the wafer center to a maximum of around -100 mV at the wafer edge.

ΔVt scatter between wafers of the same batch:
The average, maximum and minimum ΔVt measured after 10 Mrads (SiO_2) on three wafers from the same batch, selected to represent the natural deviations (minimum, maximum, typical) of *electrical* parameters (except radiation hardness parameters) induced by the process are shown in figure 2. The scatter in these results between wafers from the same batch is very low, which shows the good reproducibility of the hardness level in the same batch.

ΔVt scatter between batches:
The distribution of the average ΔVt, measured after 10 Mrads (SiO_2) for 10 batches manufactured at LETI with the stabilized DMILL process is shown in figure 3. The average ΔVt after 10 Mrads (SiO_2) is -100 mV (+35mV / -65 mV), it is below the Vt fluctuations accepted for the process without irradiation.

2.2.2. PMOS:

ΔVt scatter in a wafer:
The distribution of the threshold voltage shift ΔVt after 10 Mrads (SiO_2) as a function of the position of the test transistor on the wafer is shown in figure 4. ΔVt goes from a minimum of around -180 mV at the wafer center to a maximum of the order of -200 mV at its edge.

ΔVt scatter between wafers of the same batch:
The average, maximum and minimum ΔVt measured after 10 Mrads (SiO_2) on three wafers from the same batch, selected to represent the natural deviations (minimum, maximum, typical) of *electrical* parameters (except radiation hardness parameters) induced by the process are shown in figure 5. As for the NMOS, the scatter in these results between wafers from the same batch is very low, which shows the good reproducibility of the hardness level in the same batch.

ΔVt scatter between batches:
The distribution of the average ΔVt, measured after 10 Mrads (SiO_2) for 6 batches manufactured at LETI with the stabilized DMILL process is shown in figure 6. The average ΔVt after 10 Mrads (SiO_2) is -180 mV +/-30 mV. This show the good reproducibility of the hardness between wafers.

2.2.3. NPN:

Scatter in a wafer:
The distribution of the variation of the gain ß after 10 Mrads (SiO_2), normalized to the initial gain ßo, as a function of the position of the test transistor on the wafer, is shown in Figure 7. This distribution which extends from ß/ßo = 70% to ß/ßo = 80% is practically independant of the position of the test transistor on the wafer.

Scatter between wafers of the same batch:
The average, minimum and maximum values of ß measured after 10 Mrads (SiO_2) for the three wafers used to study the scatter of ΔVt of the MOS between batches are shown in figure 8. Here again the scatter is very narrow with the extreme values of ß after 10 Mrads between a minimum of 128 and a maximum of 148. These results show the good reproducibility of the hardness between wafers from the same batch.

Scatter between batches:
The distribution of the average values ß/ßo measured after 10 Mrads (SiO_2) for 6 batches manufactured at LETI with the stabilized DMILL process is shown in Figure 9. This distribution extends from ß/ßo = 88% to ß/ßo = 70%, showing the good reproducibility of the hardness between wafers.

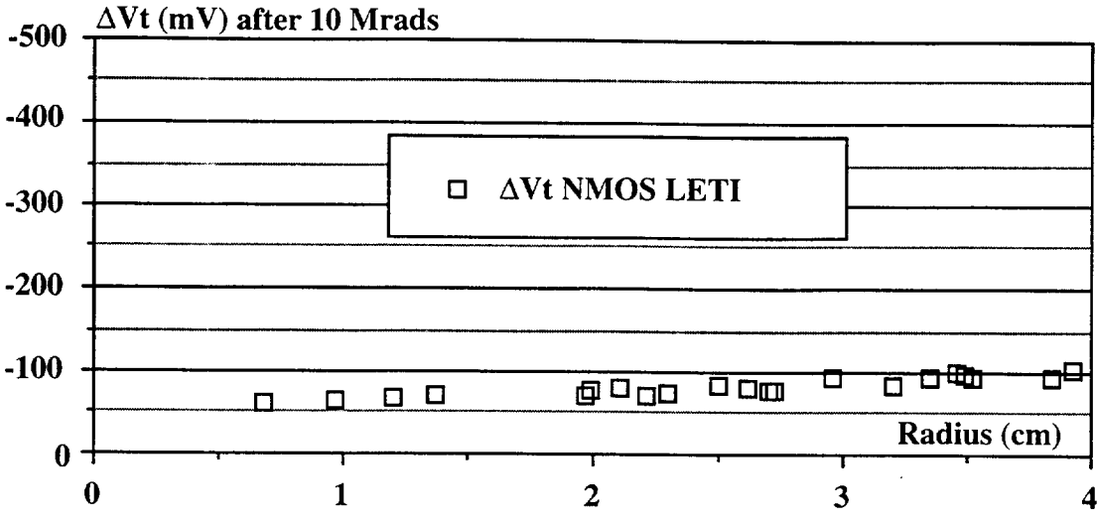


Figure 1: NMOS 25/0.8. Distribution of threshold voltage shift ΔVt after 10 Mrads (SiO2), as a function of the position of the transistor on the wafer.

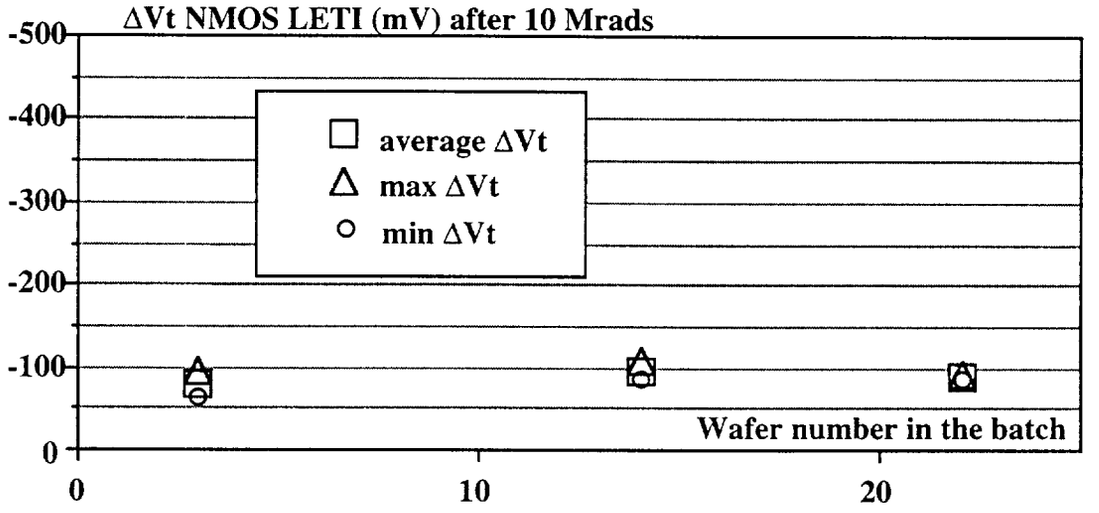


Figure 2: NMOS 25/0.8. Distribution of average, maximum and minimum threshold voltage shift ΔVt after 10 Mrads (SiO2) for three wafers from the same LETI batch.

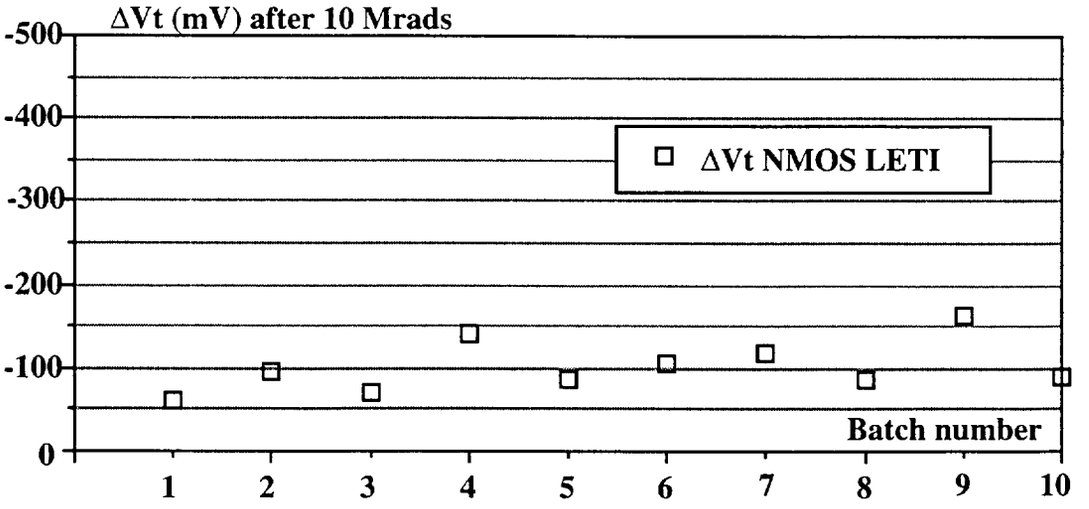


Figure 3: NMOS 25/0.8. Distribution of average threshold voltage shift ΔVt measured after 10 Mrads (SiO2) for 10 LETI batches manufactured at LETI with the stabilized process.

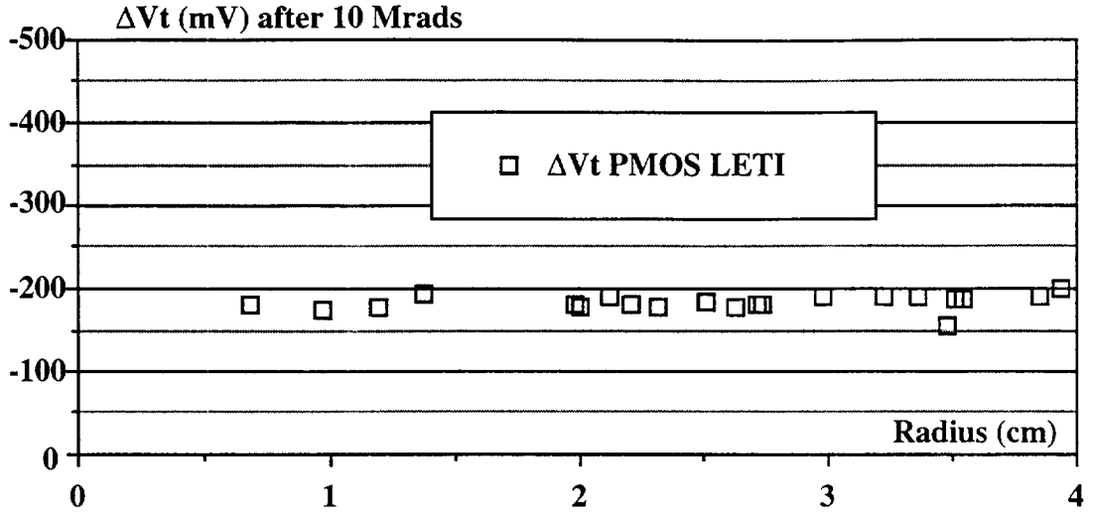


Figure 4: PMOS 25/0.8. Distribution of threshold voltage shift ΔVt after 10 Mrads (SiO2), as a function of the position of the transistor on the wafer.

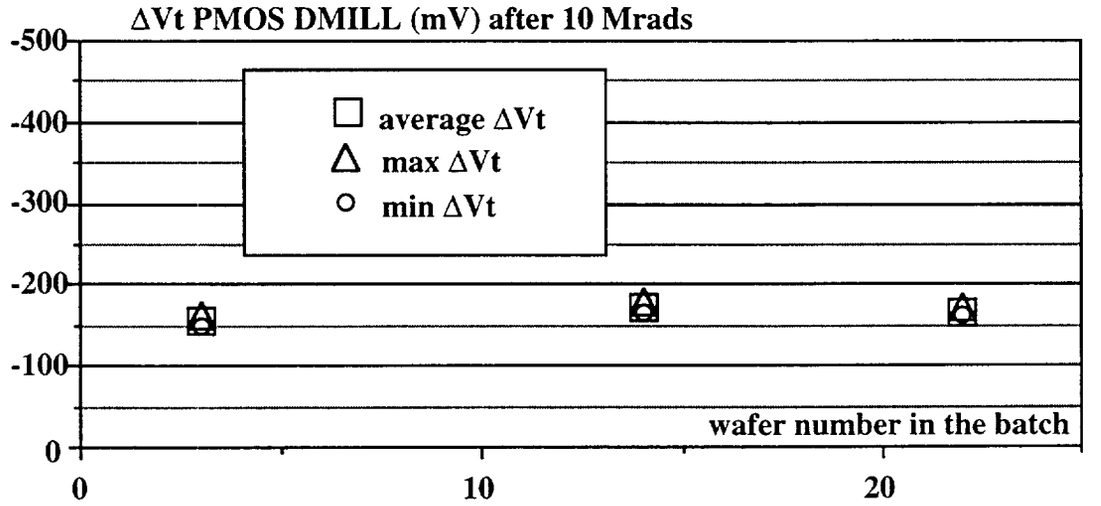


Figure 5: PMOS 25/0.8. Distribution of average, maximum and minimum threshold voltage shift ΔVt after 10 Mrads (SiO2) measured for three wafers from the same LETI batch.

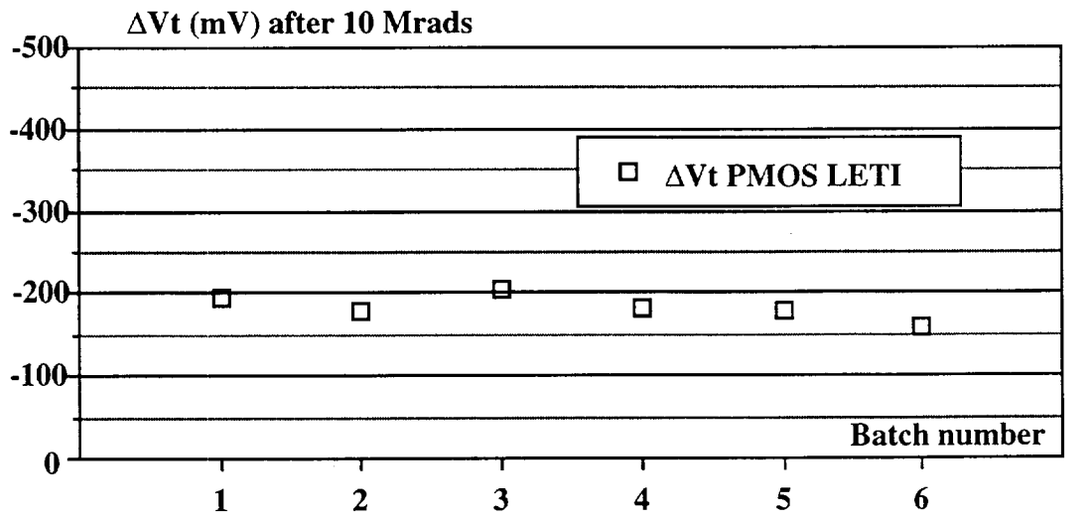


Figure 6: PMOS 25/0.8. Distribution of average threshold voltage shift ΔVt measured after 10 Mrads (SiO2) for 10 LETI batches from the stabilized process.

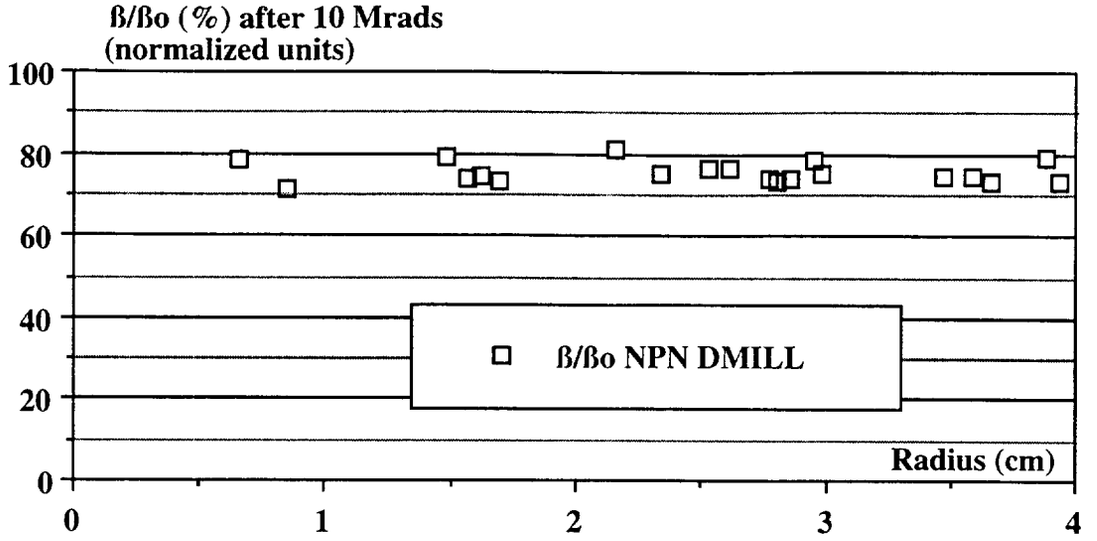


Figure 7: NPN 1.2*1.2. Distribution of average ß/ßo (%) measured after 10 Mrads (SiO2), as a function of the position of the transistor on the wafer.

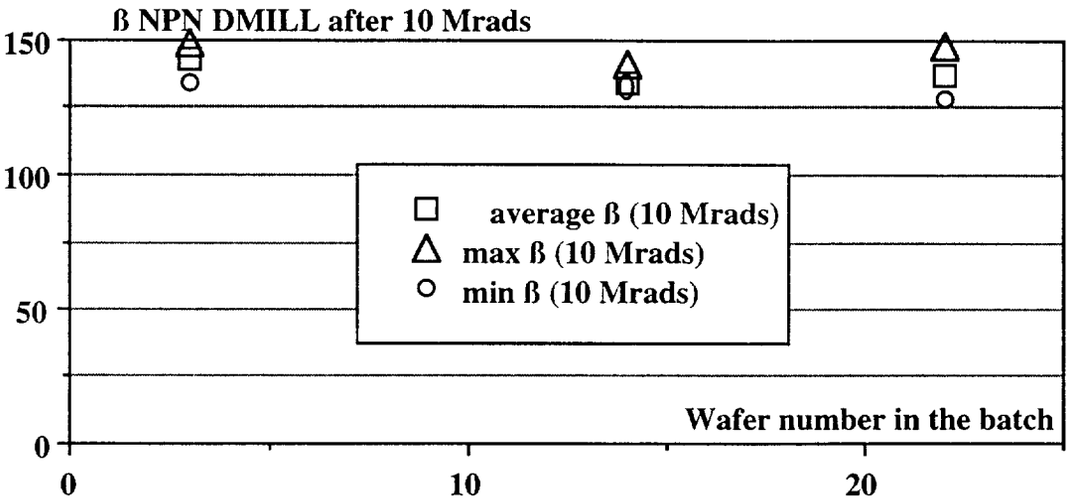


Figure 8: NPN 1.2x1.2. Distribution of average, maximum and minimum ß/ßo (%) measured after 10 Mrads (SiO2) for three wafers from the same LETI batch.

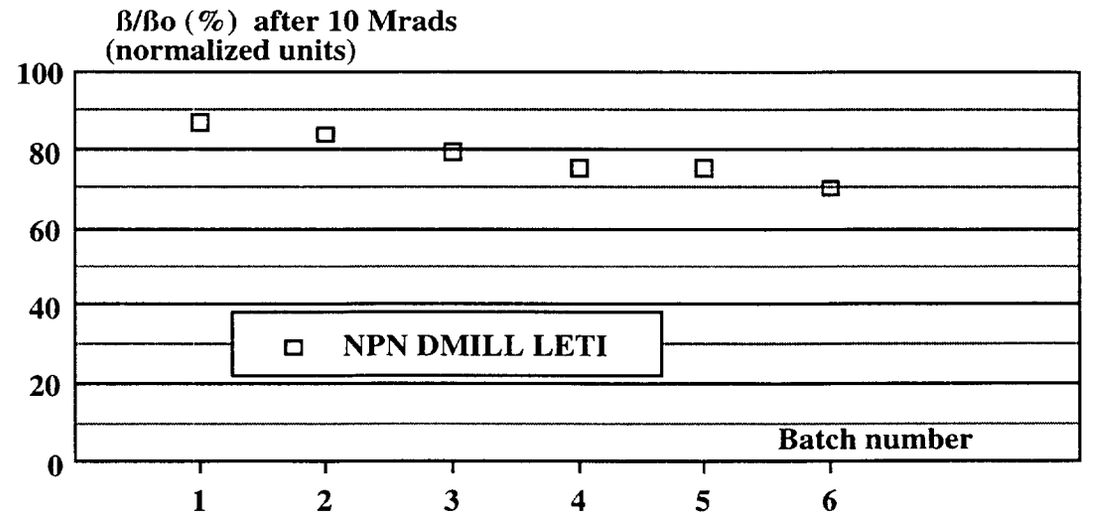


Figure 9: NPN 1.2x1.2. Distribution of average ß/ßo (%) measured after 10 Mrads (SiO2) for 6 batches from the stabilized DMILL process.

2.2.4. PJFET:

The effects of ionizing dose on the DMILL PJFETs are very small: the observed degradations after 10 Mrads are typically $\Delta Vp = -15$ mV for the pinch-off voltage. These shifts are reproducibles within a wafer, between wafers in a batch and between batches.

2.3. Neutron hardness

Owing to their operating mode, NMOS and PMOS are not sensitive to neutron irradiations up to 10^{15} n/cm^2. Neutron irradiation tests are not necessary for these devices.

JFETs and bipolar transistors are sensitive to neutron irradiation. Neutron irradiation tests were performed, using 1 MeV neutrons produced by a fission reactor. Results are presented in sections 2.3.1. and 2.3.2.

2.3.1. NPN:

As the variation in the gain with neutron irradiation does not depend on the biasing, the test of bipolars were performed with all the electrodes grounded. The variation in the normalized gain, ß/ßo, with the neutron fluence for 1.2µm x 1.2µm bipolar transistors is shown in Figure 10. The DMILL NPN have a nominal gain of 150; after an irradiation to 10^{14} n/cm^2, they retain a gain of 75, which is sufficient for the majority of BiCMOS circuits.

2.3.2. PJFET:

As the variation of the pinch-of voltage with neutron irradiation does not depend on the biasing, the tests of JFETs were made with the electrodes grounded. The variation of the normalized pinch-off voltage, Vp/Vpo, with neutron fluence, for 100µm / 1.2µm PJFETs is shown in Figure 11. The DMILL PJFETs have a nominal pinch-off voltage of 1.2V; this voltage is shifted by around 250 mV after 10^{14} n/cm^2.

2.4. Noise.

Typical noise spectra measured for the 4 types of elementary transistors from 3 DMILL batches manufactured at LETI with the stabilized process are given in Figures 12 to 15. The sizes of the test transistors and the bias used during the tests are given in Table 4.

Transistor	Size	biasing during measurement
NMOS	W/L = 5000µm/3µm	Vp = -3V, Id = 100 µA
PMOS	W/L = 5000µm/3µm	Vp = +3V, Id = 100 µA
NPN	emitter = 10µm*1.2µm	Ic = 100 µA
PJFET	W/L = 2000µm/1.2µm	Id = 100 µA

Table 4

2.4.1. NMOS.

NMOS from 4 batches manufactured at LETI with the stabilized process have a corner frequency of around 50 kHz and a with noise level of around 2.4 nV/√Hz. These results are similar to those presented and discussed in the previous written status report in 1995.

NMOS with a size allowing noise measurement were not implemented in the other DMILL batches processed at LETI.

2.4.2. PMOS.

PMOS from 4 batches manufactured at LETI with the stabilized process have a corner frequency between 4 kHz and 10 kHz and a with noise level between 1.8 nV/√Hz and 2.4 nV/√Hz. These results are similar to or better than those presented and discussed in the previous written status report in 1995.

PMOS with a size allowing noise measurement were not implemented in the other DMILL batches processed at LETI.

2.4.3. NPN.

NPN from 3 batches manufactured at LETI with the stabilized process have a very small low-frequency noise and a with noise level between 1.5 nV/√Hz and 2 nV/√Hz. These results are similar to or better than those presented and discussed in the previous written status report in 1995.

NPN with a size allowing noise measurement were not implemented in the other DMILL batches processed at LETI.

2.4.4. PJFETs.

PJFETs from 2 batches manufactured at LETI with the stabilized process have a corner frequency of 1 kHz and a with noise level of 3 nV/√Hz. These results are similar to those presented and discussed in the previous written status report in 1995.

PJFETs with a size allowing noise measurement were not implemented in the other DMILL batches processed at LETI.

CONCLUSION CONCERNING DMILL STABILIZATION AT LETI.

DMILL technology was developed to integrate low noise NMOS, PMOS, NPN and PJFETs with a radiation hardness level of 10 Mrads and 10^{14} n/cm^2. The results given in this section show that this objective has been reached. The DMILL technology stabilized at LETI has the targeted radiation hardness level with a narrow distribution reproducible within a wafer and between wafers and batches; and its transistors reproducibly have the targeted low noise properties.

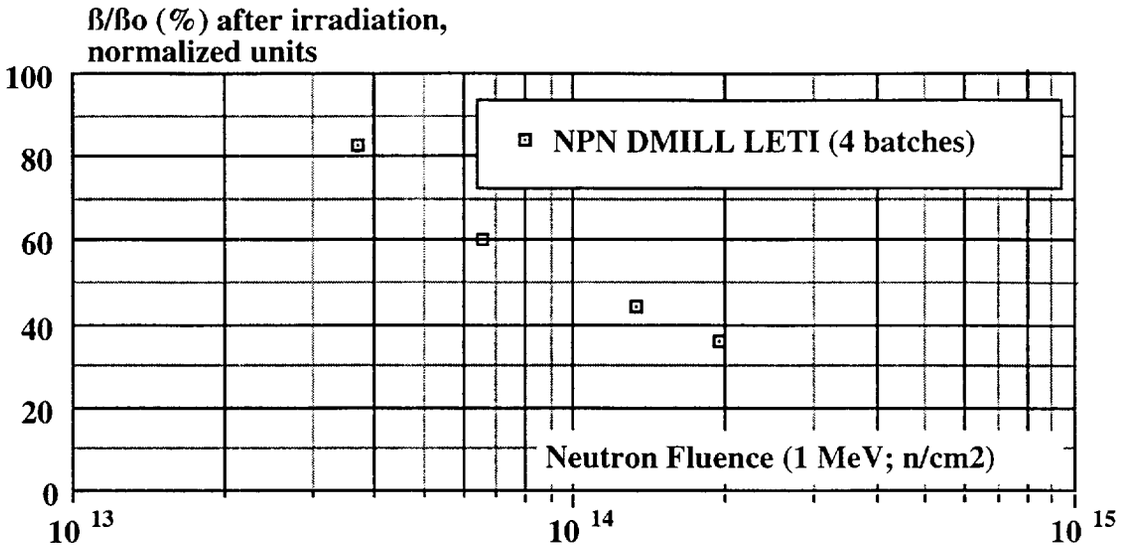


Figure 10: NPN 1.2µm*1.2µm. Evolution of ß/ßo (%) with neutron irradiation, measured with Ic = 100µA for 4 batches from LETI stabilized process.

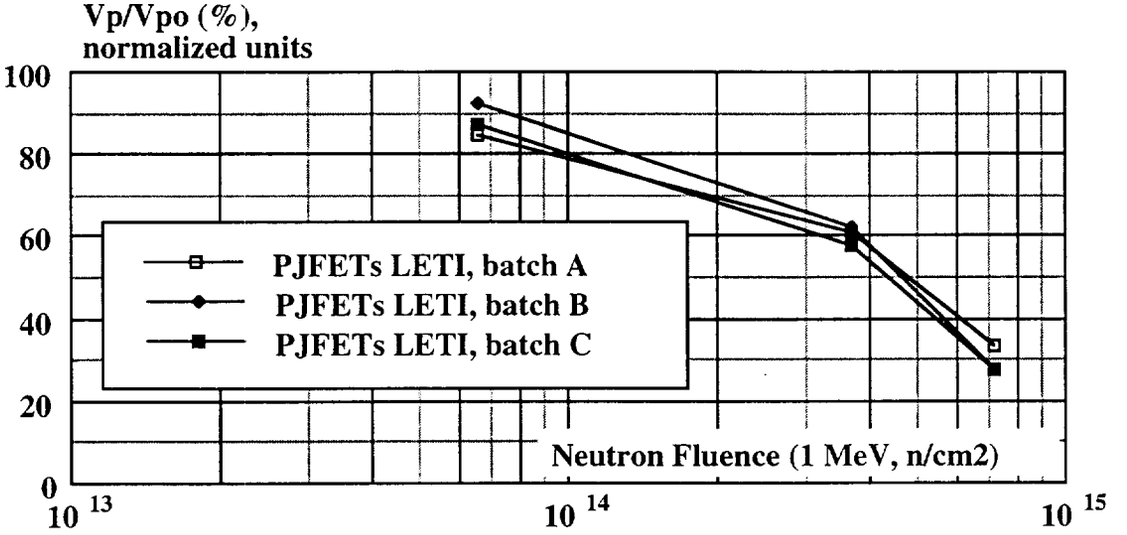


Figure 11: PJFET 100µm/1.2µm. Variation of Vp/Vpo (%) with neutron irradiation, measured for 4 batches from LETI stabilized process.

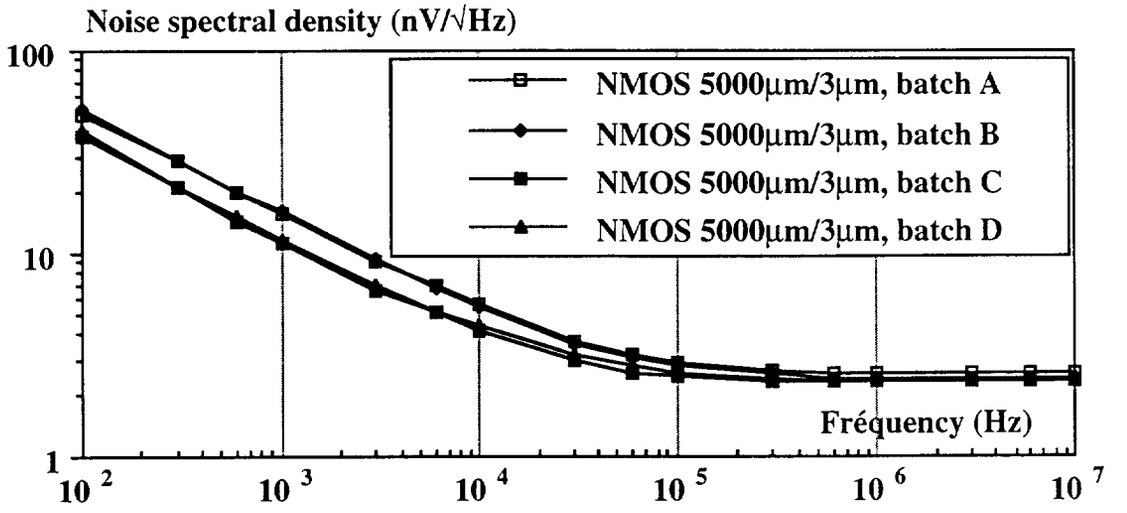


Fig.12: NMOS, W/L = 5000 / 3, Id = 100 µA, Vp = -3V. Noise spectrale density measured on NMOS for 4 batches from LETI stabilized process.

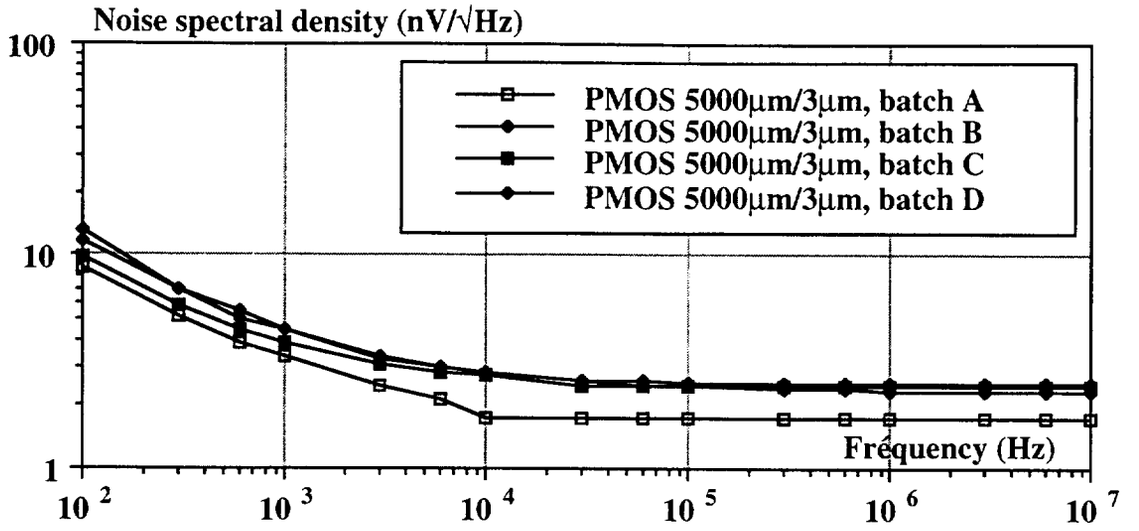


Fig.13: PMOS, W/L = 5000 / 3, Id = 100 µA, Vp = -3V. Noise spectrale density measured on PMOS for 4 batches from LETI stabilized process.

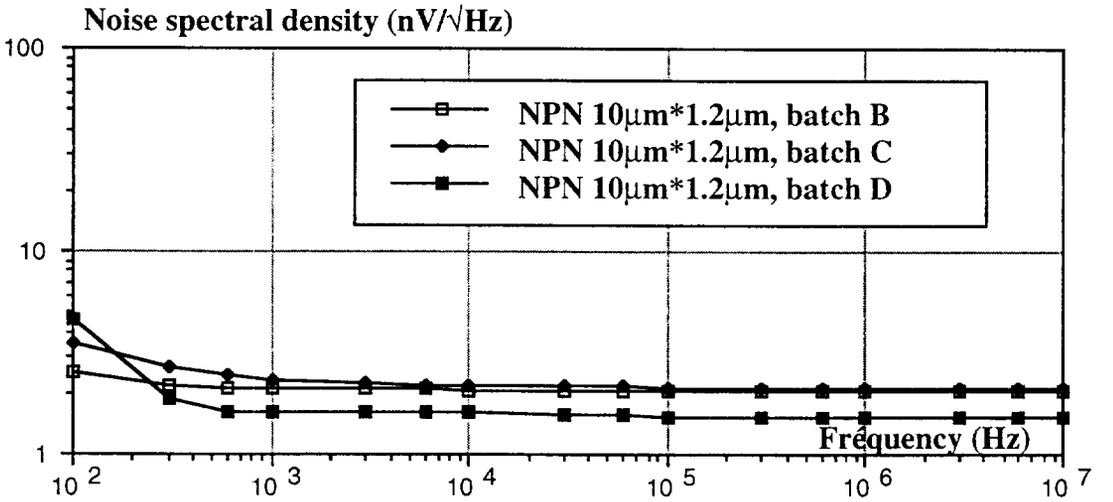


Fig.14: NPN, emitter = 10µm*1.2µm, Ic = 100µA. Noise spectrale density of NPN for 3 LETI batches, stabilized process. (The geometry 10*1.2 was not implemented in batch A).

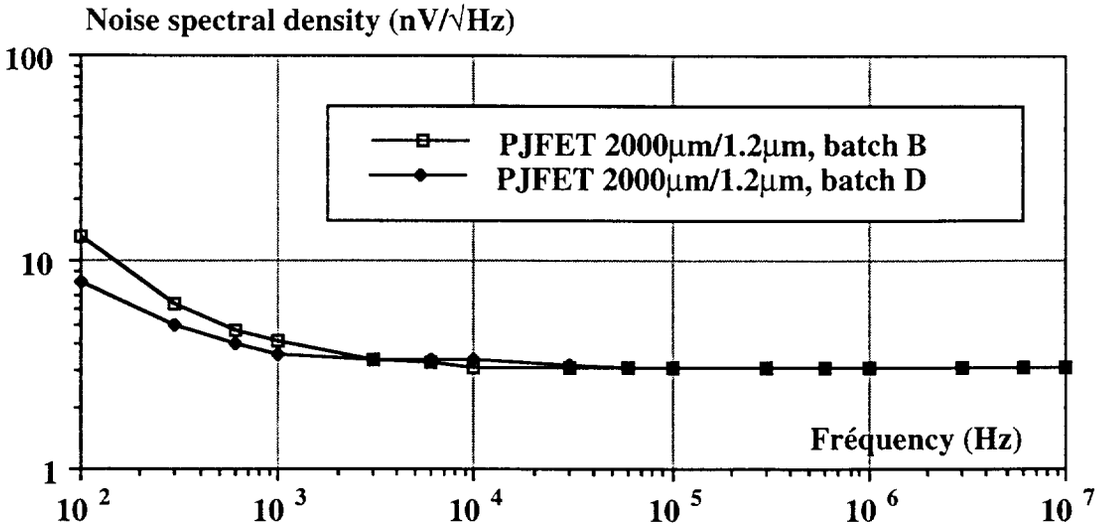


Fig.15: PJFET, W/L = 2000/1.2, Id = 100 µA; Noise spectrale density of PJFETs for 2 LETI batches, stabilized process. (2000/1.2 PJFETs were not implemented in batches A and C).

3. SUMMARY OF THE MPWs PROCESSED BY THE CEA BETWEEN 94 AND 97

From the end of 1994 to 1997, the CEA organized MPW (Multi Project Wafer) batches with the objective of allowing laboratories working on the construction of the LHC to start the study of rad-hard ASICs with DMILL technology.

3.1. Organization

Each applicant laboratory, after signing a Non Disclosure Agreement, received from the CEA a Design Kit containing the simulation parameters and design rules required for the design of full-custom circuits. At the request of a number of these laboratories, the CEA organized three tutorial courses for facilitating the starting of the first circuit designs.

Each user then provided the CEA with a GDSII-type file containing the design of the circuit(s) that he wished to submit.

After receiving all the files for a MPW, the CEA assembled the different layouts in a reticle, subcontracted the manufacture of the corresponding masks then manufactured the batch of wafers that was in each case accompanied by a back-up for process security.

The DMILL user laboratories then received their encapsulated prototype circuits as specified in their request, after signing an agreement committing them to respect a number of usage conditions taking account of the specific properties of the technology.

To date, 27 laboratories have received the DMILL design kit and 17 of these have received DMILL circuits for testing, that they or a partner laboratory has developed.

The planning of the manufacture of all the MPWs batches undertaken by the CEA from 1994 to 1997 is shown in Figure 16.

3.2. Design kit développed by the CEA and furnished to DMILL user laboratories.

The first public version of the DMILL Design Kit was prepared at the end of 1994; it contained the preliminary design rules and simulation parameters which had been previously validated in DMILL Consortium and which had allowed the development of analog and digital circuits giving electrical results quite close to the simulations.

Optimizations were made in this Design Kit in 1995 and 1996 (establishment of final design rules, addition of "extraction" oriented design rules, implementation of parameters obtained from stabilized batches, etc.) resulting in official updates that were sent to the DMILL users.

The present version of the Design Kit (DDK V.2.8) gives satisfactory results both for electrical simulation and design rules verification. Its main elements are:

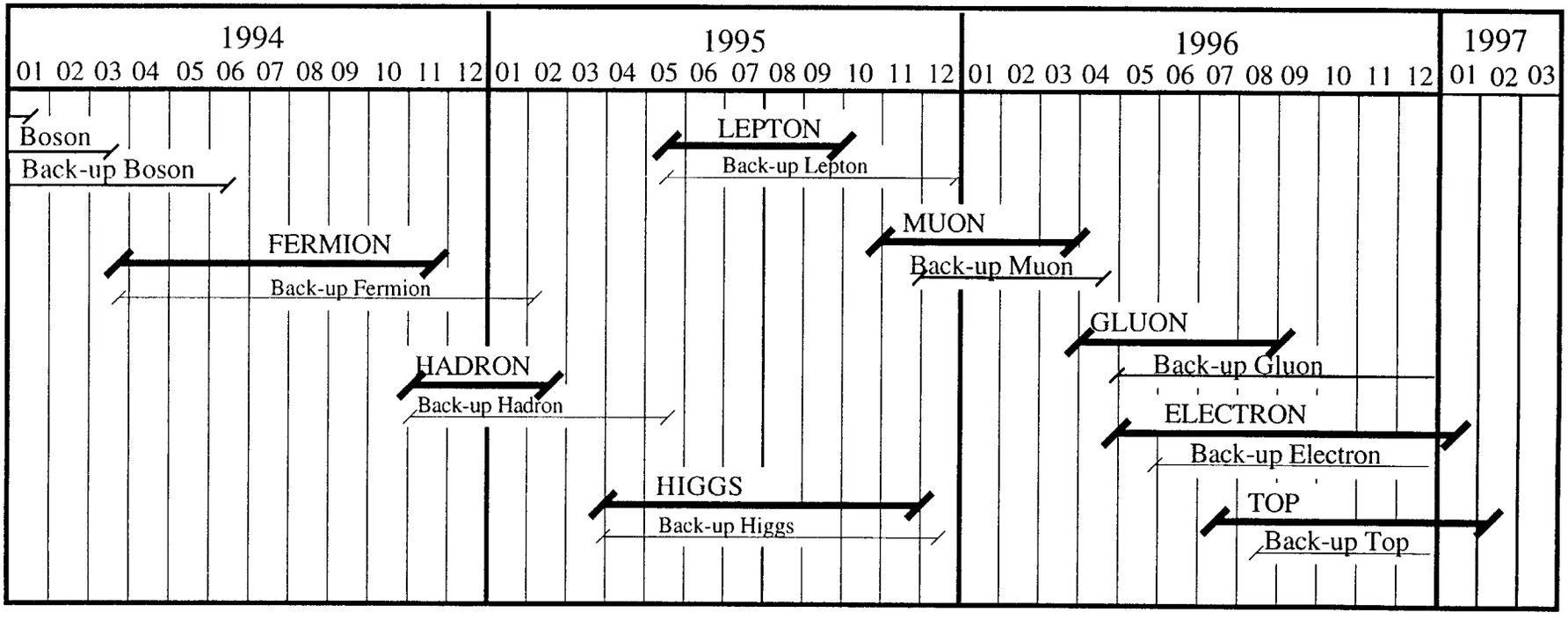
As files dedicated to Cadence / Analog Artist:

Extracted simulation parameters for the following models [21]:
- SPICE level 3 model for the NMOS and PMOS, parametrized as a function of the transistor dimensions;
- Schichman-Hodges model for the PJFET,
- Gummel-Poon model for the NPN bipolar.

Technological files containing the following tools:
- Basic DRC (Design Rules Checking) program, plus different options;
- Program for extracting simulation parameters from active and passive components and certain parasitic resistors and capacitors;
- LVS (Layout versus Schematics) checking program.

DMILL MPWs PROCESSED AT LETI DURING THE PERIOD 1994-1997

Process CEA-LETI



1994:
MPWs: "Hadron", "Fermion".

1995:
MPWs: "Lepton", "Higg"s, "Muon".

1996:
MPWs: "Electron", "Gluon", "Top".

From 1997 onwards:
DMILL commercialized by TEMIC / Matra-MHS
for prototyping (MPWs) or for volume production.

Main batch: duration between circuits submission (GDSII format) and packaged chips delivery.
Back-up.

Fig. 16

Library:
- Description of transistors, resistors and capacitors as parametrized cells.
- Description of pads, contacts and anti-ESD protections devices.
- Examples of transistors, resistors and capacitors.

Printed material:

- Document detailing the technology oriented design rules;
- Additional informations on the simulation parameters and the design rules.

3.3. Contents of MPWs organized between 1994 and 1997

The 8 DMILL MPW batches processed at LETI between 1994 and 1997 supplied a total of 84 HEP-dedicated circuits or sub-circuits, corresponding to a total surface area of 1,000 mm^2 of silicon. Many of the circuits contained in the first MPW reticles were small (typically 5 to 10 mm^2) elementary functional blocks studied for their subsequent integration in more complex ASICs. Progressively, the DMILL users submitted in the DMILL MPWs increasingly complex and larger circuits, reaching up to 84 mm^2 and integrating up to 1 million transistors. The distribution of the surface areas of the different circuits submitted in these MPWs are summarized in Table 5.

size (mm2)	number of circuits
1 - 9	58
9 - 25	15
25 - 50	7
50 - 100	4

Table 5

Examples of complex circuits developed as part of the DMILL MPWs in 1996 by several collaborations for the ATLAS and CMS detectors are given in Table 6. The circuits marked with a (*) are now being developed and will be processed in the 1997 MPWs whose organization is described in section 5.

Sub-détector	Circuit	Design Collaboration
CMS Pixels	32 channels readout Matrix	PSI
CMS Trackers	"FILTRES" circuit	IPNL + LEPSI + Saclay
	APV-6 (translation of a RAL design) (*)	IPNL + LEPSI + Saclay + RAL
CMS Calorimeters	trans-impedance amplifier	IPNL
ATLAS Pixels	12x63 channels readout Matrix	CPPM
	14x156 channels readout Matrix	CPPM
ATLAS Trackers	SCTA-128 / SCTB-128	CERN
ATLAS Calorimeters	"Pipeline" circuit (stopped)	Saclay + LAL
	circuit "ATLAS-CALO" (*)	Saclay + LAL + Nevis Lab.

Table 6

3.4. Examples of notable results (not exhaustive list)

SCTA-32 studied for the readout of the ATLAS SCT [16-17]:
This BiCMOS circuit developed at CERN contains 32 bipolar amplifier channels followed by an analog memory with 32 112-ceel deep amplifier channels, then 32 output amplifier channels and a 32 to 1 MUX operating at 10 MHz. The analog memory is governed by control electronics associated with a FIFO in which the memory adresses are stored. This circuit, which integrates 30,000 transistors on 31,3 mm^2, is completely operational. Its electrical characteristics match the ATLAS SCT requirements and are practically unchanged after 10 Mrads. A 128-channel version integrating 80,000 transistors on 65 mm^2 is now being tested at CERN. The first results show that the correction made in the MUX now allow operation at 40 MHz.

SCTB-32 studied for the readout of the ATLAS SCT :
This BiCMOS circuit also developed by CERN has 32 channels of preamplifiers and discriminators followed by a digital FIFO and a 32 to 1 MUX operating at 40 MHz. This circuit, which integrates 25,000 transistors on 7.8 mm^2, is completely operational. Its electrical characteristics match the ATLAS SCT requirements and are practically unchanged after 10 Mrads, apart from an increase in power consumption which probably is due to an anomaly in the batch from which the chips were taken. A 128-channel version integrating 120,000 transistors on 28,3 mm^2 is now under test at CERN. First results show a complete functionnality at 40 MHz with a preamplifier noise level and a channel to channel discriminator threshold variation within the specifications.

Matrix of 12*63 cells for the readout of ATLAS pixels [18-20]:

This circuit developed by CPPM has 12 columns of 63 pixels. Each pixel is made up of a BiCMOS-JFET preamplifier, a discriminator, and a logic bloc allowing the sending of the informations in the bottom of each column. A logic circuit at the matrix bottom simultaneously processes all the columns and allows outputing the data by initiating a level 1 trigger. The assembly of these elements brings together 300,000 transistors on a 41-mm^2 chip. This circuit is completely operational before and after irradiation up to at least 30 Mrads. It is associated by bump-bonding to a matrix of silicon pixels and under the test beam it has shown electrical performances which completely satisfy the reading of the ATLAS pixels. A new version with 14*156 cells and integrating 1,000,000 transistors on 72 mm^2 is now under test at the CPPM.

DEMDSM circuit dedicated to the final acceptance of DMILL industrial transfer at MHS:

The objective of this circuit designed by Saclay is to be used in the final acceptance of the DMILL technology when its transfer to MHS is complete. It should thus be as representative as possible of mixed analog-digital circuits which will be developed for HEP applications. It is also designed to be easily tested using the wafer probe points at an operating frequency going up to 40 MHz in a purely logic interface.

DEMDSM is constructed around the HPSALM circuit [14,15] initially developed by Saclay and the LAL for reading the ATLAS calorimeter and successfully tested under irradiation up to 10 Mrads in 1995. Some elements have been removed from the basic analog memory while this have been surrounded by new blocks allowing the automatic generation of test stimuli and control signals required for the memory operation and blocks for providing fault detection.

DEMDSM integrates around 49,000 transistors on 28 mm^2 of silicon. Around three quarters of these transistors are used in the logic operations and the remaining quarters in the analog operations. The circuit includes 16 analog channels each with 128 memory cells corresponding to a total of 2048 storage capacitors of 500 fF. It also includes 64 NPN bipolar minimum geometry transistors (4 per channel) used as an input element for level comparators for simulating a front-end stage characteristic of LHC-type circuits. No PJFET transistor is used.

DEMDSM's structure is shown in figure 17. This circuit was tested with a clock frequency up to 60 MHz, these tests showed that it is completely operational.

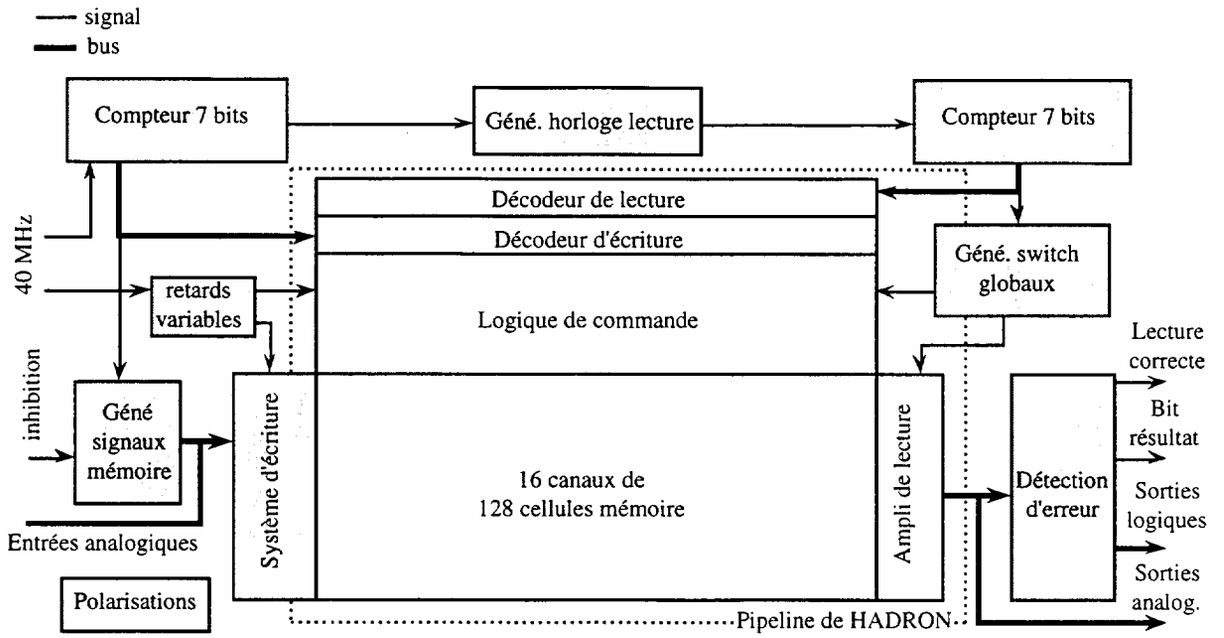


Figure 17: DEMDSM circuit architecture.

4. INDUSTRIAL TRANSFER OF DMILL TECHNOLOGY AT MHS

Following the withdrawal of Thomson-TCS from the DMILL Consortium, the CEA contacted different European industrial companies. These negotiations were completed at the end of 1995 in the choice of the Matra-MHS company, a 50%-owned subsidiary of the German Daimler-Benz group and 50%-owned subsidiary of the French Lagardère group. The agreements concluded between the two groups have given the executive management of the Matra-MHS company to TEMIC a Daimler-Benz Subsidiary. The position of Matra-MHS in the Daimler-Benz group is shown in Figure 18.

4.1 Summary of elements of the contract signed by Matra-MHS and the CEA:

Subject: transfer of DMILL technology developed by the CEA, to the 6" production line of Matra-MHS at Nantes; and non-exclusive operating licence for this technology granted to MHS by the CEA.

Specifications: once DMILL technology is stabilized at MHS it shall have the same electrical properties, hardness and noise as those obtained in the DMILL technology stabilized at LETI. The success of this will be inspected by the CEA and MHS in the final acceptance of the technology.

Transfer duration: 18 months starting from the signing of the contract (the contract was signed September 27, 1995).

Technology longevity: MHS is committed by this contract to keep DMILL on its production line for at least 10 years starting from the contract signing date. DMILL will therefore be operated by MHS at least to the end of September 2005.

Radiation Hardness monitoring: MHS will monitor the hardness of all DMILL batches that it will produce, using a radiation tests procedure developped by the CEA.

The DMILL transfer plan is shown in Figure 19. For review, the general plan of the DMILL project is given in Figure 20.

PRODUCTION AND SALE OF DMILL BY TEMIC, GERMAN SUBSIDIARY OF DAIMLER-BENZ

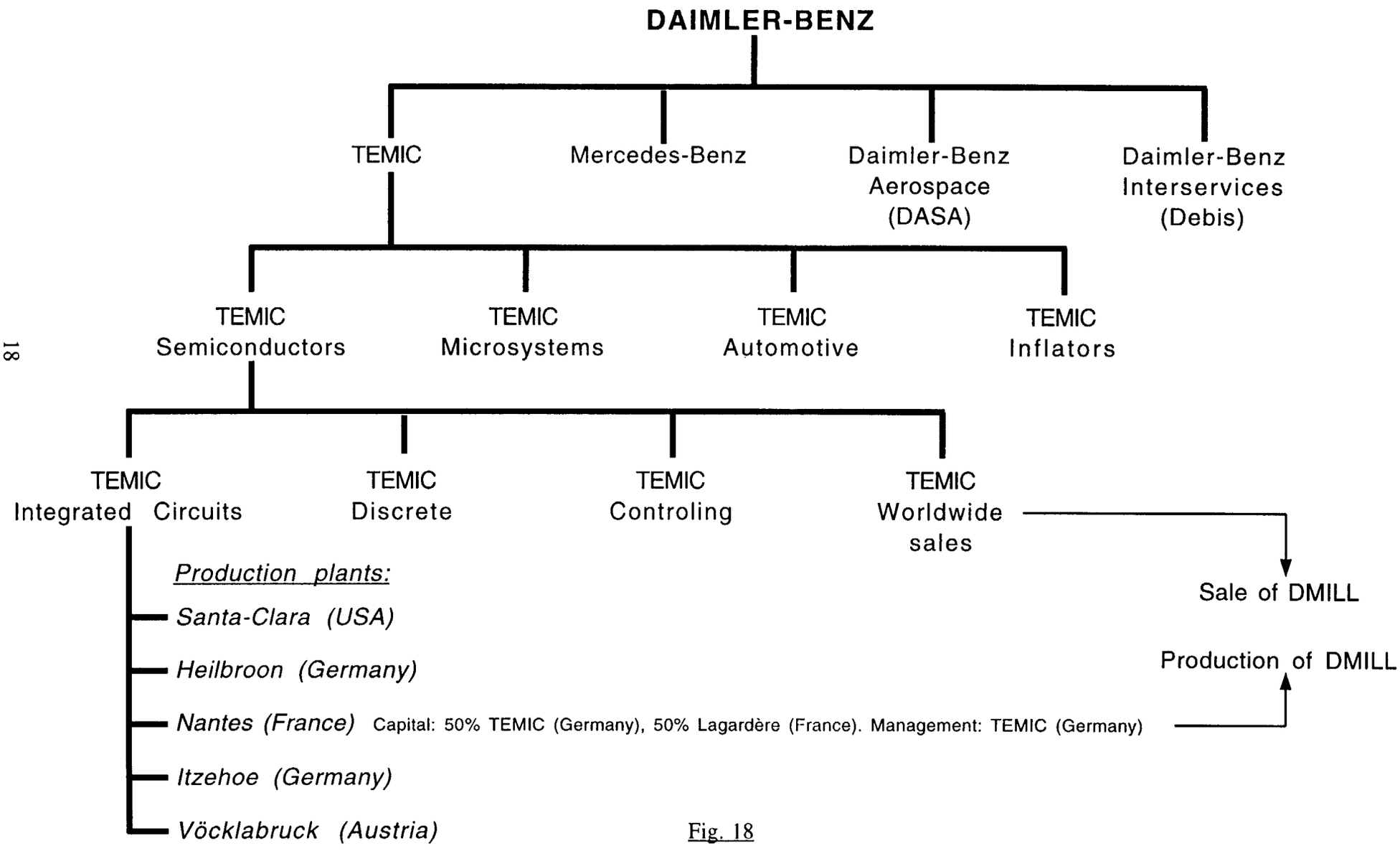


Fig. 18

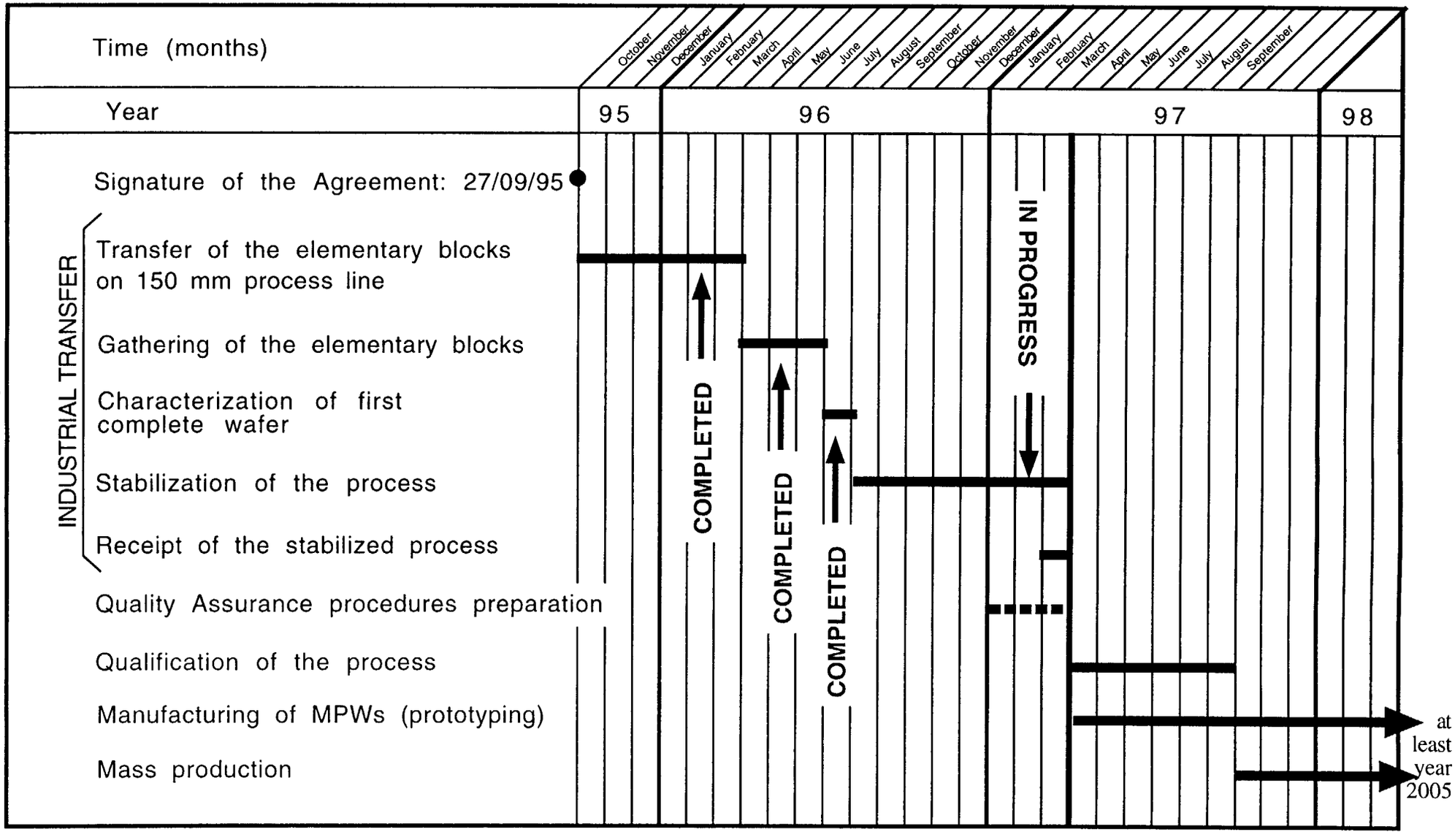


Fig.19: Industrial transfer of DMILL at MHS production plant (Nantes)

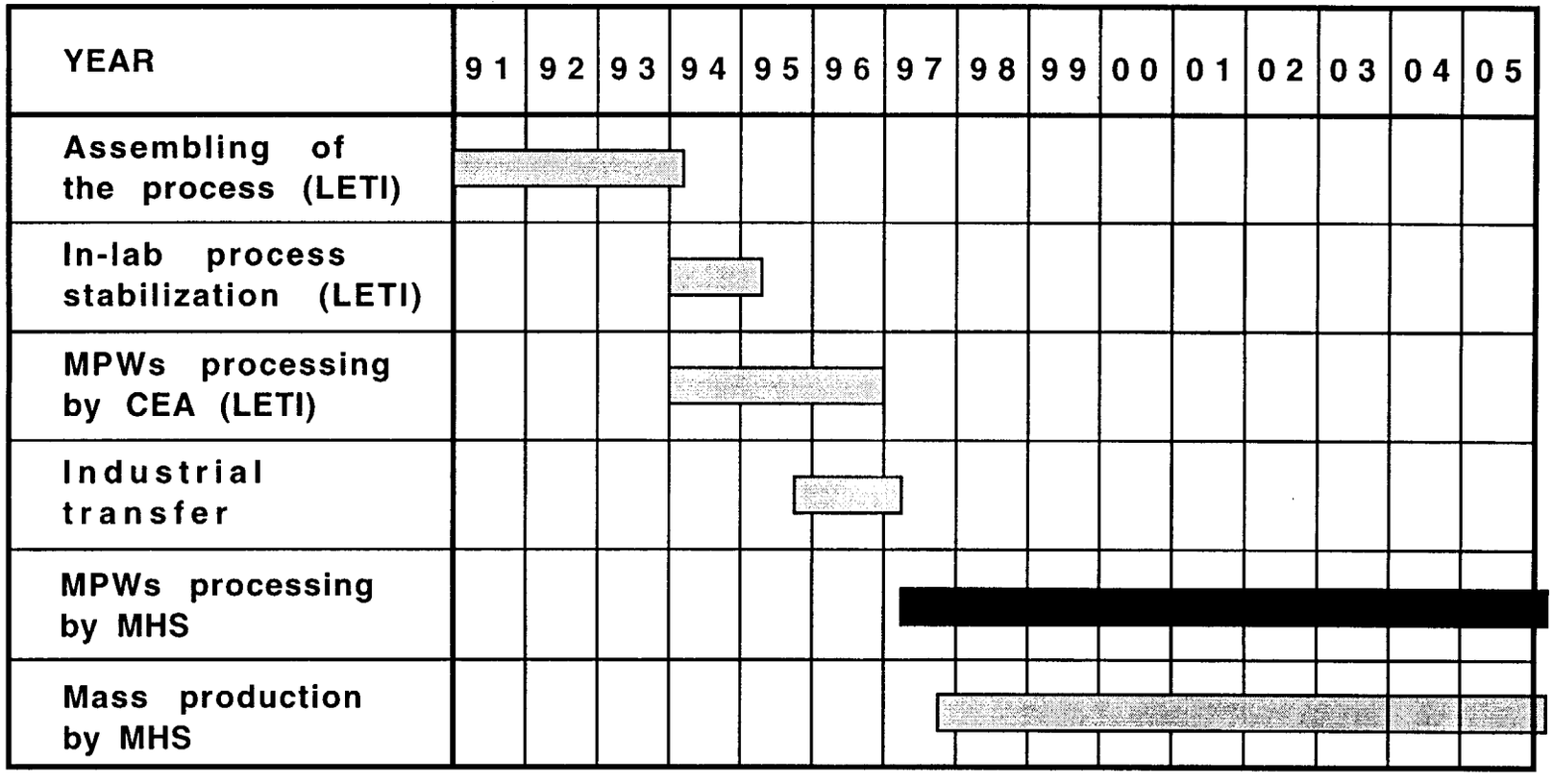


Fig. 20: General schedule of DMILL project.

4.2. Selected strategy for DMILL transfer:

To give the best chances for the success of DMILL's industrial transfer, the CEA and MHS have agreed on the following strategy:

- Transfer of DMILL to the new 6" production line common to all the other MHS technologies. *The DMILL process does not require the implementation of specific equipment.*
- Use of the FMEA (Failure Modes and Effects Analysis) procedure for the transfer of each of the process elementary modules. This approach has made possible evaluating the criticality of each step with respect to final DMILL properties (electrical properties, hardness, noise) thus making the process reliable and implementing inspection as far upstream as possible.
- Development of the circuit DEMDSM representative of HEP applications, which will be used for the acceptance and qualification of the technology (cf. §.3.4., §.4.3.3. and §.4.3.4.).
- The organization selected for the transfer is:
  . Technical working groups organized by domains of expertise;
  . Weekly technical meetings;
  . Program committee made up of MHS and CEA managers;
  . Meetings of the Program Committee every 2 months or more often if necessary.

4.3. Milestones and present results:

4.3.1. Modules transfer and assembling; characterization of first silicon:

The first three stages (transfer of different DMILL elementary modules to the MHS production line, assembly of these modules into a first complete DMILL batch, then characterization of this batch) were successfully completed in the times foreseen in the planning (Fig. 19).

4.3.2. Technology stabilization:

Stabilization of the technology is in progress. Its objective is to optimize a number of process parameters so as to obtain technological, electrical, radiation hardness and noise parameters as close as possible to those of the batches processed at LETI. This stage is now close to be complete. The most part of process parameters is now conform to the specifications. There are a few additional optimizations that have yet to be finished before starting the reproducibility checks.

The main results obtained to date for DMILL at MHS are:

- The technological and electrical parameters obtained with DMILL by MHS (process stabilization in progress) are close or identical to those obtained at LETI. A additional optimization of a number of electrical parameters is currently in progress, close to be complete.
- The radiation hardness (Figures 21 to 23) of NMOS, PMOS and NPN from the MHS DMILL batches (process stabilization in progress) is close to that obtained for the components from the LETI DMILL batches. An additional optimization program is currently in progress. PJFETs radiation hardness measurements remain to be done.
- The noise spectrums (Figures 24 to 27) of the 4 types of transistors from the MHS DMILL batches (process stabilization in progress) are very close to those obtained for the components from the DMILL LETI batches.
- The preliminary manufacturing yield of elementary transistors is identical to that obtained at LETI.
- The 16-bit microprocessor (10,000 transistors, 14 mm^2) and the 16 k-bit SRAM memory from MHS DMILL batches have characteristics comparable to those of the LETI DMILL batches.
- The DEMDSM acceptance circuit (cf. §.3.4., §.4.3.3. and §.4.3.4.) from the MHS DMILL batches is completely operational, with a clock frequency of 40 MHz.

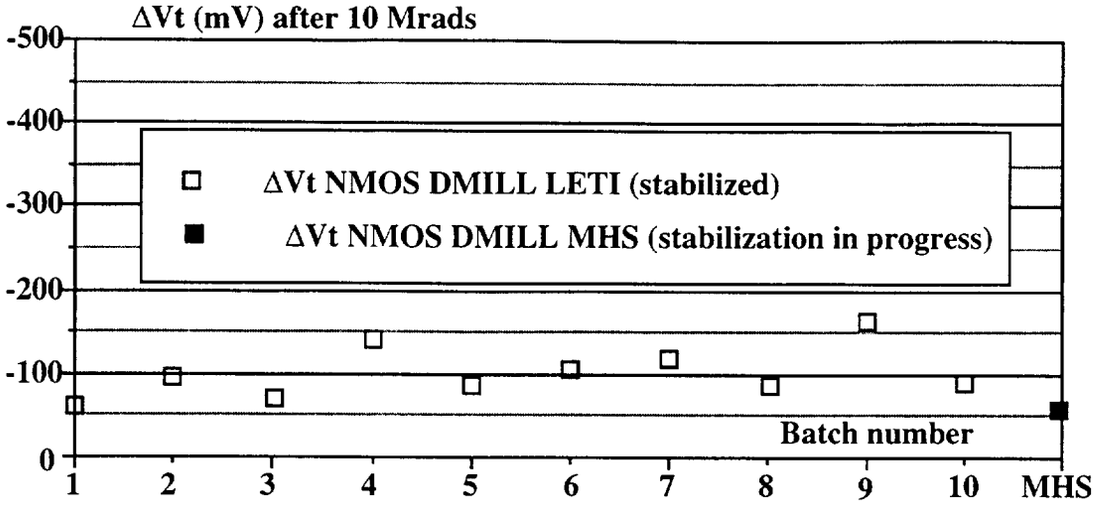


Figure 21: NMOS 25/0.8. Average threshold voltage shift ΔVt measured after 10 Mrads (SiO2) on MHS batch (stabilization in progress), compared to results from LETI batches.

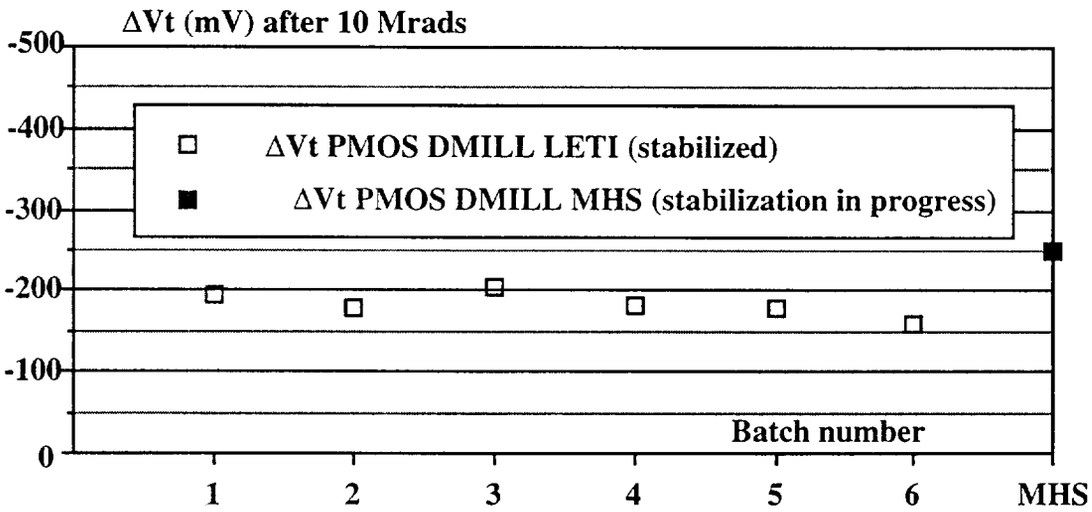


Figure 22: PMOS 25/0.8. Average threshold voltage shift ΔVt measured after 10 Mrads (SiO2) on MHS batch (stabilization in progress), compared to results from LETI batches.

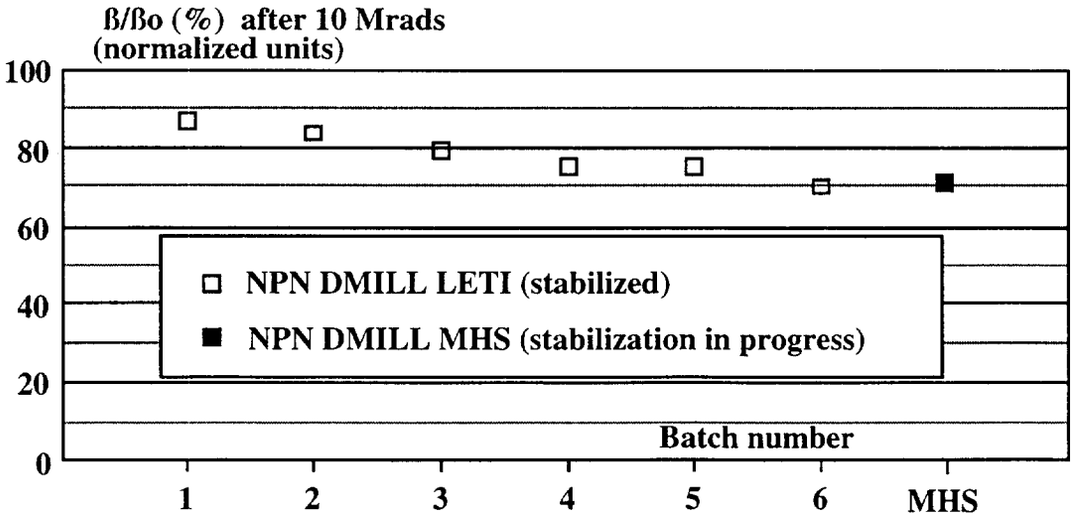


Figure 23: NPN 1.2*1.2. Average ß/ßo (%) measured after 10 Mrads (SiO2) on MHS batch (stabilization in progress), compared to results from LETI batches.

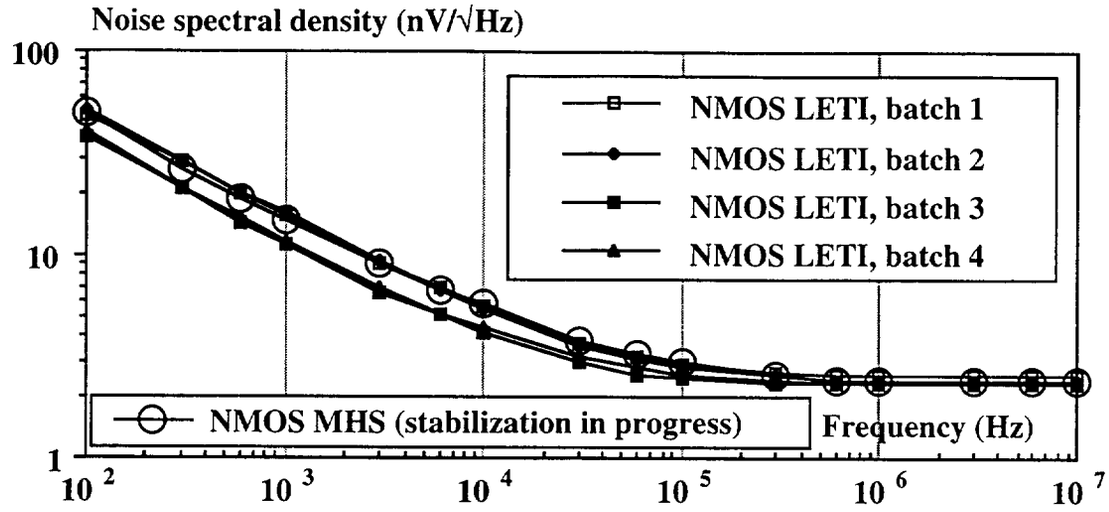


Fig.24: NMOS, W/L = 5000 / 3, Id = 100 µA, Vp = -3V. Preliminary noise spectrale density on MHS batch (stabilization in progress), compared to results obtained with LETI batches.

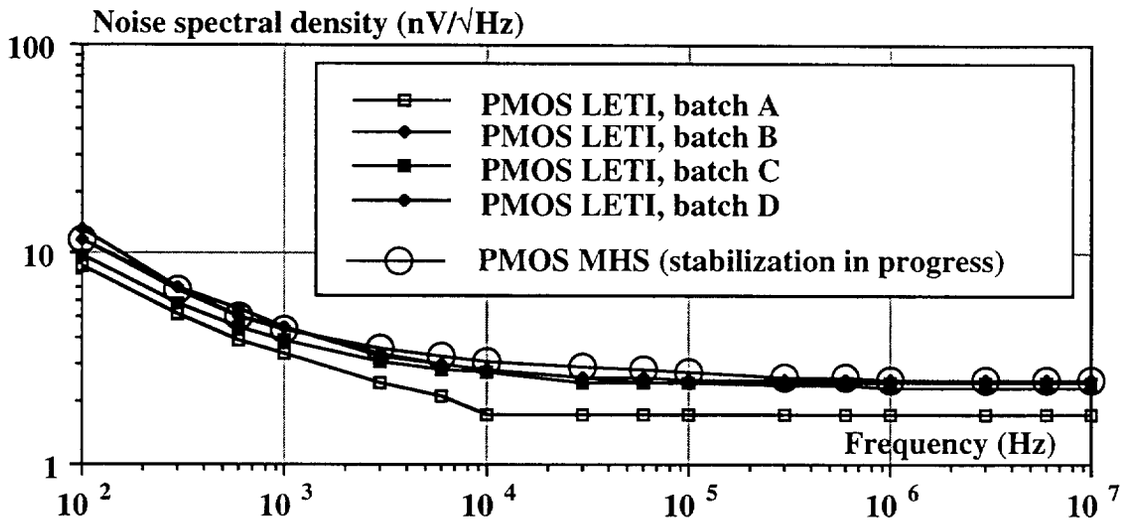


Fig.25: PMOS, W/L = 5000 / 3, Id = 100 µA, Vp = 3V. Preliminary noise spectrale density on MHS batch (stabilization in progress), compared to results obtained with LETI batches.

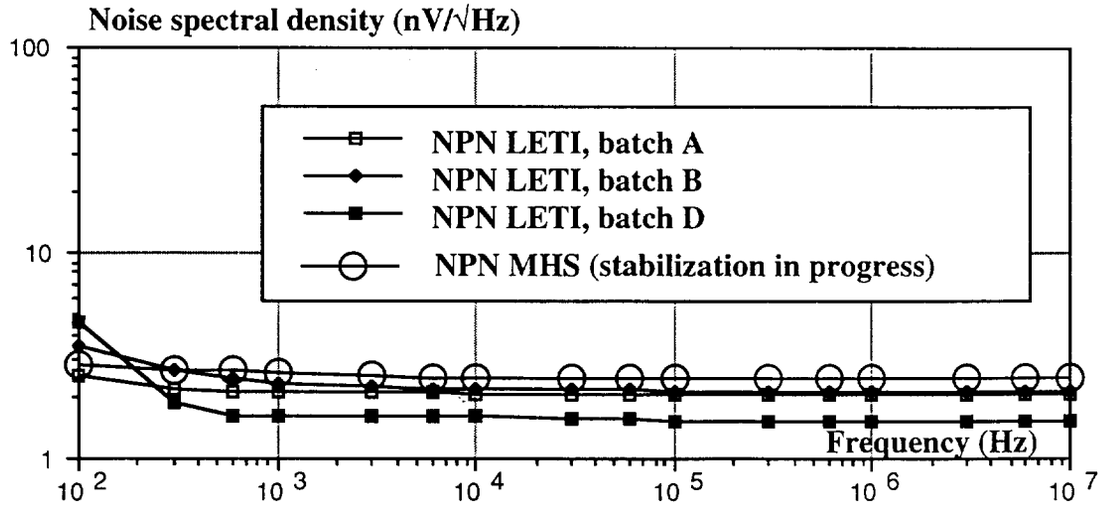


Fig.26: NPN, emitter = 10*1.2, Ic = 100 µA. Preliminary results of noise spectrale density on MHS batch (stabilization in progress), compared to results obtained with LETI batches.

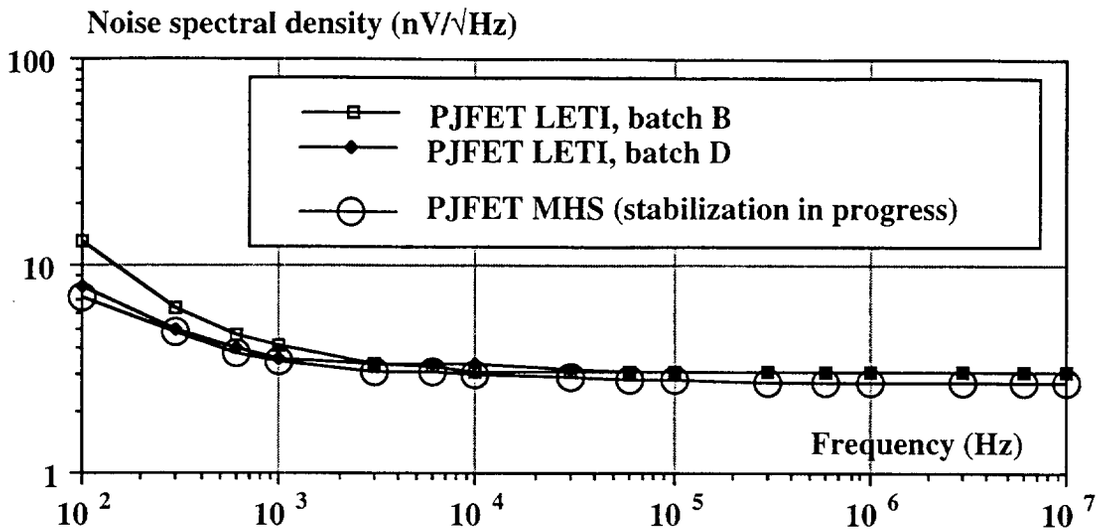


Fig.27: PJFET, W/L = 2000 / 1.2, Id = 100 µA,. Preliminary results of noise spectrale density on MHS batch (stabilization in progress), compared to results obtained with LETI batches.

4.3.3. Final transfer acceptance:

The final acceptance consists of a verification of the conformity of the technology parameters with the specifications. It comprises the following points:

- A compilation of the obtained results at the end of the stabilization for the batches manufactured by MHS with an unchanged process flow;
- Exhaustive measurements of all the technology parameters (technological, electrical, hardness, noise) from MHS stabilized batches. The distribution of this asembly of parameters will constitute a reference that MHS will carrefully ensure reproducing in all the production batches;
- Aging tests (electromigration, hot carriers injection, ...),
- Yield tests of the DEMDSM acceptance circuit and other circuits.

All of the measurements which will be made for the transfer acceptance and the test devices used for these measurements are summarized in Table 7.

Measurements	Test Device
technological parameters	- specific technological test structures.
electrical parameters (not including radiation hardness and noise)	- elementary transistors, - elementary passive components.
radiation hardness	- elementary transistors, - "DEMDSM" acceptance circuit
noise spectrums	- dedicated elementary transistors, - operational trans-impedance amplifiers.
aging (electromigration, hot carriers injection)	- dedicated test structures.
Circuit yield	- 16-bits microprocessor, - 16 k-bits SRAM, - operational amplifiers, - "DEMDSM" acceptance circuit

Table 7: Measurements foreseen in the final transfer acceptance.

4.3.4. Technology qualification:

After technology acceptance, complementary measurements will be made of several batches to qualify the capability of the technology for mass production of circuits. These complementary measurements will include:

- Aging tests accelerated by thermal activation, using the "DEMDSM" acceptance circuit, and based on the standard industrial procedures employed by MHS for qualification of its different technologies.
- New electrical and technological parameter measurements for confirming the capability of the technology measured at the end of the stabilization phase.

SUMMARY OF THE PRESENT TRANSFER SITUATION

WITH RESPECT TO THE PLANNED PROGRAM:

The stabilization is now close to completion. (cf.§.4.3.2.). The last optimization works should be finished mid-March, a delay of 6 weeks with respect to the planned date.

The final transfer acceptance (cf.§.4.3.3.) will start mid-April, also six weeks later than planned. This delay will not affect the starting of the first MPW batch (cf. 5.2.1.), which will benefit from the complete mastery of the technology acquired by MHS in the process stabilization.

The qualification (cf.§.4.3.4.) will also start mid-April and be complete in October at the latest.

5. ACCESS TO DMILL FROM 1997 ONWARDS

5.1. Design Kit and logic cell library:

The Design Kit developed by the CEA will be available from the CEA until the end of May. Starting in June, a new MHS version Design Kit will be available from the IMEC (cf.§.5.2.1) or MHS. This new Design Kit will incorporate that developed by the CEA with addition of the following:
- Worst case simulation parameters based on models used by the CEA;
- Nominal and worst case simulation parameters based on the BSIM model;
- Documents reformatted by MHS and printed in two volumes called EDR (Electrical Design Rules) and TDR (Topological Design Rules).

A library of logic cells was developed in DMILL technology by IMEC at the request of CERN. This library will allow saving a great deal of time in digital circuits design. However, the logic cells in this library, which will be generated automatically from a basic library, will not be optimized in terms of integration density and will have to be validated by further electrical tests. This logic cell library will be available from March onwards, from both MHS and IMEC.

5.2. Access to DMILL for developing prototype circuits:

There will be two possible approaches for developing prototype circuits: use of MPW reticles or use of dedicated reticles.

5.2.1 Use of MPW reticles

MHS has entrusted the organization of MPWs to the Belgian institute IMEC, a representative of EUROPRACTICE [23].

A minimum of three MPWs will be organized in 1997. April 2nd has been fixed as the deadline for submitting circuits for the first DMILL MPW batch (beta run); those for the subsequent MPWs have yet to be set, probably the end of June and beginning of November. If required, it will be possible to have additional MPWs.

For the following years, IMEC will organize a minimum of three DMILL MPWs per year, which can be increased as a function of the demand.

The average foreseen cycle time between the deadline for circuit submission and receiving of the components will be 3 months. This time may be slightly longer for the first DMILL MPW beta run.

The flow of information between the different partners is shown in figure 28.

Matra-MHS will be involved as foundry. IMEC, intermediate between MHS and the users, will supply the Design Kit as an encripted CD ROM. After signing the "Agreement on the use of DMILL Components" document which also includes the "Non Disclosure Agreement" clauses, a deciphering key will be provided. Maintenance of the Design Kit will be carried out annually on the basis of software modifications (Cadence) or possibly technological files modifications.

The standard MPW service will include the sending of 20 non-tested and non assembled samples associated with the electrical and irradiation results obtained for the test structures by MHS.

For additional services, the standard EUROPRACTICE conditions apply:
- Test using probe points of analog and/or digital circuits;
- Additional sectioning of chips;
- Assembly;
- Final test.

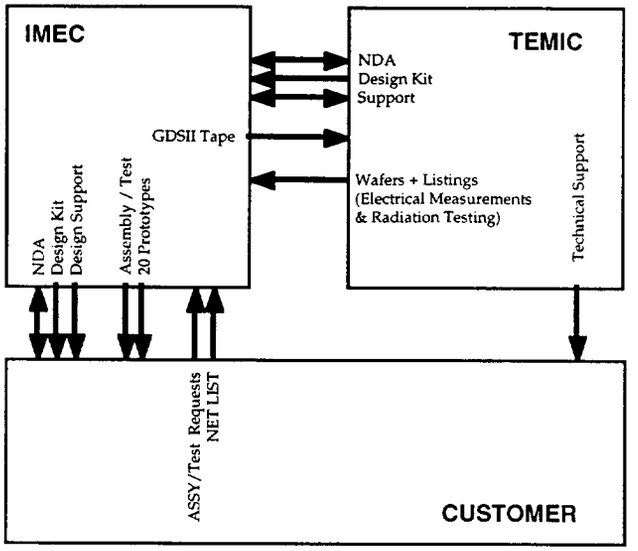


Fig.28: Information flow between MPWs partners.

5.2.2 Use of dedicated reticles:

Certain developments cannot be carried out as part of the MPWs. In this case, the users will be able to submit their circuit to either IMEC or MHS. The minimum delivery will then be eight 6"-wafers. The cycle time and services associated with this service are the same as those for the MPWs.

5.3. Mass production of circuits:

Access to DMILL for mass production is to be made directly to MHS. To verify the sensitivity of the design with respect to the process, a pilot production will be made to analyse the yields using a representative sampling. If there are problems a joint MHS-Designer analysis can be envisaged.

The foreseen flow and inspection points are shown in figure 29.

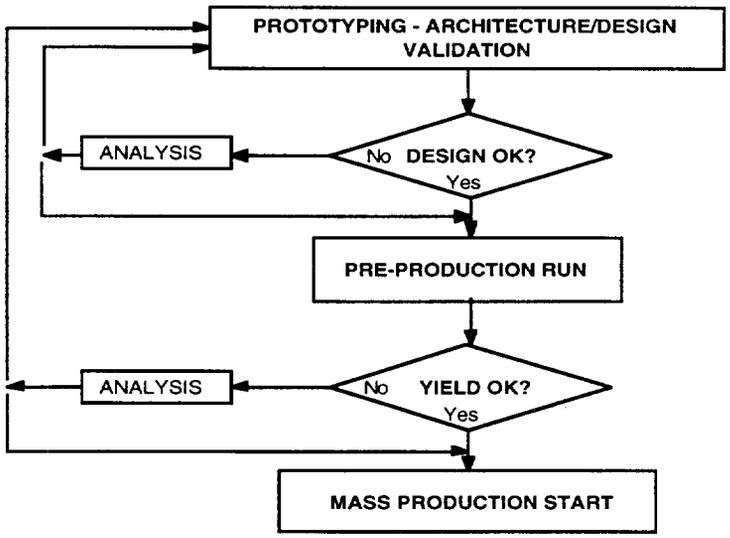


Figure 29: flows and inspection points for a circuit development and production.

5.4. Production tests and inspections as part of the standard MHS offer:

Matra-MHS will employ a quality assurance procedure which will include inspection of the electrical, radiation hardness and noise parameters (cf. appendix 1).

Thus, all the manufactured wafers will be electrically verified using the Process Control Monitors (PCM) tests in the sectioning lines. Any wafer not conforming to the specifications will be rejected. A list of the test characteristics obtained with PCMs will be provided with each delivered wafer.

A radiation assurance will be implemented to survey the shifts in the essential parameters of the elementary devices after an irradiation up to 10 Mrads (SiO_2), and to survey the neutron radiation hardness (cf.appendix 1). This radiation assurance will be regularly carried out on 100% of the manufactured batches, unless otherwise requested. The necessity for this radiation assurance is discussed in appendix 2. A conformity certificate will be provided with each batch of wafers. The statistical follow-up of the shifts of electrical parameters under irradiation will allow ascertaining continuously the technology's capability in terms of radiation hardness.

Irradiation tests at doses above 10 Mrads will also be proposed as part of the services in addition to the standard offer.

Noise monitoring will be carried out on the basis of the MPWs, i.e., at least three times per year. The noise characteristics of elementary devices with different dimensions will be measured before and after irradiation with several biasing conditions representing typical usage cases.

6. CONCLUSIONS

DMILL technology was developed to integrate low noise NMOS, PMOS, NPN and PJFET transistors with a hardness level of at least 10 Mrads and 10^{14} n/cm^2. The results given in this report show that this objective has been fully reached. The DMILL technology stabilized at LETI has the targeted hardness level with a narrow distribution reproducible over and between wafers and between batches; and its transistors have the targeted low-noise properties, which are also reproducible.

Eight DMILL MPWs have been organized by the CEA to allow the HEP community to develop circuits for LHC applications. Several circuits intended for ATLAS and CMS and integrating up to 1 million transistors have been developed through these MPWs by different DMILL user laboratories. Electrical and hardness tests of these circuits show that they completly satisfy the LHC requirements.

The industrial transfer of DMILL to MHS is in progress; the technology is currently in phase of stabilization. Practically all the technological, electrical, hardness and noise parameters of the process are similar to those obtained at LETI. A complementary optimization program for number of parameters is being undertaken. This will be followed in March by an exhaustive check of the reproducibility using several batches; then in mid-April by the final acceptance of the technology transfer. Qualification of the technology will also start in mid-April and will be completed in October at the latest, as foreseen in the transfer planning.

Development of prototype circuits is henceforth possible via MPWs organized by IMEC (EUROPRACTICE) or directly via MHS. The first MPW (run beta) will start April 2nd and will be followed by two other MPWs in 1997 and at least 3 MPWs per year for the following years.

It will be possible to start the first mass production runs using DMILL in October 1997 at the latest.

Hardness will be inspected regularly by MHS up to 10 Mrads and 10^{14} n/cm^2 for all of the batches it produces. The process noise parameters will be monitored via the MPW batches.

MHS is contractually committed to keeping DMILL technology on its production line up to at least September 2005.

7. ACKNOWLEDGEMENT

The CEA is most grateful to the following laboratories, which provided valuable assistance in carrying out the DMILL MPWs in 1995 and 1996:

- IN2P3 - CNRS (France);
- University of Pavia (Italy);
- CERN (Switzerland);
- University of Basel (Switzerland);
- Paul Scherrer Institut - PSI (Suisse).

7. REFERENCES

[1] CMS, Technical proposal, CERN/LHCC/94-38, LHCC/P1, 15 Dec. 1994.

[2] ATLAS, Technical proposal, CERN/LHCC/94-43, LHCC/P2, 15 Dec. 1994.

[3] "Radiation dose expected in LHC inner detectors", Th.Mouthuy, ATLAS internal note, INDET.NO.12, 22 july 1992.

[4] "DMILL, une technologie mixte analogique-numérique durcie adaptée aux besoins de la Physique des Hautes Energies", M. Dentan et al., R. Truche et al., O. Flament et al., Recueil des communications de la journée d'Etudes "Electronique durcie contre les rayonnements nucléaires", Société des Electriciens et des Electroniciens, Arcueil, 3 novembre 1994.

[5] "PJFET on SIMOX for Rad-Hard Analog Devices", E.Dupont-Nivet et al., IEEE International Conference on SOS/SOI Technology, Key West, Florida, October 1990.

[6] "A Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics: DMILL (Durci Mixte sur Isolant Logico-Linéaire)", M. Dentan et al., R. Truche et al., E.Dupont-Nivet et al., R&D Proposal, CERN/DRDC/92-32/P42, may 1992.

[7] "A hardened technology on SOI for analog devices", E. Dupont-Nivet et al., IEEE Transaction on Nuclear Science, Vol.39, N°3, June 1992.

[8] "DMILL (Durci Mixte sur Isolant Logico-Linéaire), a mixed analog-digital radiation hard technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., Nuclear Physics B - (Proc. Suppl.) 32 (1993), North-Holland, May 1993.

[9] "A six device new technology for mixed analog-digital and rad-hard applications", JP.Blanc et al., Proc. ESSDERC 1993.

[10] "DMILL, A Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., CERN/DRDC/93-45, DRDC/RD29 Status Report, 19 October 1993.

[11] "Study of a CMOS-JFET-Bipolar Radiation-Hard Analog-Digital Technology Suitable for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., IEEE TNS vol.40, N°6, dec.1993.

[12] "Radiation Effects on SOI Analog Devices Parameters". O. Flament et al., IEEE TNS 41(3) p565, june 1994.

[13] "DMILL, A Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., CERN/LERB/95-13/Project RD29 Status Report, march 1995.

[14] "DMILL, A Mixed Analog-Digital Radiation-Hard BiCMOS Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., L. Blanquart et al., CERN/LHCC/95-56/Proceedings of the 1st Workshop on Electronics for LHC experiments, Lisbon, Oct.1995.

[15] "DMILL, A Mixed Analog-Digital Radiation-Hard BiCMOS Technology for High Energy Physics Electronics", M. Dentan et al., R. Truche et al., O. Flament et al., IEEE Transaction on Nuclear Sciences, june 1996, vol.43, part.II, pp.1763-1767.

[16] "SCTA - A rad-hard BiCMOS Analog Readout ASICfor the ATLAS Semiconductor Tracker", F. Anghinolfi, W. Dabrowski, E. Delagnes, J. Kaplon, U. Koetz, P. Jarron, F. Lugiez, C. Posch, S. Roe and P. Weilhammer, CERN/ECP 96-19Presented at the IEEE Nuclear Science Symposium, Anaheim, Nov. 1996. To be published in the Conference Proceedings and in IEEE Transactions on Nuclear Science in 1997.

[17] "Development of Front-End Electronics for Silicon Strip Detectors using the DMILL BiCMOS Rad-Hard Process", F. Anghinolfi, W. Dabrowski; E. Delagnes, J. Kaplon, F. Lugiez, R. Szczygiel, Proceedings of the 2nd Workshop on Electronics for LHC experiments, Balatonfüred, September 1996, pp.483-487.

[18] "Study of proton radiation effects on analog IC designed for High Energy Physics in a BiCMOS-JFET rad-hard technology", L. Blanquart et al., IEEE TNS, Vol. 41, N°6, Dec.1994.

[19] "Test Results for Prototype Pixel chips for ATLAS in DMILL Rad-Hard Technology", L. Blanquart, V. Bonzom, A. Mekkaoui, P. Delpierre, Proceedings of the 1st Workshop on Electronics for LHC experiments, Lisbon, September 11-15, 1995, p.68.

[20] "Pixel Analog Cells Prototypes for ATLAS in DMILL Technology", Submitted to Nucl. Instr. Meth.

[21] "Modeling in DMILL technology of CMOS components for analog applications", E. Orsier, transparencies of the Microelectronics Users Group (MUG) meeting, CERN, Nov. 16, 1994.

[22] "Handbook of Radiation Effects", A. Holmes-Siedel and Len Adams, Oxford Science Publications, 1993, p. 179.

[23] EUROPRACTICE ASICs newsline, mars 1997 issue (to be published).

[24] "Total Dose Effect on Negative Voltage Regulator", J. Beaucour, T. Carrière, A. Gach, D. Laxague, P. Poirot, IEEE Transactions on Nuclear Science, Vol. 41, N°6, Decembre 1994, pp. 2420 - 2426.

APPENDIX 1:

GENERAL PRINCIPLES OF QUALITY ASSURANCE

PLANNED BY MHS FOR DMILL

MHS will apply the quality assurance procedures normally used for its other CMOS and bipolar technologies and will add specific hardness and noise inspection procedures, now being prepared.

A1.1. Standard procedures:

These procedures mainly use the two following analysis tools:

- SPC (Statistical Process Control), which measures the distribution of technological or electrical parameters accessible during the process and initiate corrections each time that these parameters tend to deviate from their nominal values. SPC is a particularly powerfull preventive tool for ensuring the process reproducibility (parameters centered on their nominal values).
- PCM (Process Control Monitoring), which measures the distribution of technological or electrical parameters accessible at the end of the process, and initiates the batch acceptance or rejection. In case of rejection, the PCM also initiates a series of corrective actions. The percentage of batch rejection by the PCM is considerably reduced by the preventive actions provided by the SPC.

A1.2. Hardness monitoring:

Hardness is obtained by the implementation of specific technological solutions. The technological steps containing these solutions will be inspected by SPC, like all other steps in the process.

However, in spite of the reproducibility of the process made possible by the SPC, an *a posteriori* hardness verification is indispensable even for a rad-hard technology, as explained in appendix 2. This hardness inspection will complete the standard PCM inspections. It will be carried out statistically using radiation tests up to 10 Mrads and 10^{14} n/cm^2, representatives of the hardness level required for the LHC inner detectors. Batches without this hardness level will be rejected.

Monotoring of hardness to ionizing radiation:

MHS will use a test protocol developped by the CEA - Bruyères-le-Châtel, taking into account the specific radiation constraints foreseen in the LHC applications. This protocol will be based on test methods used since many years by CEA - bruyères le Châtel for DMILL technology. It will consist in statistical hardness tests made systematically by MHS on each batch. This will be by sampling of specific test structures containing the 4 types of DMILL transistors. The sampling will be done using several wafers taken from each batch. The test structures will be irradiated locally on wafer up to 10 Mrads with an ARACOR type X-ray generator. They will be biased during the irradiation exactly as in the tests carried out on the DMILL batches produced by LETI (cf. §.2.2.).

Monotoring of hardness to neutrons:

Due to their construction the MOS are insensitive to fluences up to 10^{15} n/cm^2; thus they do not require any neutron irradiation tests.

The inspection procedure for hardness to neutrons of bipolar transistors will be based on electrical measurements of the transition frequency Ft, directly linked to the hardness of the bipolars to neutrons, as explained in [22].

The inspection procedure for hardness to neutrons of PJFETs will be based on electrical measurements of certain parameters related to the channel of the transistor, directly linked to the hardness of the JFETs to neutrons.

A1.3. Noise monitoring:

The noise inspection procedure is being prepared. It will be based on measurements of noise spectra made with several biasing conditions for the 4 transistor types of DMILL technology. The envisaged transistors for these inspections are summarized in Table 8.

Transistor	Dimensions
NMOS	W/L = 2000 µm / 1.2 µm
NMOS	W/L = 5000 µm / 3.0 µm
PMOS	W/L = 2000 µm / 1.2 µm
PMOS	W/L = 5000 µm / 3.0 µm
NPN	Emitter surface: 1.2 µm x 1.2 µm
NPN	Emitter surface: 10 µm x 1.2 µm
P-JFET	W/L = 2000 µm / 1.2 µm

Table 8.

APPENDIX 2:

ANALYSIS OF THE HARDNESS ASSURANCE

REQUIRED FOR LHC APPLICATIONS

One of the objective of laboratories working on the construction of ATLAS and CMS detectors is to have in the detectors electronic circuits with a hardness satisfying, at a high confidence, the radiation constraints imposed by their application. Two methods can be used to reach this objective:

A2.1. Use of hardened technologies.

The process flow of such technologies has been studied by the manufacturer to obtain a reproducible high average value and narrow distribution of the hardness level. The hardness level is the ionizing radiation dose or the neutron fluence above which the shift in the electrical parameters of the components are outside the specifications and become unacceptable for normal circuit operation.

For hardened technologies, the average value and the distribution of the hardness level are known accurately by the manufacturer who ensures keeping these constant by various technological parameters inspections (SPC) made during the process.

However, certain shifts can occur in the process, producing batches out of specifications. If these affect the electrical parameters, they will be quickly identified by measurements made during the process (SPC) or after the process (PCM) and the concerned batches will be rejected. On the other hand, if they change the radiation hardness to ionizing dose, there is no electrical test without irradiation that will detect these changes. At the present time, there is no electrical test method that will allow predicting hardness to the ionizing dose without irradiation.

To eliminate this shift risk, the manufacturer must carry out a hardness inspection based on irradiation followed by electrical measurements. This inspection is generally made by sampling of elementary test transistors. The sampling depth is determined by the required hardness level and by the average value and distribution of the hardness level previously measured on the stabilized process. The higher the hardness level of the technology, the greater the possible reduction in the sampling required for inspecting the hardness.

Some irradiation effects are threshold phenomena. For example, above a certain dose, a leakage current can appear between an NMOS drain and source, or between two adjascent NMOS transistors. Radiation tests showing satisfactory hardness up to 1 or 2 Mrads do not allow predicting that this hardness will remain satisfactory after an irradiation of 10 Mrads. The hardness inspections must necessarily include irradiations to doses equivalent to those expected in the targeted application.

The general procedure for the use of hardened technologies is:
The user will obtain the results of radiation tests, carried out up to the required dose by sampling of a preliminary production batch, *from the manufacturer*. He can then irradiate a few of his circuits to the same dose to establish a correspondence between the hardness level measured by the manufacturer for elementary test devices and that he measured for his circuit. This correspondence will allow him to judge if the hardness level tested by the manufacturer is sufficient or not for his application. This procedure will subsequently allow purchasing those batches that have successfully undergone radiation tests at a level satisfying the application requirements. Any risk of purchasing a non-conforming batch is thus eliminated.

On the other hand, if the hardness level tested by the manufacturer on the delivered batches is below that required by the targeted application, the user will have to perform up to the required dose level all the additional radiation tests *himself*. He also will have to support the rejection risks (insufficient hardness level or too broad distribution when the tests are made at the required dose for the targeted application), without any possible claim on the manufacturer.

A2.2. Use of non hardened technologies.

A number of technologies for applications not requiring hardness can show, in radiation tests of a few batches, a certain hardness level. The hardness in such technologies is fortuitous and the manufacturer has not made any specific process flow study to ensure its reproducibility nor to inspect its average value or distribution.

The user selecting such a technology in view of an application requiring radiation hardness will have to carry out all the necessary radiation tests himself. These destructive tests will have to be made by sampling of elementary devices. The sampling will have to be broad, since no specific operation has been carried out to guarantee a narrow distribution. It will have to be done by the user for each batch, since there is no guarantee ensuring the user that the manufacturer will not modify a process parameter that does not affect the electrical parameters of the technology but is critical for the hardness, or that he will use exactly the same machines for all of the process for each batches.

Only batches with a sufficiently high and narrowly distributed hardness level will be able to be used reliably for applications requiring hardness. Batches with a broad hardness level distribution shall have to be rejected, since they contain a significant proportion of non conforming circuits. It will not be possible to return these batches that the user has paid for to the manufacturer who is not responsible for the hardness.

For the long term, it is clear that the lifetime of the hardness will not be guaranteed by the manufacturer, who will be able to freely modify his technology whatever the consequences on the hardness level may be. All the development work for full custom circuits with such technologies can therefore be totally lost from one day the next, without any possible claim on the manufacturer.

Furthermore, the execution and interpretation of radiation tests for selecting a technology intended for operating during ten years in a radiation environment of the type expected in the ATLAS and CMS detectors is a critical operation which requires an in-depth knowledge of the irradiation effects on components, and even a thorough knowledge of the studied technology.

Finally, the use of non rad-hard submicron technologies for low-dose applications with the goal of reducing the threshold voltage shifts under ionizing radiations (1) does not eliminate the necessity of performing all of the irradiation inspections mentionned above. The selection of this type of technology does not remove the problem of NMOS drain-source leakage current induced by ionizing irradiation. The use of special structures like square MOS transistors is a possible solution for eliminating these leakage currents but it introduces design difficulties and significantly reduces the integration density and the maximum operating frequency (owing to increased parasitic capacitances). In spite of such solutions, the problem of irradiation-induced leakage currents between adjascent NMOS transistors remains. This problem cannot be solved satisfactorily: it generates additional design complications and an greater reduction of the integration density.

For all these reasons, the use technologies without a guaranteed hardness level cannot be envisaged as a reliable means for applications requiring hardness above a few tens of kilorads and must be treated with extreme caution even for applications requiring a few kilorads hardness.

On the other hand, use of certain "of the shelf" components such as power supply, etc. selected by suitable radiation tests can be considered. Indeed, it can be hoped that the potentially low price and variety of the supply sources of this type of product allow compensating the cost of the rejects of radiation tests and ensuring a certain lifetime either by stocking several items or by changing the supply source. However, this approach is not without risks, as discussed in [24].

(1) For several reasons among which the thermal budget of the process, the MOS threshold voltage shift induced by ionizing irradiations is potentially smaller in submicron technologies than in non-submicron technologies. The leakage currents induced by irradiation in or between NMOS do not follow this trend.