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# RADTOL R&D
# Proposal for studying radiation tolerant ICs for LHC

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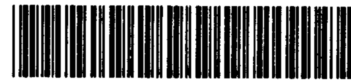

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## 1. Introduction

In the recent years, intensive work has been carried out on the development of custom ICs for the readout electronics for LHC experiments. As far as radiation hardness is concerned, attention has been focused on high total dose applications, mainly for the tracker systems. The dose foreseen in this inner region is estimated to be higher than 1 Mrad/year. In the framework of R&D projects (RD9 and RD20) and in the ATLAS and CMS experiments, the study of different radiation hard processes has been pursued and good contacts with the manufacturers have been established. The results of these studies have been discussed during the Microelectronics User Group (MUG) rad hard meetings, and now some HEP groups are working to develop radiation hard ICs for the LHC experiments on some of the available rad-hard processes[‡].

In addition, a lot of the standard commercial electronic components and ASICs which are planned to be installed near the LHC machine and in the detectors will receive total doses in the range of 10krad to 300krad. This is the case for the outer detector regions of ATLAS, CMS and LHC-B, such as muons, outer regions of the calorimeters and trackers, and the whole ALICE detector. Emerging commercial VLSI deep submicron CMOS processes have a very thin gate oxide of 10nm or less, and therefore submicron devices are expected to become intrinsically hardened against charge trapping effects in the thin oxides. Preliminary studies by several teams indicate promising results for radiation tolerant applications of submicron CMOS processes. This approach has several advantages coming from the use of mainstream technology, such as high volume production and stable processes, high yield, and high device density technology.

In the MUG meeting held at CERN in June 1996, the issue of radiation tolerant circuits manufactured on commercial CMOS deep submicron processes has been addressed. On this occasion, it has been suggested out that the use of such processes, though promising, requires high care and often the application of special architectural and layout techniques. Failures could come not only from total dose effects, but also from Single Event Effects (SEE), and particulary from latchup that can destroy ICs completely, or render them unusable if they are not protected by an anti-latchup system.

The use of Commercial Off The Shelf (COTS) parts is getting more and more popular in the Space community, where the total dose tolerance required is around 20-50 krad over a ten year mission[1]. Though the demand in total dose is lower than that of the outer detectors of the LHC experiments, a specific design methodology for custom chips, latch-up protection and proper qualification protocols for standard CMOS parts are common needs. The Space community has been working on components and technology qualification for more than 20 years, and a standard procedure [2,3] which guarantees the reliability of ICs in the space environment has been defined and is under continuous revision. The HEP community could profit from this experience.

[‡] Harris semiconductor/USA, Honeywell/USA, TEMIC-MHS/Germany-France

## 2. Rad tolerance approaches in commercial VLSI technologies

Commercial VLSI technologies produced in large volumes have the advantage of the thinner gate oxide typical for deep submicron CMOS processes, which is inherently radiation tolerant. Nevertheless, other characteristics of the radiation response are very technology dependent and design layout dependent, and require investigation on different similar processes. In the MIC group of the ECP division at CERN, a first study of the radiation tolerance of three commercial submicron technologies has given some preliminary results.

### *Preliminary study of submicron CMOS technologies*

The study carried out in CERN-ECP/MIC was focused on test transistors and circuits fabricated in 0.7 and 0.5 μm technologies provided by MIETEC and 0.5 μm provided by ST. Reports summarizing the results of the study are joined as annex I and II. Only total dose effects were considered, but the study of SEEs (Single Event Effects) is foreseen in our programme and is of crucial importance for the reliability of the LHC electronic instrumentation.

As expected, the threshold shift of the transistors is of the order of 100 to 300 mV after 1Mrad, decreasing with the thickness of the gate oxide. But the main concern comes instead from the leakage current of n-channel transistors. This leakage originates from source-to-drain current at the edge of the channel, and it is caused by the bird's beak parasitic transistor in inversion after irradiation, or by transistor-to-transistor leakage due to inversion of the substrate under the field oxide. The two leakage effects depend very strongly on the electric field.

The radiation response of the measured transistors is very sensitive to the bias. When a high potential is applied to the gate, the electric field in the bird's beak thick oxide can be sufficiently high to prevent the recombination of the electron-hole pairs created by the irradiation. Therefore, the holes are trapped in this oxide and cause a high threshold shift of the parasitic lateral transistor, hence a significant leakage. As this phenomenon is proportional to the electric field, it is particularly important for digital circuits, where the gate potential can go up to VDD. Nevertheless, also for low power analog ICs the transistor leakage can modify the DC operating conditions significantly and cause circuit failure. The leakage of the parasitic bird's beak transistor can be very high: currents up to the μA level have been measured in submicron devices under worst case gate biasing. The digital circuits we have tested exhibit a significant power consumption increase (for exemple for an ADC, an increase of 2 orders of magnitude after 100 krad irradiation).

### *Design techniques to increase the radiation tolerance*

From these preliminary results, it is clear that transistor leakage current is a major issue to be addressed for total dose effects. Therefore, our programme proposes the study and implementation of design techniques to prevent n-channel leakage. These techniques consist mainly in the use of edegeless transistors to eliminate the bird's beak leakage and of guardrings around n-channel devices to cut the leaky inversion path below the field oxide between adjacent n+ junctions. This design approach has already been envisaged in the past on technologies with feature size larger than one micron, but the radiation tolerance obtained was limited by the threshold shift of the main transistor. The density achievable was also quite unsatisfactory. In modern submicron technologies the threshold shift of the main transistor becomes very small due to the extremely thin gate oxide. Moreover, the density can be very high thanks to the small feature size and the availability of several metal layers for easy connections. These design techniques are therefore becoming increasingly attractive.

### *Low dose rate effects*

Tests at low dose rate radiation exposure, as expected for radiation tolerant applications for the LHC, is not feasible in a practicable period of time. Therefore, accelerated radiation tests with the parametrisation of the annealing effects is mandatory. At present, all the results concerning leakage refer to a high dose rate irradiation followed by room temperature annealing. These results are not representative of what will happen in the LHC, where the dose rate will be orders of magnitude lower. In that case, the annealing of the trapped holes will improve the long term leakage behaviour and this will happen simultaneously with the irradiation on a long time scale.

In order to predict the actual behaviour of the threshold shift and, most important, of the leakage when the transistors will be positioned in the LHC and irradiated at the low dose rates, it is necessary to find a model predicting the time and temperature evolution of the trapped holes in the oxide. Such a model could allow the correct extrapolation to the low dose rates of the LHC, by annealing at high temperature the circuits irradiated in the laboratory at high dose rate. The correct extrapolation is particularly important for very low total dose applications (~10 krad/year), where some technologies might survive without any special precaution if the annealing is sufficiently effective.

The study and verification of such a model is included in our programme, and will require equipment and knowledge of isochronal and isothermal annealing techniques which exist in some of the institutes participating to this proposal.

### *Single event effects SEE.*

Although total dose effects will be reduced by the use of submicron technologies, Single Event Effects are not likely to be affected. However, in HEP there is very little knowledge about these effects. The Space community, on the other hand, has been studying such effects for many years. One of the aims of the collaboration is to understand the importance of these problems in the LHC environment and to find ways of quantifying the tolerance of the different technologies to these effects. In particular it is essential to understand the radiation induced latch-up phenomena in submicron technology.

### *Neutron damage*

Neutron irradiation of CMOS integrated circuits is not considered an issue in terms of total dose response for an integrated flux less than $10^{13}$ neutron/cm$^2$. Nevertheless, we will include a study of the response to the effect of neutron total dose to confirm the intrinsic robustness of CMOS processes. What is not known is whether neutrons could cause latch up phenomena in CMOS ICs. We envisage to address this issue in order to estimate the danger of such effect in the LHC environment.

## 3. Goals

The objectives of this programme can be divided into 5 related categories:

### *1) Study of the use of deep submicron CMOS technologies in a radiation environment*

Starting from the characterization of the radiation response of submicron processes, a study of possible design methodologies to increase the tolerance of ICs manufactured in these technologies will be carried on. This includes the development of design techniques and the assessment of the effectiveness of these techniques through the implementation of test structures and demonstrator circuits in different VLSI submicron commercial technologies. The circuits designed in this context will be chosen amongst those that will be needed at LHC, such as ADC, readout electronics for detectors, instrumentation circuits, and general purpose digital circuits. Special precautions have also to be implemented in I/O cells. A collaboration with semiconductor industry is envisaged. If enough resources are available, the adaptation of standard cell libraries to

the radiation tolerant version will be performed with the help of interested vendors and microelectronics institutes.

### *2) Establishment of a methodology to predict long term effects at low dose rates*

This part will be focused on the understanding of the temperature-accelerated annealing and how to extrapolate its results to predict the actual behaviour of ICs irradiated for 10 years at the low dose rate of the LHC. The results of this study will be used in suggesting the guidelines for a qualification protocol of components and ASICs for LHC experiments.

### *3) Approach of latch-up protection*

All ICs not specifically developed to be latchup-free by process or by design rules in a radiation environment could be subject to this phenomenon, and the consequences could be fatal. To prevent this from happening, protection circuits will be developed which limit supply current and de-latch the components. This would save the component where the latchup has occurred, and make the electronics system tolerant to latch-up.

### *4) Study of SEU effects and their impact on LHC electronic reliability*

SEU has been recognised by the Space community to be a reliability issue. Dynamic logical state upset in memories and digital circuits could damage the integrity of the logical sequence of the control logic. The impact on the reliability of LHC electronics is still not clear. Our objective is to address the SEU issue with experienced institutes of the collaboration.

### *5) Gathering information on radiation tolerance of COTS*

Several electronics systems at LHC will use existing commercial off-the-shelf (COTS) electronics. Knowledge of their radiation tolerance is essential for building electronics equipment placed in a LHC radiation environment. Our objective here is to collect information to enable the HEP community to prepare later a database of radiation tolerant COTS adapted to the need of LHC electronics instrumentation.

## 4. 1997 and 1998 timescale

January 97 -January 98

- Study of single event effects and improvement techniques.
- Development of hardening layout techniques and hardening circuit techniques
- Setting up and calibration of X-ray machine for radiation effects study
- Evaluation of radiation effects on the existing CRIAD ADC fabricated in 0.7µm CMOS MIETEC process.
- Development of common test vehicles for the study of radiation effects of submicron CMOS processes from different vendors.
- Time-Temperature parametrisation for low dose rate
- Study of the radiation effects in 0.5µm, 0.35µm, 0.25µm CMOS from different vendors.

January 98 January 99

- Development of a radiation tolerant TDC
- Validation of the time-temperature model for low dose rate
- Design of rad tolerant CRIAD ADC in 0.5µm CMOS
- Test of rad tolerant readout cell for pixel detector in 0.35µm/0.5µm

- Readout Electronics for pad detectors in 0.7µm/0.5µm using rad tolerant design techniques
- Development of latch-up protection circuit

### *Milestones 97 and 98*

1.Parametrisation of radiation effects of the studied submicron processes. — end of 97.

2.Assessement of the effectiveness of radiation tolerant design techniques — end of 98.

2.Characterisation of test vehicles and ASIC demonstrators
- Test vehicles — end of 97
- ADC — end of 98

4. Assessement of latch up protection circuit — end of 98

5. Assessement of the time-temperature modeling for low dose rate — end of 98

6. Study of radiation resistance, SEE and total dose response of digital standard cell — end of 98

7. Adaptation of standard library using rad tolerant design techniques — end of 98

## 5. Request for financial ressources from CERN in 97

| | |
|---|---|
| 3 Processing runs in collaboration with wafer fab | 150K |
| Travel and meetings | 25K |
| Special instrumentation | 55K |
| Consultancy, contracts and visitors subsistance | 30K |
| Total 1 year/97 | 260K |
| Cost of the second year is expected to be the same | |
| Total cost of the project over 2 years | 520K |

## 6. Technical resources in the specialised institutes

| | |
|---|---|
| **CEA** | Expertise in isochronal and isothermal annealing, temperature, circuit hardening, process characterisation |
| **CERN-ECP**: | Xray facility available, ion beam, ASIC design, testing resource, circuit hardening. |
| **CNES**: | Expertise in SEE , Space qualification, Latch up protection circuits |
| **Uni of Montpellier** | Expertise in dosimetry, temperature-time modelling, , Californium source latch-up and burn-out effects |
| **Uni of Padova**: | Expertise in gate oxide testing, Co-60 source and ion beam facility |
| **IMEC** | Expertise in radiation tolerant standard cells, ASIC design |
| **IST Lisboa** | ASIC design, ADC, expertise in self calibration and error correction |

In addition, we would like to keep contact with Sandia laboratory/USA to profit from their unique expertise in radiation hardening know how.

## 7. Industrial Partners

Our industrial partners have large wafer fabs for deep submicron processes. Some of them, IBM, ST and TEMIC-MHS have shown a technical interest for the study of radiation tolerance, and preliminary technical contacts have been already started. Cost of processing and of mask generation would be for a large fraction funded by industrial partners.

IBM, Yorktown Hts and Burlington site, USA

MIETEC N.V./B

PHILIPS, Eindhoven /H

ST Microlclectronics, Agrate and Castelletto sites/I, Space division Rennes/F and Crolles/F

TEMIC-MATRA, Germany and France

## 8 Overview of the collaboration

The following table shows how the research studies and resources would be shared in the collaboration. This content of this table is preliminary, resources in manpower/year have to be confirmed. Several institutes are willing to contribute in funding at the level of 10 to 20KCHF/year.

| Institutes | T.T model | Irradiation | Chip Design | Rad effect charact. | Iso. anneal. | SEE latchup | Process | Tol. Hard. techniques | ManM. |
|---|---|---|---|---|---|---|---|---|---|
| CEA | Yes | Yes | | Yes | Yes | Yes | Yes | Yes | 6 |
| CERN ECP.MIC | | Yes | Yes | Yes | | | | Yes | 12 |
| CERN-LHC.ACR | | | Yes | | | | | | 6 |
| DESY | | Yes | Yes | | | | | | ? |
| CNES | Yes | Yes | | Yes | | Yes | | Yes | 3 |
| IST | | | Yes | | | | | Yes | 4 |
| IMEC | | | Yes | Yes | | | Yes | | 4 |
| Uni of Madrid | | | Yes | | | | | | ? |
| Fac. Physics Cracow | | Yes | Yes | | | | | | ? |
| Uni of Montpellier | Yes | Californium | | Yes | Yes | | | | 6 |
| Uni of Padova | | Co-60 | | Yes | | | | | 12 |
| Petersburg | | | | | | | | | ? |
| Uni of Torino | | | | | | | | | 4 |
| BNL | | | | | | | | | 4 |
| LIP | | | | | | | | | ? |

## 8. Field of application of the rad tolerant circuits at the LHC

We have contact with electronics coordinators of ALICE, ATLAS, CMS and LHC-B to establish the list of radiation tolerant circuits planned to be used.

## References


[1] RAD COTS conference

[2] ESA/SSC basic specification No. 22900

[3] Advanced Qualification Techniques, P.S. Vinokur et al., IEEE Trans NS Scien., Vol 41, NO 3, June 1994