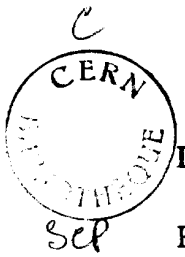

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READOUT SYSTEM TEST BENCHES

Readout architectures for LHC experiments will be required to support very high system bandwidths, comparable to those of modern supercomputers. For emerging applications such as HDTV, European industry is at present actively developing appropriate advanced basic components, like fast analog-to-digital converters and pipelined digital signal processors, as well as high-speed systems for image processing, digital video-tape recording and data transmission.

The evaluation of these complex devices and of efficient system architectures for detector readout can be achieved by the creation of versatile 'test benches' comprising personal computers and workstations closely linked with modular electronic systems and equipped with powerful interactive software. We propose to develop such test benches for application in our own studies and those of other proposed R&D projects.

To make maximum use of the collaborating laboratories' existing expertise and hardware investments, the modular electronics will initially be based on the VMEbus, complemented by special intermodule data links supporting transfer rates exceeding 100 Mbytes/sec. Available Macintosh computers will be used, supplemented by a number of Sun workstations which are required to support certain manufacturers' device and system simulation packages.
Basic hardware and software components to be developed :

Memory modules for fast signal generation and retrieval
High-speed A/D converters
Analog and digital pipelines
Digital signal processors
VLSI systolic array and data-flow video processors
Enhanced computer interfaces
High-speed data links and recorders
UNIX-based environment with special data presentation facilities
Simulation and development systems
Application packages specific to the evaluations to be performed

Different combinations of the above elements and tools would allow the configuration of a series of test benches optimized for various front-end, data transmission and trigger applications. They could thus be exploited by other project groups engaged in different aspects of LHC detector R&D. The proposed test benches would allow the detailed evaluation of architectures based on the devices currently being produced by European industry and national research laboratories, and lay the foundations for possible future projects involving custom VLSI development.