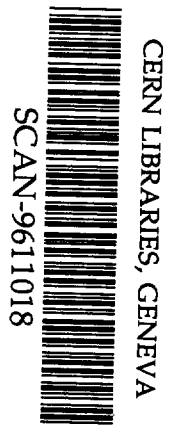


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A Fast DSP-based Calorimeter Hit Scanning System

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Abstract

A custom digital signal processor (DSP) based system has been developed to scan calorimeter hits read by a 32-channel FASTBUS waveform recorder board. The scanner system identifies hit calorimeter elements by surveying their discriminated outputs. This information is used to generate a list of addresses, which guides the readout process. The system is described and measurements of the scan times are given.

1 Introduction

In high-energy and nuclear physics experiments, a number calorimeter systems consisting of many scintillating crystals have been constructed. Although conventional systems, wherein the energy information from each element is recorded as a single digital value, perform adequately in low-to-moderate rate environments, accidental pileup effects can significantly degrade performance at high rates. To mitigate this problem, transient digitizers (TD's), which record the waveforms of the input signals have been developed [1,2]. In such systems, analysis of the recorded waveforms can be used to treat accidental hits and to provide improved energy and timing information.

In a related work, a 32-channel FASTBUS module based on switched capacitor arrays (SCA's) has been developed. This system, details of which can be found

elsewhere[3], is characterized by low power dissipation and modest cost on a per-channel basis, making it suitable for use in systems of several hundred to several thousand channels.

One of the practical issues to be addressed in multi-channel TD systems is minimizing the readout deadtime resulting from the potentially large amount of data produced. One measure taken in the SCA-TD system of reference [3] is the incorporation of a set of digital signal processors (DSP) which are capable of sparsifying the data captured by the SCA-TD.

Further reductions in deadtime can be brought about by independently identifying struck crystals and using that information to guide the readout process. For this purpose, we have developed a fast hit-scanning system, which uses discriminated signals from the crystal array to generate a list of crystals to be read. This hit-scanning system is controlled by its own DSP, which transmits a list of struck channels to the DSP's of the SCA-TD system through a fast parallel I/O bus. A schematic diagram of the total system is shown in figure 1.

In an electromagnetic calorimeter, a photon shower typically spreads over many crystals, making it necessary to expand the list of crystals to be read to include not only those that are above the discriminator threshold but their neighbors as well. This can be accomplished by incorporating the appropriate code in the DSP.

In the following section, a general overview of the scanning system is given, and in subsequent sections, the scanner board and the controller board are described. Test results are presented in section 5.

2 Overview

The hit-scanning system consists of scanner boards (up to 16 per crate) and a DSP controller board (one per crate). The scanner boards scan the input channels to identify hits and the DSP controller board controls the scanning operation and sends the hit channel list (suitably expanded to include neighboring crystals) to the SCA-TD through the DSP parallel I/O lines. The scanner boards are implemented in the FASTBUS standard[4].

3 The Scanner Boards

Discriminated signals from the calorimeter are fed into the scanner boards over twisted-pair flat cables. Each scanner board accepts 64 differential ECL

inputs. When a gate signal (NIM level) comes from the trigger system, the input signals are converted to TTL and are latched in registers (see figure 3).

One of the 16 scanner boards in each crate is directly connected to the DSP controller board through the FASTBUS auxiliary connector, whereas the other scanner boards are connected through a flat cable, as shown in figure 2. During the scanning process, the scanner boards sequentially transmit the address of hit input channels to the DSP controller board.

Each scanner board contains eight identical circuit blocks (referred to below as "scanning blocks"). Each scanning block has eight input channels, yielding a total of $8 \times 8 = 64$ channels per board. The logic diagram of a scanning block is shown in figure 3. It has an eight-bit input register, which latches the signals upon receipt of the trigger input. The address of the lowest active bit of the latched data is determined using priority-encoder logic. Once all hits in an eight-bit logic block have been scanned, the active block asserts a carry signal to the next block. Logic blocks without hits immediately pass the carry to the next block. Carries also propagate across module boundaries through front-panel coaxial connectors. A four-bit address corresponding to the scanner board and a three-bit address corresponding to the current encoder block are appended to the lower three bits from the priority encoder. The ten-bit channel address thus generated is transferred to the controller board via a fast DSP local bus. At the time of transfer, the selected bit is cleared so that another active bit (if it exists) can be processed in the next cycle. This procedure is repeated until all hits are encoded.

Two additional bits are appended to the ten-bit address to indicate that the address data (which are generated asynchronously with respect to the DSP clock) are valid. A carry signal from the last logic block is fed to the processor on the controller board to indicate that the scanning sequence is completed for the event.

4 DSP Controller Board

The controller board is designed as a FASTBUS auxiliary card, which is inserted from the rear of FASTBUS crate. The DSP processor used in this controller board is the Motorola DSP56002[5], which can operate at a 40 MHz clock frequency. The controller board has a no-wait accessible SRAM. Details of the board design can be found elsewhere [6]. There are three kinds of input/output interfaces that enable the DSP to communicate with external devices. They are: (1) the interface to the scanner boards, (2) the interface to the SCA-TD, and (3) the interface to a host computer. These correspond to (1) the DSP bus, (2) the DSP parallel I/O line, and (3) the DSP serial I/O

line, respectively.

The DSP can access the scanner boards via FASTBUS auxiliary connectors, to which the I/O bus lines of the processor are directly connected. The DSP initiates the scanning operation by accessing a specific address in the scanner modules. After scanning, the results from the scanner boards are transmitted to the DSP via its data bus. This connector is also used to supply +5V power to the DSP.

Hit-channel data must be transferred to the SCA-TD system at high speed. To achieve this, a local bus interfaced with the parallel I/O port of the processor is employed. Communication with the host computer occurs over a 38400 bps serial I/O line.

5 Performance

The performance of the hit-scanning system has been evaluated in a bench test, where elapsed times for various operations were measured.

5.1 Data Transfer Time

A detailed diagram of signal transitions during a scanning operation is shown in figure 4. The address of the input channels with hits appear on the data bus 50 ns after the processor activates the scanning operation. Address data are written into the memory of the controller board on the timing of the trailing edge of the scan signal. When reading the address data and before storing it into memory, the processor has to check the flag bits to confirm that the data is valid and that the scanning operation has been completed. This process takes about 20 cycles for the processor, which results in a maximum scanning speed of about 450 ns/hit.

5.2 Carry Signal Propagation Time

The time to scan hits and transfer a carry signal from one scanning block to another was also measured. This was done by considering the case where all eight input channels for the first (#1) and second (#2) scanning blocks were asserted but none of the inputs for the next two blocks was asserted. A timing diagram of carry-signal outputs for the first four scanning blocks is shown in figure 5. The time required to complete scanning of all eight hit channels in

blocks #1 and #2 was measured to be about $3.7 \mu\text{s}$ per block, consistent with the scanning speed of 450 ns/hit.

Since scanning block #3 has no hits, the carry signal from block #2 is passed to scanning block #4 after only 8 ns.

6 Conclusion

We have developed a fast DSP-based hit-scanning system. It can be used to make an address list of the hit channels, which can be sent to a waveform analyzer system such as the SCA-TD to significantly reduce the readout dead-time. The system is implemented in the FASTBUS standard and has achieved a scanning speed of 450 ns/hit.

7 Acknowledgments

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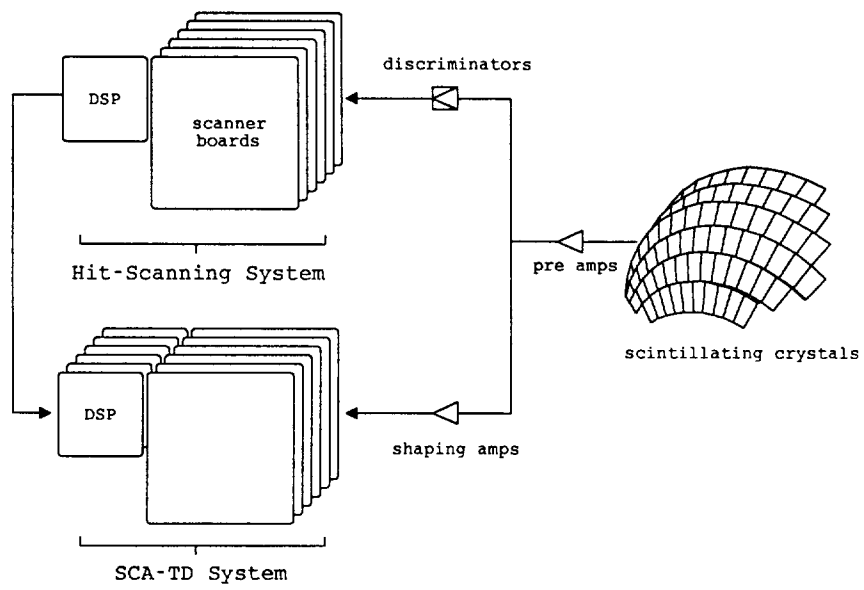


Fig. 1. Overview of the hit-scanning system.

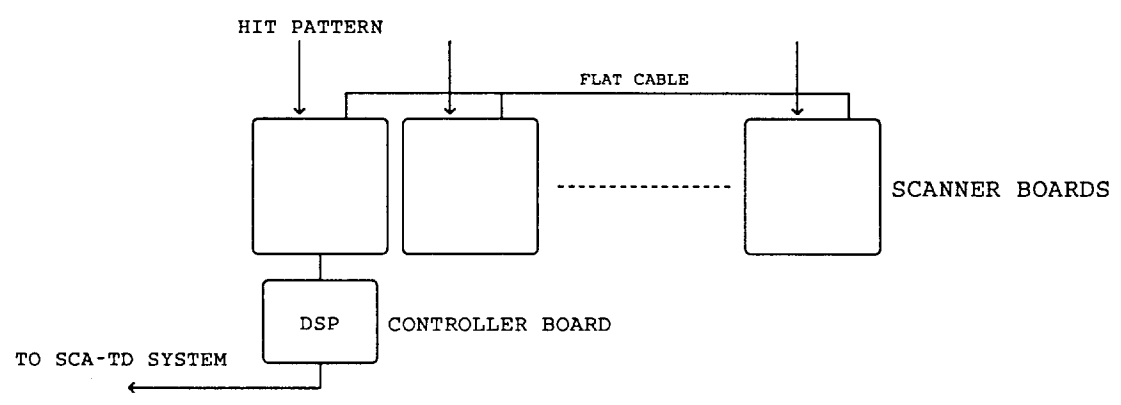


Fig. 2. Schematic layout of the hit-scanning system.

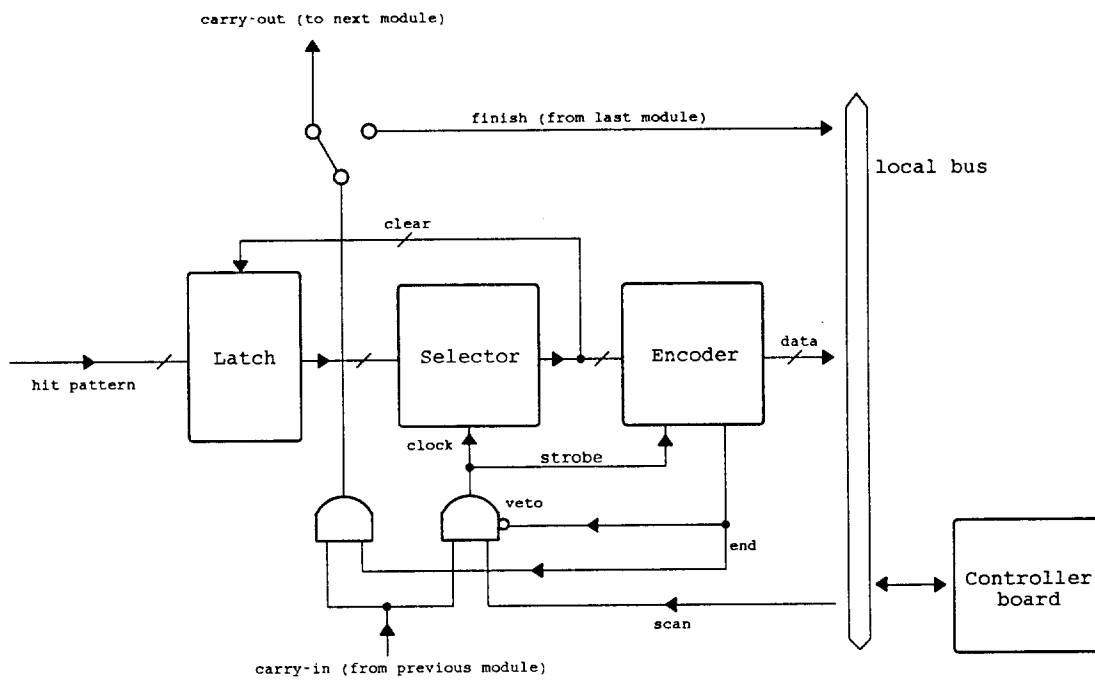


Fig. 3. Schematic logic diagram of the scanning logic.

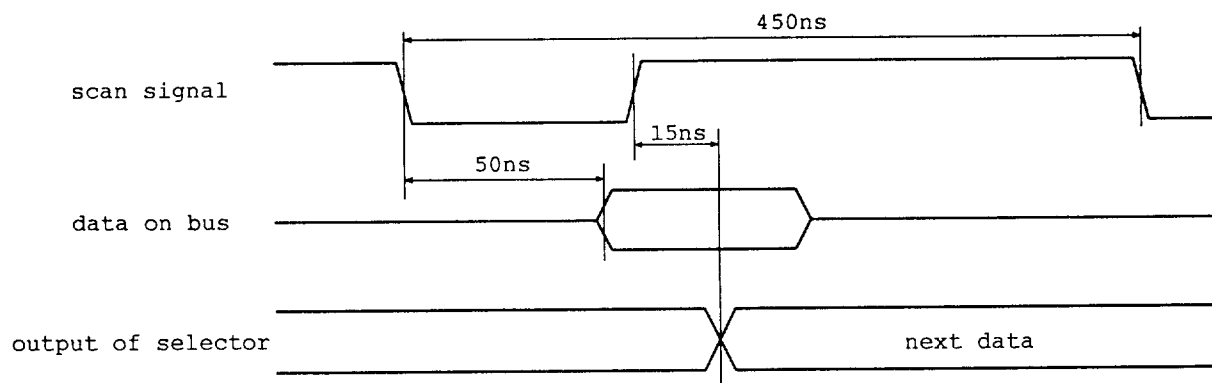


Fig. 4. Timing diagram of the scanning process.

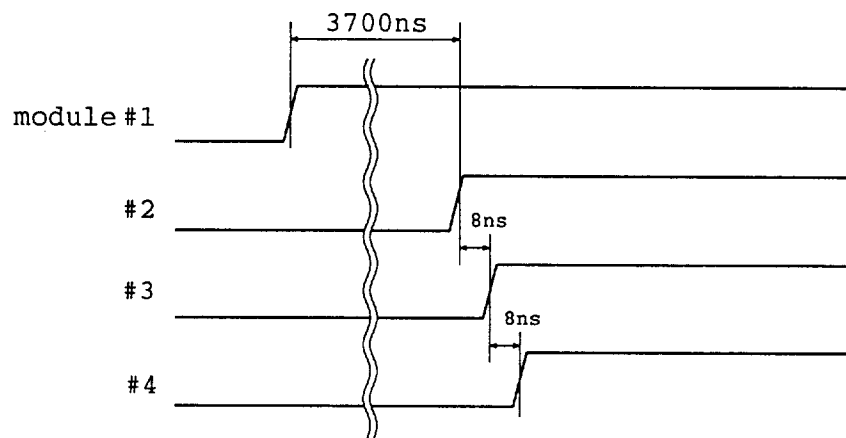


Fig. 5. Timing diagram of the carry-signal transfer for the example case mentioned in the text.