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A Switched Capacitor Based Charge-to-Time Converter

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Abstract

A readout scheme that employs switched-capacitor-array integrated circuits and a simple voltage-to-time converter to capture, delay, and time-encode analog waveforms is described. Test results from a 16-channel prototype board are presented.

1 Introduction

The first-level trigger decision times of many upcoming high-energy and nuclear physics experiments will be one microsecond or more. For timing (digital) signals, trigger latencies of this order are readily accommodated by the new generation of pipelined time-to-digital converters (TDC's) [1–3], which are typically capable of common-stop multi-hit operation and have full-scale ranges of several microseconds. However, the delay of analog signals presents a more difficult problem. The traditional approach of transmission-line delay cables is impractical for delays much beyond 500 ns, especially for systems with large numbers of channels. Although less bulky, lumped delays are costly and suffer from poor fidelity.

One solution to this problem is to use flash analog-to-digital converters[4,5] (FADC's) to encode the signals in real time followed by digital "pipeline" memories to achieve the requisite delay. Alternately, monolithic charged-coupled device[6,7] (CCD) or switched-capacitor array[8–10] (SCA) circuits can be used to store and delay the analog information while awaiting a trigger. Such systems are capable of good performance, are reasonably compact, and can potentially provide a wealth of useful information regarding the input waveform. However, they are often costly on a per-channel basis and generally require on-board processing for zero suppression to avoid overwhelming downstream elements of the data-acquisition system.

In this paper we describe a simple SCA-based system that is designed to work with commercial pipelined TDC's (for example LeCroy Models 1877 or 3377[1]). This approach combines pulse-height and timing information into a single TDC channel, thereby eliminating the need to develop a separate data acquisition path for the pulse-height information. A small amount of control logic is needed to drive the SCA's address lines (for a description of SCA operation see references [8] and [9]) and to control the readout sequence. However, this function is common to all channels in the system and needs to be implemented only once.

2 Circuit Operation

A block diagram of a single channel is shown in figure 1. The figure also shows the common control block. Figure 2 is a timing diagram showing sample waveforms at selected points in the circuit of figure 1.

The analog input voltage is split into two paths, one intended for high-speed timing and the other for pulse-height and/or pulse-shape extraction. The timing path is straightforward, consisting mainly of a timing discriminator, the details of which will depend on the application at hand. In applications where the use of a dedicated discriminator module is desired, the timing signal may be brought in as an external digital input. Alternatively, the timing path can be eliminated altogether since timing information can be derived by multiply sampling the input pulse.

The pulse-height path signal is routed to the input of an SCA. These devices, which were developed at Nevis Labs, are described in detail in references [10] and [11]. For present purposes it suffices to note that from a functional point of view, each SCA channel is equivalent to 128 sample-and-hold circuits or analog storage cells. Before receipt of a Level 1 trigger, the storage cells are addressed in a sequential round-robbin fashion such that at any given time the history of the waveform over the last 128 samples (6.4 μs for a 20 MHz sampling clock) is resident in the array.

When a Level 1 trigger is received, the control logic switches the mode line ($R/\overline{W}$) from write to read. At that point the SCA read address is set to

correspond to the event time—i.e., to the current time minus the Level 1 latency time—and the voltage stored on the first cell to be read is converted to a timing pulse. This is accomplished by driving the inverting input of a comparator with the SCA output voltage and the non-inverting input with a ramp. The output of the comparator is routed to an external multi-hit TDC. For a linear ramp, the time at which the comparator fires is directly proportional to the pulse height (plus a constant offset). Other time *vs.* voltage responses can be achieved by changing the shape of the ramp signal. We note that since the ramp signal is common to all channels, the usual concerns about non-linear transfer functions (complexity, ease of calibration, and channel-to-channel reproducibility) are greatly reduced.

Multiple samples can be read by repeating the cycle just described. Multi-hit TDC's are typically capable of recording eight to sixteen hits per channel, which should suffice for most applications. If more samples are desired, however, they can be obtained by emptying (i.e., reading) the TDC hit memories and then executing additional read cycles.

SCA's with separate read and write address lines are capable of simultaneous read/write operation. Although in the interest of simplicity the design of our current control logic does not take advantage of this feature, doing so would permit effectively deadtimeless operation [8,10]. Once again, the added "complexity cost" associated with this approach could be amortized over all channels in the system.

3 Test Results

In this section we give "proof-of-principle" test results obtained in a prototype 16-channel CAMAC module. The setup used for these tests is shown in figure 3. The system consists of three CAMAC modules, a pulser and a shaping amplifier. All but the SCA Q/T board are commercial modules. The control logic is implemented in a LeCroy 2366 Universal Logic Module (ULM), which incorporates a Xilinx 4005 series field programmable gate array (FPGA). A number of control registers are implemented in the FPGA to allow changing the Level 1 delay, the number of samples to be read, etc. Digital signals are passed between the modules over differential ECL twisted-pair transmission lines.

Figure 4 shows the output of the SCA and the corresponding TDC input signal from the output of the voltage-to-time converter. Although the dependence of the output pulse width on SCA output voltage is not visually striking, the 0.5 ns least-count and 16-bit dynamic range of the TDC [1] affords pulse-height resolution on multiple samples at the 11-12 bit per sample level, taking

full advantage of the intrinsic dynamic range of the SCA.

The linearity of the system is shown in figure 5, where the output time is plotted as a function of input pulse height. The data were obtained by inserting a passive attenuator between the pulser and the input of the shaping amplifier. From pedestal measurements an r.m.s. timing error of $\sigma_t = 0.92$ ns (equivalent to $\sigma_v = 1.45$ mV) has been observed. Combining this with the $\sim$ 3.5-V-full-scale range of the SCA, we infer an overall dynamic range of approximately 11 bits.

4 Large-Scale Implementation

An important goal of this work was the development of a circuit suitable for systems with large channel counts. To this end, we have sought a design that is physically compact and requires a minimum number of components. The SCA IC incorporates eight channels into a 30 $\times$ 30 mm^2 84-pin package and requires only an external buffer amp (available four to a package) and a comparator for the voltage-to-time conversion (also available four to a package), plus the usual DC biasing and bypassing circuitry. Thus it appears that for the packaging options most frequently employed in HEP experiments (CAMAC, FASTbus, VME, etc.), the number of channels per board will be limited by the availability of front-panel connector space rather than board area for components. Although the SCA is a custom IC, a number of labs have developed suitable designs, and nearly all of these can be fabricated in readily accessible, low-cost, CMOS processes.

In its simplest form, this technique can be used to apply a double-correlated sampling approach directly to a charge-sensitive preamplifier output or to acquire a single sample at the peak of a shaped pulse (to minimize errors due to the asynchronous relation between the sampling clock and the sampled pulse, the sampling clock period should be less than about 10% of the peaking time). On the other hand, if circumstances dictate, several samples can be acquired and more elaborate pulse-analysis algorithms applied. We note that the same hardware will perform all of these functions with minor changes in control firmware.

5 Summary and Conclusions

We have designed, built, and tested a SCA-based charge-to-time converter circuit that works in conjunction with a commercial TDC. The proposed approach offers 11-bit pulse-height resolution and can be used to extract timing

and pulse-shape information. The proposed design is both cost effective and flexible.

6 Acknowledgements

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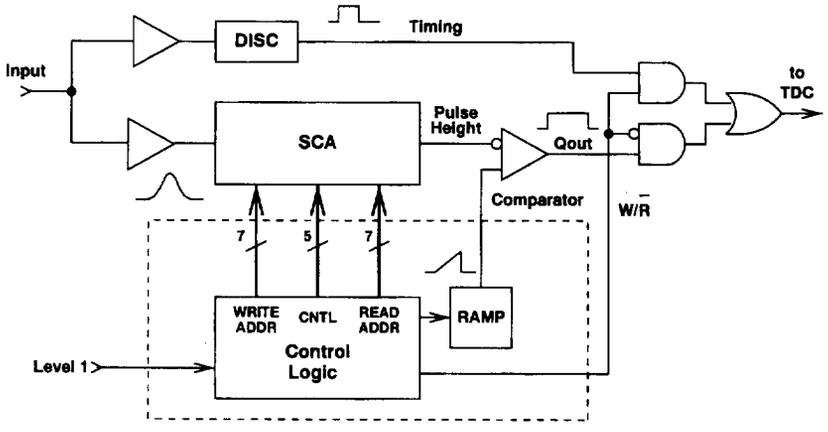

Fig. 1. Block diagram of the SCA charge-to-time converter.

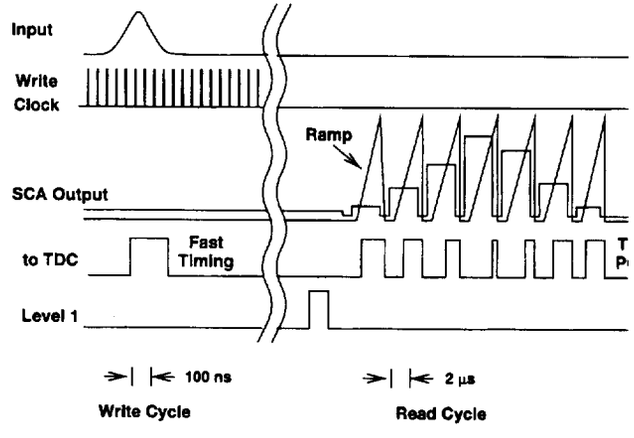

Fig. 2. Timing diagram of the SCA charge-to-time converter.

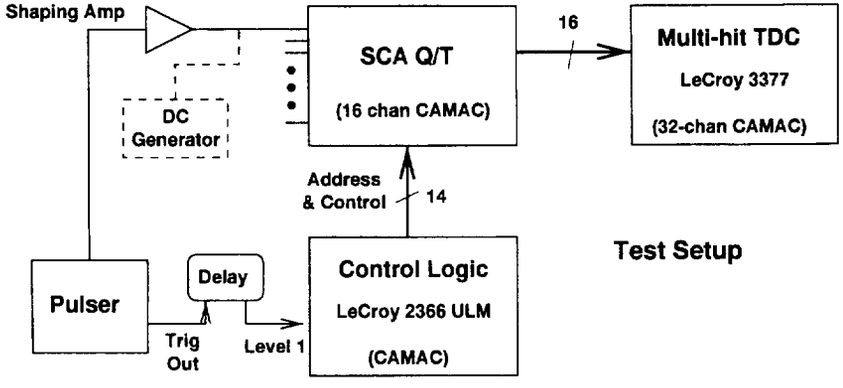

Fig. 3. Block diagram of setup used for proof-of-principle tests. The modules are controlled and read by a personal computer (not shown).

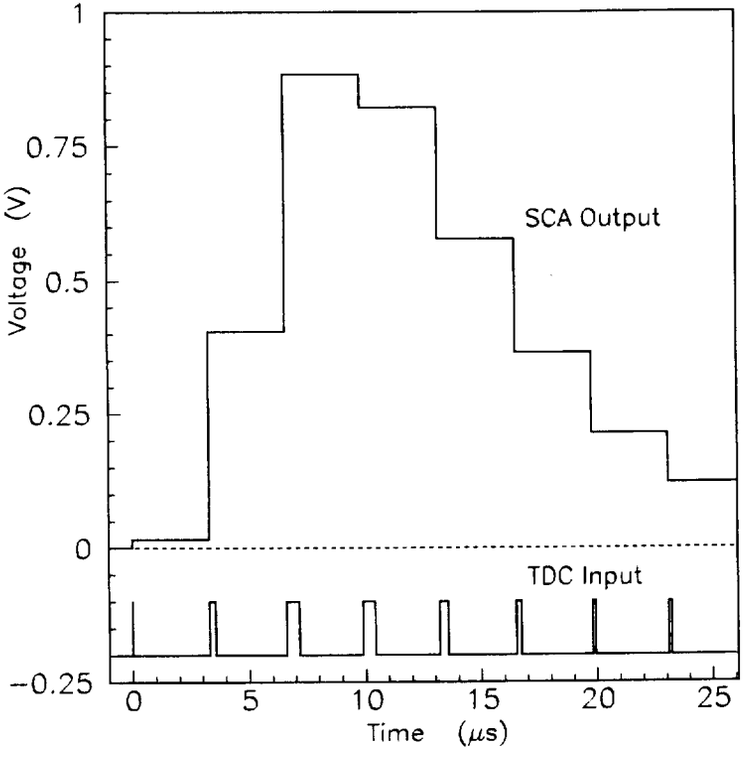

Fig. 4. Sample waveform from the prototype setup. The SCA output waveform corresponding to the captured output pulse from a shaping amplifier is shown in the upper part of the figure. The input sampling rate was 10 MHz. The lower part of the figure is the corresponding TDC input (voltage-to-time converter output).

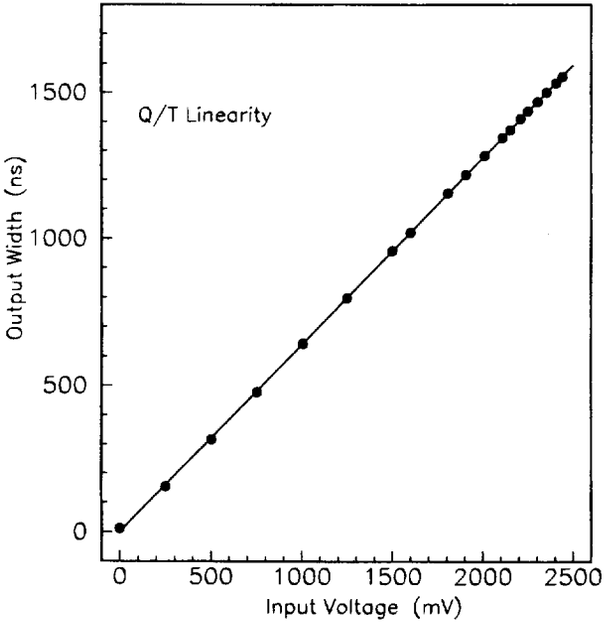

Fig. 5. Pulse time *vs.* input pulse height response for the system.