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DMILL, A Mixed Analog-Digital Radiation Hard Technology for High Energy Physics Electronics

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Abstract

Physics experiments under preparation with the future LHC (Large Hadron Collider) require a fast, low noise, very rad-hard, mixed analog-digital microelectronics VLSI technology.

On the basis of the first R&D started in 1989, a Consortium bringing together the CEA (Commissariat à l'Energie Atomique), Thomson-TCS (Thomson CSF Semiconducteurs spécifiques) and IN2P3 (National Institute for Nuclear Physics and Particle Physics) has been created in 1992 to develop and to industrialize DMILL technology (Durci Mixte sur Isolant Logico-Linéaire), a new rad-hard analog-digital technology especially designed to meet these High Energy Physics requirements.

DMILL uses an SOI substrate and integrates monolithically rad-hard analog-digital CMOS, JFET and bipolar transistors. CMOS and bipolar transistors, with electrical characteristics close to modern BiCMOS technologies, have been chosen to allow the design on the same chip of both analog and digital fast rad-hard circuits. JFET transistors permit designs of low noise very rad-hard circuits for room or cryogenic temperature operation. Results obtained for prototype circuits dedicated to ATLAS or CMS readout electronics confirm the very good adaptation of DMILL to LHC requirements.

The DMILL project was presented to the DRDC in May 1992, and accepted by the CERN Research Board in June [1]. A first Status report was presented to DRDC in October 1993 [2], followed by a short progress report in September 1994. This paper reports on the progress of the DMILL project since October 1993, and presents its industrialization schedule. The main efforts in this project since October 1993 have been concentrated on the final optimisation of each DMILL devices, and on the stabilization of the process in the development laboratory. This stabilization is now close to completion; the start of the industrial transfer is foreseen mid-1995, it will be completed mid-1996 and will be followed by the industrial qualification, which will be completed at the end of 1996. DMILL will be available at industrial site for prototyping or production from 1997 onwards.

To make possible the development of prototype circuits dedicated to ATLAS or CMS by laboratories involved in LHC developments, a first MPC (Multi Project Chip) was organized in 1994 with DMILL technology. Two new MPCs have been organized in 1995 and two other MPCs will be organized in 1996 to allow these laboratories to carry out their works with DMILL up to its industrial availability.

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1. RECALLING OF OUR GOALS

As described in the R&D proposal of our project [1], RD29 is supported by a Consortium bringing together three divisions of the CEA: DSM-Saclay (Matter Science Directorate), LETI-DTA (Advanced Technology Directorate) and Centre d'Etudes de Bruyères-le-Châtel; IN2P3 (National Institute for Nuclear Physics and Particle Physics) and the Thomson-TCS (Thomson CSF Semiconducteurs spécifiques) firm.

The goal of this Consortium is to develop and to industrialize DMILL, a new rad-hard analog-digital technology specially dedicated to High Energy Physics Electronics [3,4,5,6,7]. DMILL Technology integrates monolithically rad-hard CMOS, PJFETs and NPN bipolar transistors, together with two families of rad-hard resistances and capacitances. These components have been chosen for their complementary properties which offer a large degree of flexibility in circuits design thus making it possible to meet the particularly severe requirements imposed for ATLAS or CMS readout electronics. The electrical and radiation hardness characteristics of DMILL components have been chosen to meet the hard LHC specifications [8,9,10,11].

The planning of the development and the industrialization of DMILL foresees the end of the industrial transfer and qualification of the technology for the end of 1996. DMILL will be available at industrial site from the beginning of 1997, in agreement with the LHC planning. For the pre-industrial period, to allow the laboratories engaged in the construction of ATLAS or CMS to continue the development of prototype circuits with DMILL technology for these detectors, the Consortium has organized MPCs (Multi Project Chips) for these users since the end of 1993. This organization of MPCs will be maintained until the technology is available industrially.

2. SUMMARY OF THE TECHNICAL WORKS PERFORMED SINCE OCTOBER 93

The technical work done on DMILL since October 1993 has been directed to optimization of components, simulation parameters and design rules; characterization of DMILL sensitivity to transient radiation effects like Single Event Effects (SEU), production of demonstrator circuits for ATLAS or CMS, and stabilization of the process. The organization of the Consortium for carrying out these works is summarized in Appendix 1.

2.1 Components optimization

In October 1993, in the presentation of the last complete DMILL status report, the technology already included all its final constituents. However, some of these still required optimization:
- the CMOS included a gate with a minimum length of 1.2 µm; this minimum length was reduced to 0.8 µm to reach the speed and integration density of sub-micronic technologies. The hardness of these components was already compatible with requirements for the central part of LHC detectors. It was, however, decided to improve it further with the goal of not having to make allowance for shift of the electrical simulation parameters with ionizing doses up to at least 10 Mrad (10^5 Gy).
- The NPN bipolar transistors had a somewhat too high Rbb' base resistance that has been reduced. The hardness of these components, which was already compatible with central detectors requirements, has been further improved.
- The JFETs met the specified objectives.
- The electrical and hardness characteristics of the resistances and capacitances meet the requirements.
- Anti-ESD protection devices have been tested on digital circuits. The study of these devices has continued and been extended to the analog field.

The optimizations carried out for these different components were prepared at the end of 1993 using several technological process simulators (Suprem-3, Bipole, Suprem-4/Athena and Pisces/Atlas) and were then verified by actual processes in 1994. The results of these optimizations are given in section 3.

2.2 Optimization of simulation parameters and design rules

With the electrical parameters supplied to DMILL users in December 1993, these were able to carry out suitable simulations of their circuits. The parameters furnished were SPICE level 3 parameters for CMOS, SPICE JFET parameters for JFET, and SPICE Gummel-Poon parameters for bipolar transistor. Capacitances, parasitic capacitances and resistances were also described. However, some laboratories using DMILL requested optimization of these parameters to increase the accuracy and precision of analog circuit simulations. A new methodology for extracting simulation parameters was developed by the Leti to meet this request [3]. Using this methodology, a new set of parameters has been established in January '95. In one hand it takes into account the last component improvements mostly dedicated to radiation hardness, and in the other hand improvements in analog modelling of CMOS transistors have been made as far as SPICE level 3 allows it. Non-SPICE models are now under study for CMOS transistors to further increase the precision of analog circuits simulations.

The 1.2 µm design rules used for DMILL in 1993 were modified to obtain a first 0.8 µm set, mainly for the CMOS, but also for bipolar and JFET. These new rules take into account the trench structure isolation used instead the mesa structure in order to improve the integration density. Some rules may possibly change, depending on electrical results and processing yield.

A design rules verification file has been developed with the Cadence DIVA software. It includes the Design Rules Checking (DRC), several verifications of transistors, the extraction of the layout and its comparison with the schematic (LVS). The extraction of parasitic capacitances are also performed in the extract part. More informations are included in the extracted view, which allow the recalculation of model parameters. Until now, a full back-annotation (recognition of models of all kind of transistors, parasitic capacitances, calculation of drain and source capacitance) and re-simulation have been made in the 4.3 version of Analog Artist. This verification file has been successfully tested on a pixel matrix integrating 23,000 transistors. The next improvement may be the development of a software which will translate the extract file to a standard ELDO or HSPICE netlist.

2.3 Characterization of DMILL sensitivity to transient radiation effects

In addition to the hardness of its components to *cumulated* radiation effects, DMILL uses a silicon on insulator substrate (SOI) which was chosen to reduce its sensitivity to *transient* radiation effects. Indeed, single protons or heavy ions are liable to induce temporary electrical perturbations (spurious signals or upsets of memory state) or, in some cases, permanent destruction (by a latch-up mechanism) in circuits made on a bulk silicon substrate. The use of SOI substrate strongly reduce or in some cases completely avoids the probability of occurence of such mechanisms. Measurement of the sensitivity of DMILL to transient radiation effects was performed using a dynamic shift register irradiated with a proton beam. First results are given in section 4.

2.4 Study of demonstrator circuits dedicated to ATLAS or CMS

Circuits for testing the performances of DMILL technology as parts of the applications required for ATLAS or CMS inner detector acquisition channels were studied by DMILL users and submitted to Fermion or Higgs reticles. A part of these circuits were tested before and after gamma-ray irradiation in the first quarter of 1995. Complementary irradiations of circuits issued from boson reticle (processed in 1993) were also made in 1994. Preliminary results of these works are given in chapter 4.

2.5 Stabilization of the process

1994 and the first quarter of 1995 were largely devoted to stabilization of the processing within the laboratory (CEA-Leti). This stabilization was carried out by processing and characterizing numerous batches from Boson, Fermion and Hadron reticles. From october 93 to march 95, 12 electrical batch of SIMOX wafers were processed at Leti for DMILL technology, with 4 different sets of reticles:

- One set with NMOS only in order to study the 0.8 µm LDD technology (1 batch).

- One set with BiCMOS + PJFET transistors, integrating both 1.2 μm and 0.8 μm components and circuits to validate the design rules and process simulation (7 batches); the last two batches begin the stabilization phase of the technology.
- Two sets of reticles with complex circuits:
  . "Fermion" reticle, mainly dedicated to users members of DMILL Consortium (2 batches).
  . "Hadron" reticle, mainly dedicated to users non members of DMILL Consortium (2 batches).

These batches made it possible to show the reproducibility of the electrical characteristics and of the radiation hardness of the components and to carry out the preliminary statistical analyses of the process yield.

2.6 Organization of MPCs for laboratories involved in LHC developments.

MPCs have been organized with DMILL technology for laboratories involved in LHC developments. The organization of these MPCs is described in section 5.

3. RESULTS OBTAINED FOR COMPONENTS:

As mentionned in section 2.1, new improvements were prepared on DMILL components at the end of 1993, using technological process simulators, and were then verified by actual processes in 1994. We give here the main results of these optimizations.

3.1 CMOS transistors.

a/ gamma irradiation at room temperature (^{60}Co source)

As for tests performed in 1993 on CMOS issued from the boson reticle, two different bias conditions were used during irradiation and post-irradiation annealing of CMOS transistors issued from optimized batches (1994):

	NMOS		PMOS	
	Analog bias	Digital bias	Analog bias	Digital bias
Vgs	+1.5 V	+5 V	-1.5 V	-5 V
Vds	+5 V	0 V	-5 V	0 V
Vbs	0 V	0 V	0 V	0 V

Fig. MD1 to MD4 show typical values of the threshold voltage shift versus irradiation dose and typical values of the relative variation of transconductance versus irradiation dose, measured within 1 hour after each irradiation step, on NMOS and PMOS issued from the improved DMILL process.

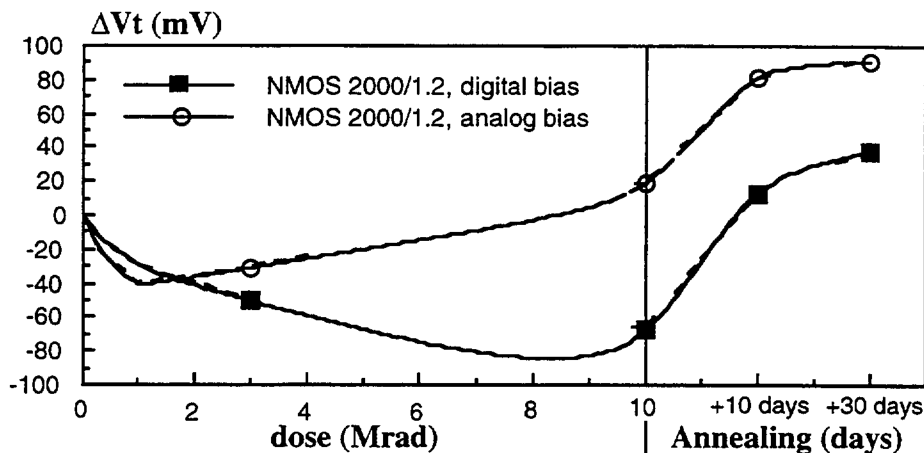


Fig. MD1: ΔVt (dose) for NMOS using two different bias conditions.

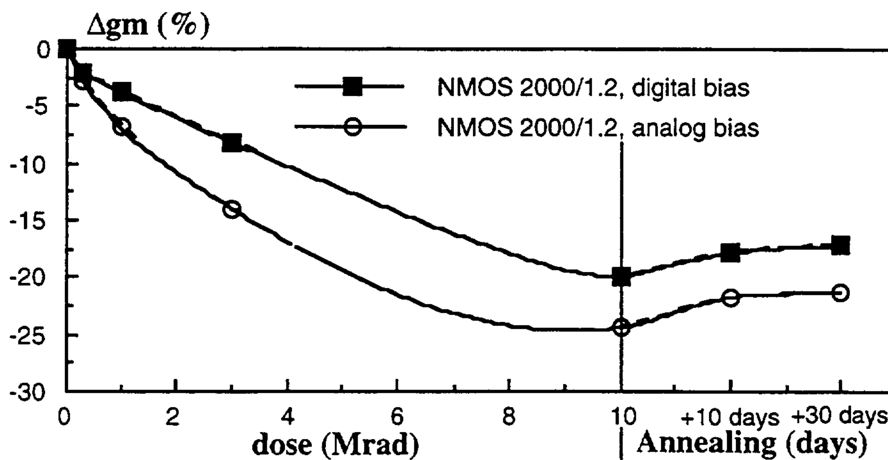


Fig. MD2: Δgm (dose) for NMOS using two different bias conditions.

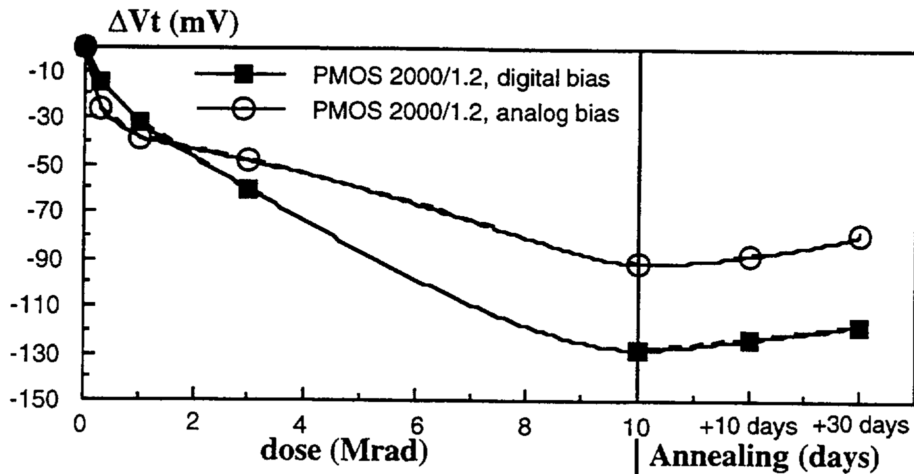


Fig. MD3: ΔVt (dose) for PMOS using two different bias conditions.

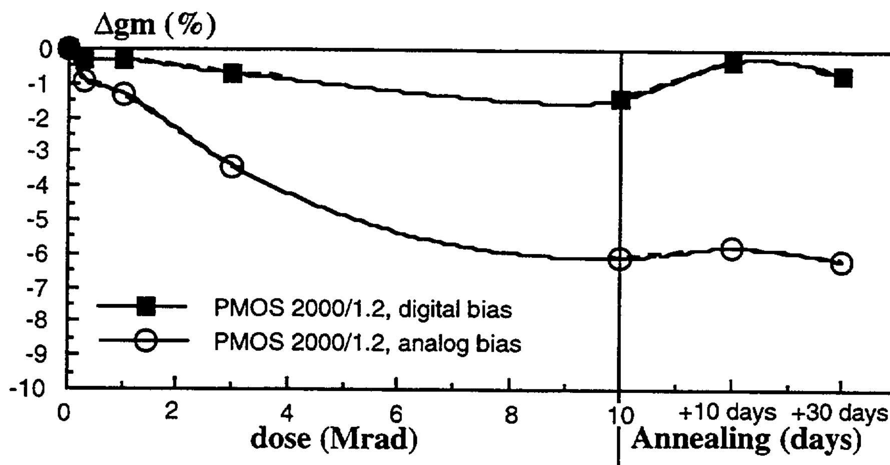


Fig. MD4: Δgm (dose) for PMOS using two different bias conditions.

After 10 Mrad + 30 days annealing, the maximum Vt shift remains less than 80 mV for NMOS and less than 130 mV for PMOS (worst bias case), and the maximum Δgm remains less than 25% for NMOS and less than 7% for PMOS (worst bias case). These characteristics demonstrates the significant improvement of the radiation hardness resulting from the works performed on DMILL in 1994. The small ΔVt induced on these devices by gamma irradiation up to 10 Mrad(SiO2) is now typically in the range of the precision of Vt obtained on standard CMOS technologies. This good stability of Vt permits to make not allowance for the Vt shift induced by gamma irradiation up to 10 Mrad, for the electrical simulation of circuits.

b/ Noise characteristics.

Fig. MD5 and MD6 show the input noise spectrum measured on NMOS and PMOS transistors sized with W/L = 5000/3. During noise measurements, these devices issued from the improved process were biased with a 100 µA drain current and a +4 volts (PMOS) and -4 volts (NMOS) body contact bias. Before irradiation, we have measured a γ factor of 0.79 and a corner frequency of 40 KHz for NMOS, and a γ factor of 0.76 and a corner frequency of 2.1 KHz for PMOS. The theoretical value is $\gamma = 0.66$. After 10 Mrad(SiO2), these values are slightly modified: we have measured a γ factor of 0.92 and a corner frequency of 55 KHz for NMOS, and a γ factor of 0.91 and a corner frequency of 19 KHz for PMOS. As a preliminary conclusion, these devices exhibit low noise characteristics, i.e. the improvement of the technology in term of radiation hardness or in term of minimum gate length (now 0.8 µm with the LDD structures) has not affect their low noise properties.

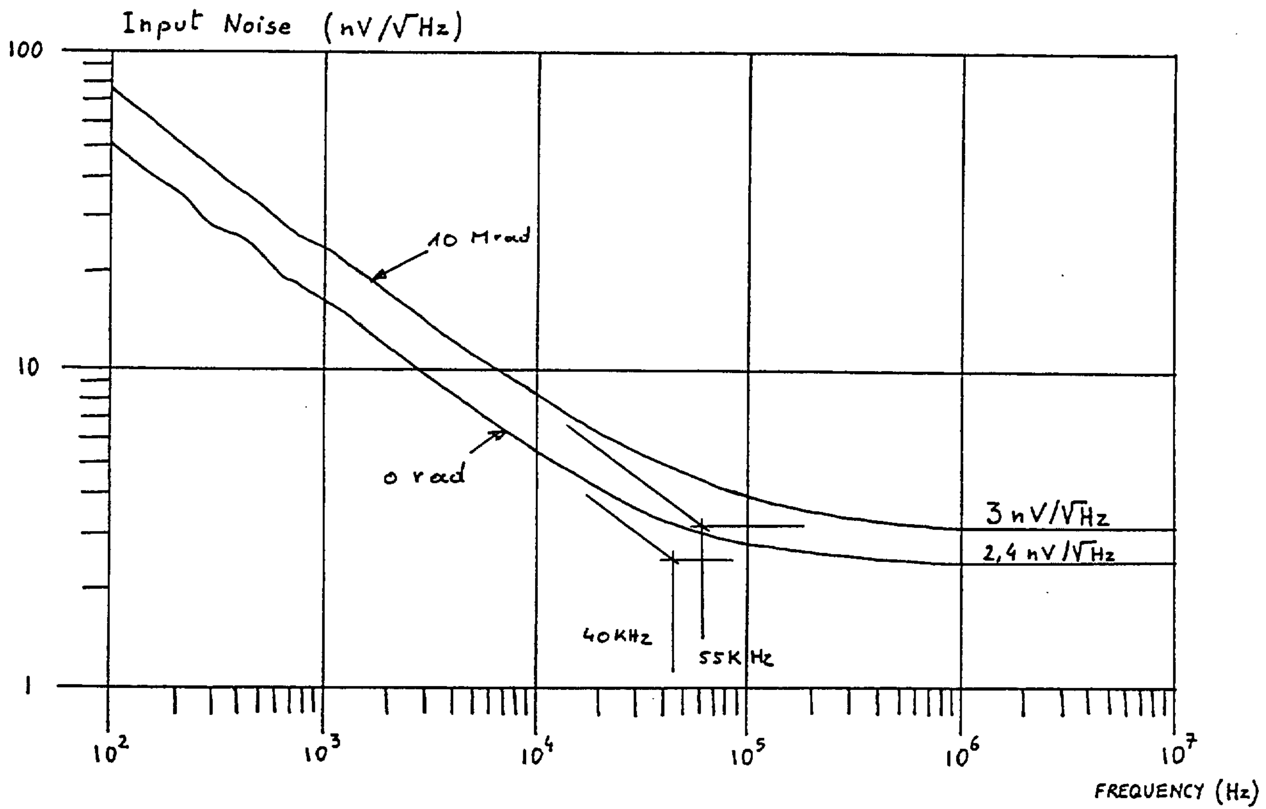


Fig. MD5: NMOS input noise spectrum vs gamma irradiation dose (W/L = 5000/3, Id = 100μA, Vp = -4Volts)

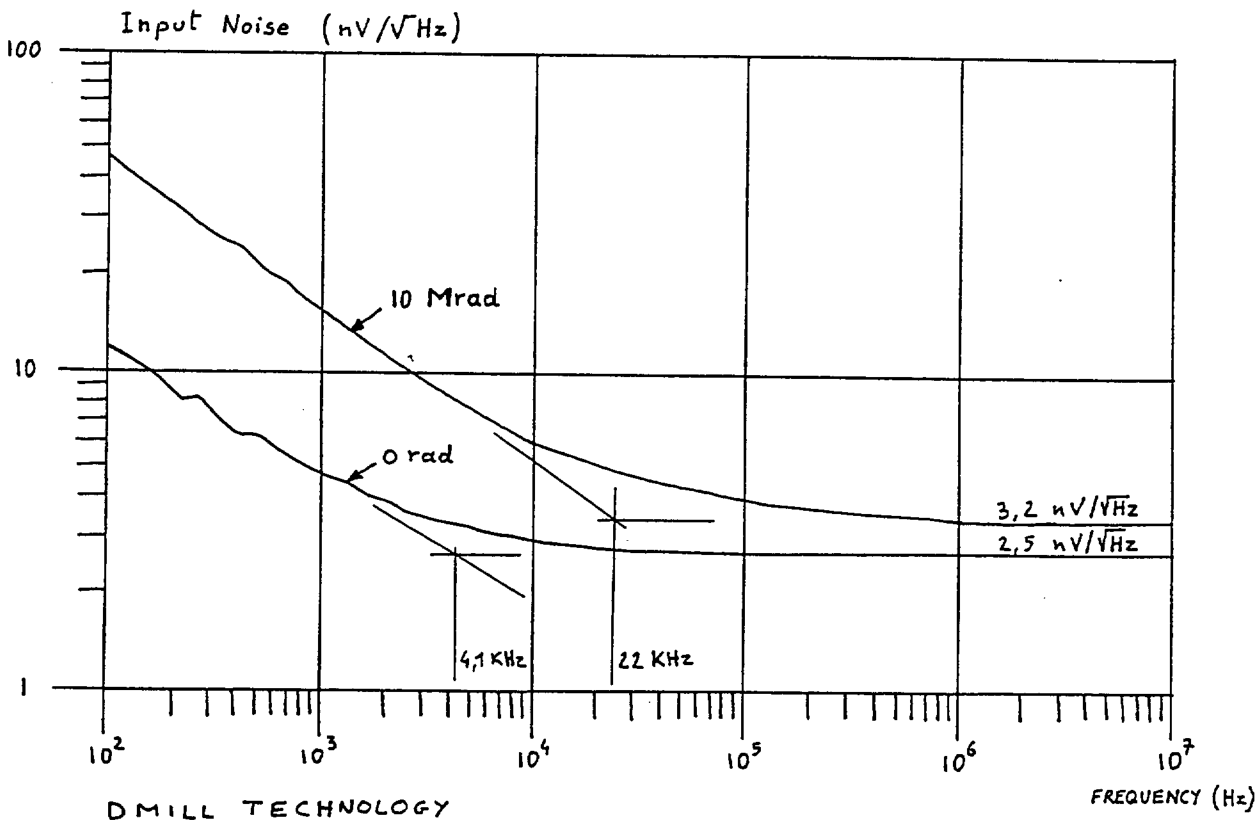


Fig. MD6: PMOS input noise spectrum vs gamma irradiation dose (W/L = 5000/3, Id = 100μA, Vp = +4Volts)

c/ gamma irradiation at cryogenic temperature (^{60}Co source)

The characterization of DMILL technology for operation at cryogenic temperature has been taken place over the past year. Encouraging results were obtained at 90 K on MOS transistors. The stability of the threshold voltage versus temperature has been studied. Tests demonstrate that simple circuits are functional at this temperature. In general the 90 K operation of microelectronic technologies is a key point for calorimeters (LAr or LKr) readout electronics, which should not only be operational at this temperature, but also rad-hard. On the radiation hardeness side, extensive work has been done to study the influence of dose rate. This could favourably affect the radiation response of elementary devices and consequently of circuits. Experiments are currently under way to investigate the response of MOS devices at liquid argon temperature to a long duration radiation exposure. The same tests are currently under way for elementary circuits. In this context, Saclay, in close association with the ATLAS project, has developped the tools necessary to evaluate on a long time scale the ionizing radiation response of some devices and circuits. These experiments use facilities available at the COCASE ^{60}Co irradiation source at Saclay, primarily dedicated to the test of crystals for the CMS detector. Dose rates provided by this source are particularly weak, and well adapted to the simulation of the LHC radiative constraints. First results should be obtained at the end of 1995.

d/ neutrons irradiations.

As discussed in our previous status report, CMOS are not sensitive to neutrons [2].

3.2 NPN bipolar transistors.

a/ gamma irradiation (^{60}Co source)

We have tested several sizes of NPN bipolar transistor under gamma irradiation. During irradiation as well as during post-irradiation annealing, these devices were biased with Vbe = +0.7 V and Vce = +5 V. Figure MD7 show the evolution of the current gain ß (Ic) with the ionizing dose for an NPN bipolar transistor sized with a 10*1.2 µm2 emitter surface. For a collector current Ic = 10 µA, the initial current gain measured on this device was 150; after 10 Mrad(SiO2) this gain current for the same Ic was slightly reduced, with a final value of 110. This final value is almost unchanged after 1 month annealing.

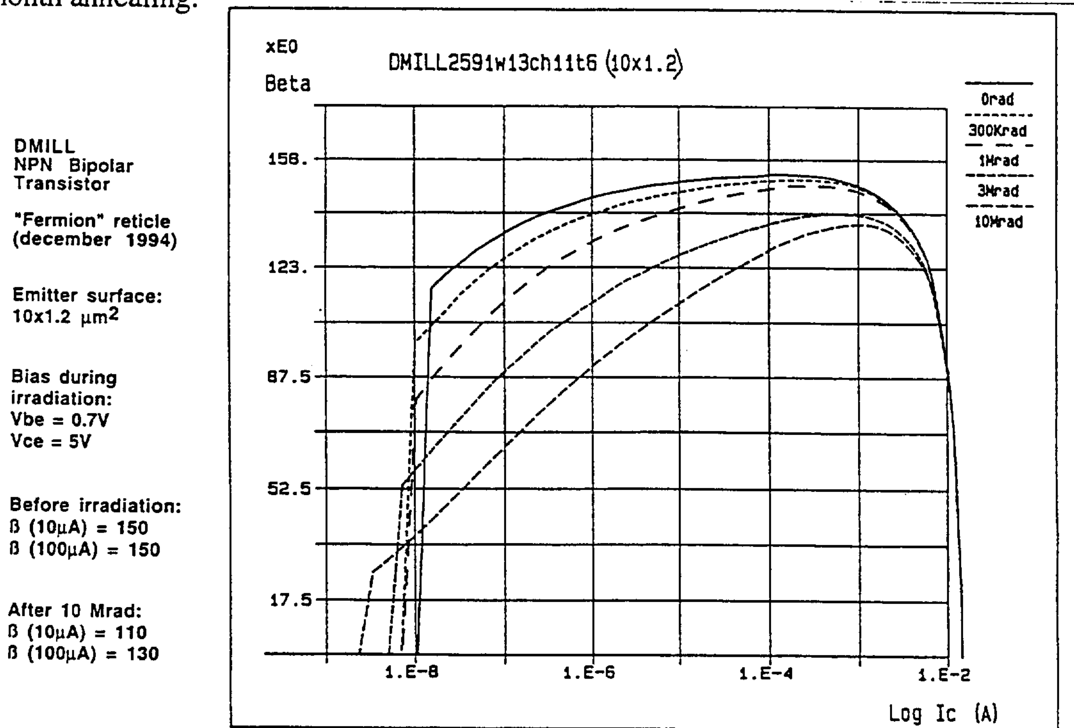


Fig. MD7: evolution of ß(Ic) versus gamma irradiation dose for an NPN bipolar transistor, emitter surface = 10*1.2 µm^2.

b/ Noise characteristics.

Fig. MD8 shows the input noise spectrum measured on the same NPN bipolar transistor sized with a 10*1.2 µm2 emitter surface. During noise measurements, this device issued from the improved process was biased with a collector current Ic = 100 µA. As expected for a bipolar transistor, this device exhibit a noise figure without low frequency term. This noise figure is not affected by gamma irradiation. The thermal noise measured with this device is Snv = 2.1 nV/√Hz. This value allows to give a maximum value to its base resistance: $Rbb' \leq [(Snv_{measured})^2 - (2kT/gm_{measured})^2]/4kT$; which gives for this device Rbb' ≤ 125 Ohms. As a first conclusion, improvements on the process have lead to bipolars exhibiting a good stability of the current gain ß versus ionizing dose even at low collector current, and a reasonable Rbb' value. This bipolars are well suited for the design of low noise preamplifiers.

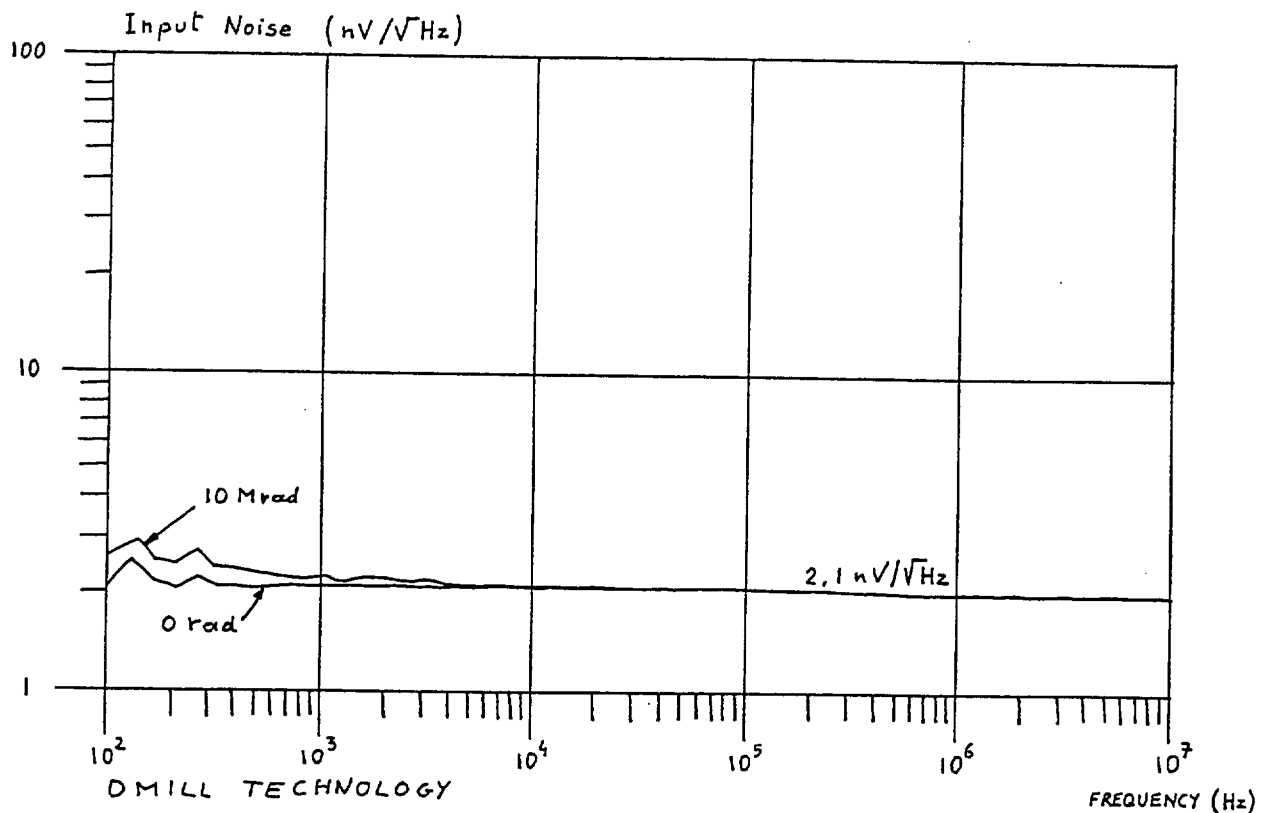


Fig. MD8: NPN bipolar transistor input noise spectrum vs gamma irradiation dose emitter surface = 10*1.2 µm^2, Ic = 100 µA.

c/ neutrons irradiations.(1 MeV)

Figure MD9 show the evolution of the current gain ß (Ic) with the ionizing dose for an NPN bipolar transistor sized with a 1.2*1.2 µm2 emitter surface, issued from previous non optimized batches (1993). The value of the current gain ß of this device was not optimized. For a collector current Ic = 100 µA, the initial current gain measured on this device was ß = 100; after 10^{14}n/cm^2 (1MeV) this gain current for the same Ic was slightly reduced: Δß/ß = -35%, corresponding to a final value of 65. With a such final value, this bipolar remains quite suitable for operation in circuits.

The value of current gain ß of optimized devices is now fixed between 150 and 180. Neutron irradiations of such optimized NPN bipolar transistors are currently under way.

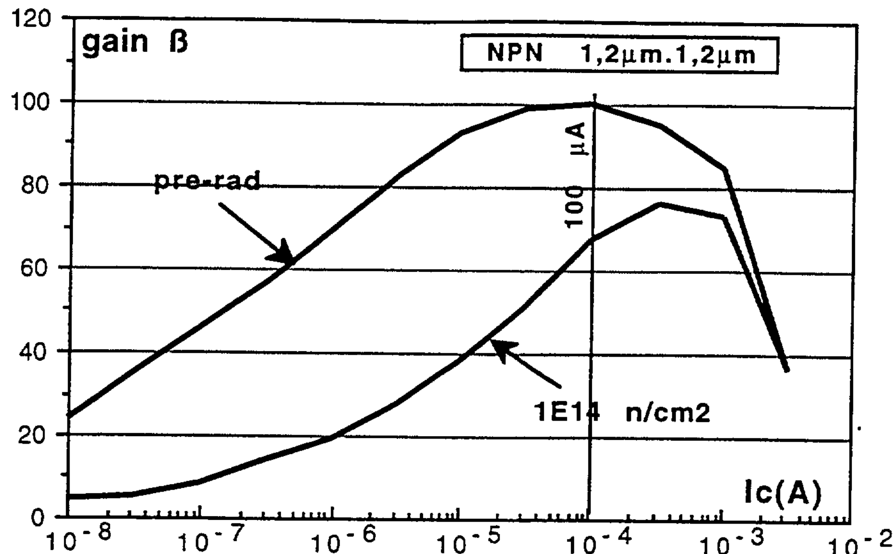


Fig. MD9: evolution of ß(Ic) versus neutron irradiation for an NPN bipolar transistor, (device issued from 1993' batches: non optimized process); emitter surface = 1.2*1.2 μm^2.

3.3. PJFET transistors.

The radiation hardness characteristics of PJFETs presented in our last status report [2] remain valuable: JFETs exhibit a very low sensitivity to gamma, neutron or proton irradiations.

Additional noise measurements have been performed on PJFETs with different W/L. Fig. MD10 shows the input noise spectrum measured on a PJFET sized with W/L = 2000/1.2 and biased with a drain current of 400 µA, before and after irradiation up to 10 Mrad(SiO2). Before irradiation, the thermal noise was 1.9 nV√Hz and the corner frequency Fc = 1 KHz. After 10 Mrad(SiO2), the thermal noise is unchanged and the corner frequency is slightly increased: Fc(10 Mrad) = 30 KHz.

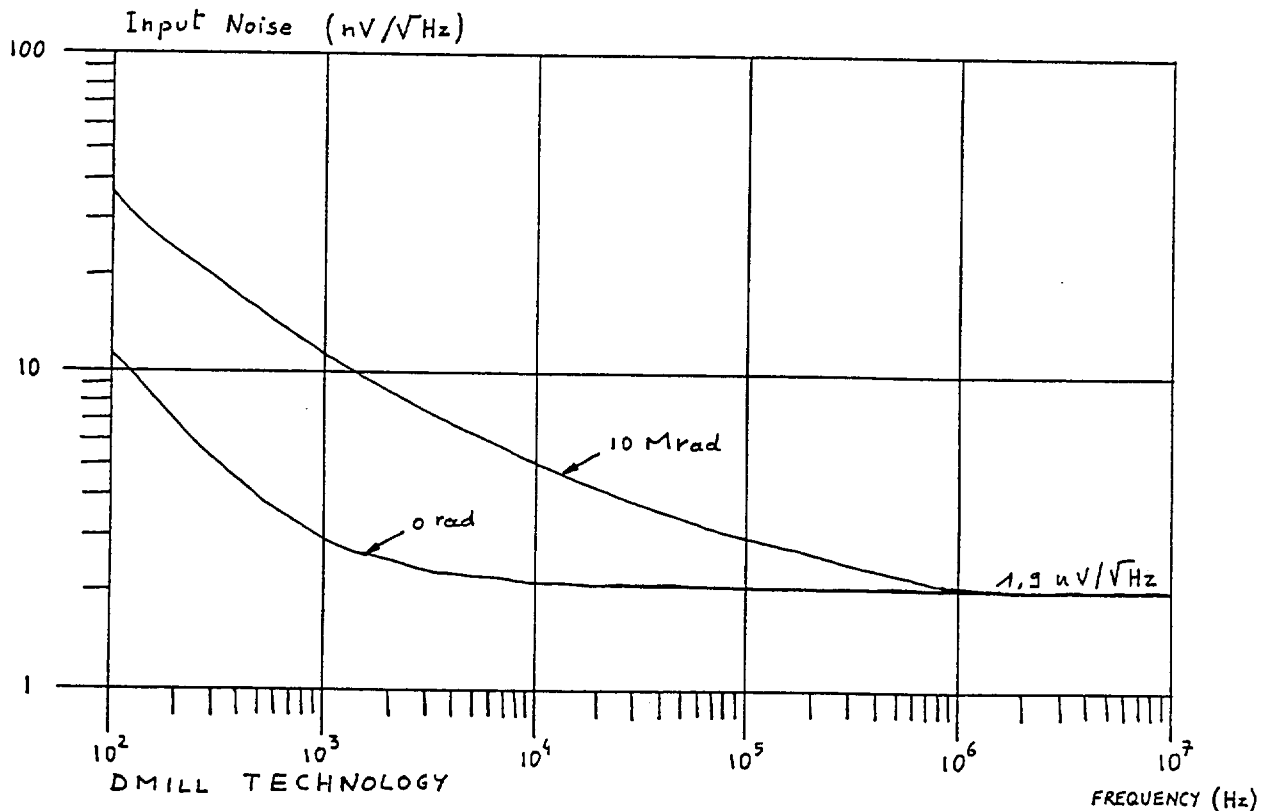


Fig. MD10: PJFET input noise spectrum vs gamma irradiation dose
W/L = 2000/1.2; Id = 400 µA.

3.4. Resistances and capacitances.

a/ Resistances:

The absolute value of resistances designed with P-substrat or with DSP in Fermion or Hadron batches is a little bit different from that predicted by parameters of simulation. This difference is mainly due to the change in the effective value of doping level of P-substrat and of DSP; this is an unexpected consequence of the work made on the technology in order to improve the radiation hardness of the various transistors.

Fig. MD11 shows the evolution of resistances made with P- substrate (high resistances) and resistances made with DSP (mid resistances), as a function of ionizing dose, and after post-irradiation annealing. These results concerning devices issued from the optimized process are consistent with those concerning devices issued from the non optimized process presented in our previous status report.

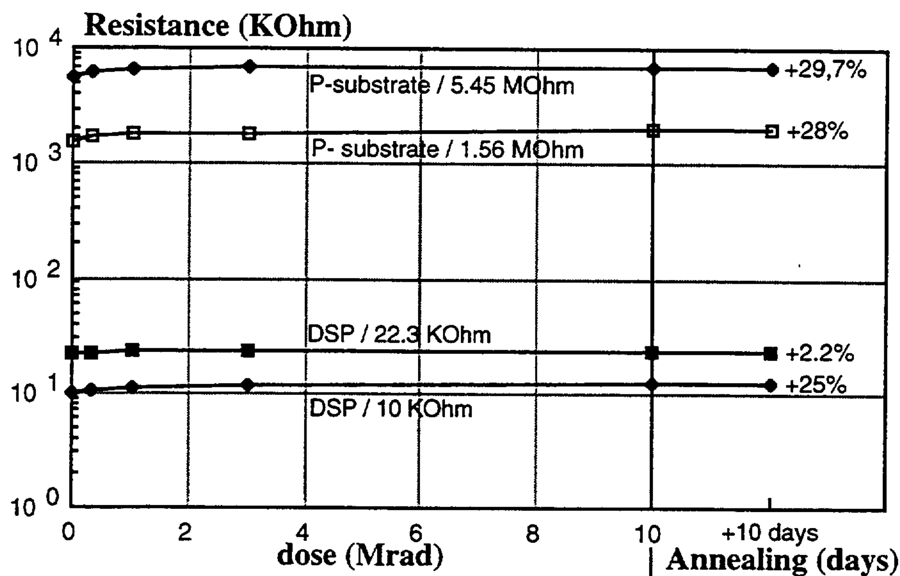


Fig. MD11: evolution of resistances made with DSP or with P-substrate, versus ionizing dose.

b/ Capacitances:

These devices are not sensitive to gamma irradiation nor to neutron irradiations.

3.5. Anti-ESD (ElectroStatic Discharge) protective devices.

The performances of anti-ESD (Electro Static Discharges) input protection devices have been evaluated on different circuits (microprocessors, analog amplifiers, analog devices) from boson reticle (1993). These first results have lead to new structures of protection devices which were implemented in Fermion and Hadron reticles (1994). A protection device is now found for digital circuits. Its size will be optimized through new structures implemented in Higgs and Lepton reticles (1995). A complementary study of the input protection device dedicated to analog circuits will be carried out through new structures also implemented in Higgs and Lepton reticles (1995).

4. RESULTS OBTAINED FOR LHC DEDICATED CIRCUITS

4.1. Digital circuits.

a/ Static digital circuits.

a.1. Results from Fermion Reticle

As in the Boson reticle [2], toggle circuit and by-ten frequency divider (design Saclay) have been implemented in the Fermion reticle processed in 1994. Both these circuits are based on masterslave D-FLIP FLOPs designed with 0.8µm gate length CMOS transistors. They have been irradiated with gamma rays (^{60}Co) up to 10 Mrad(SiO2). During irradiation and annealing, they were operating with a 40 MHz clock frequency (6V supply).
These circuits have been characterized within 3 hours after irradiation for dose up to 10 Mrad(SiO2), and then after 1month annealing at room temperature.

Before irradiation, the power consumption of the toggle circuit was 2.4 µW/MHz (Vdd=3V) which is very close to the simulation predictions (2.25 µW/MHz). The maximum clock frequency, limited by the test bench, was 120 MHz.
After 10 Mrad(SiO2), we didn't find any change in maximal operation frequency nor in power consumption (see fig ED1). This good behaviour is mainly due to the improvement of the NMOS radiation hardness (see chapter 3).

As for the Boson reticle [2], there is no degradation of the rise time for CMOS or BiCMos digital buffers.

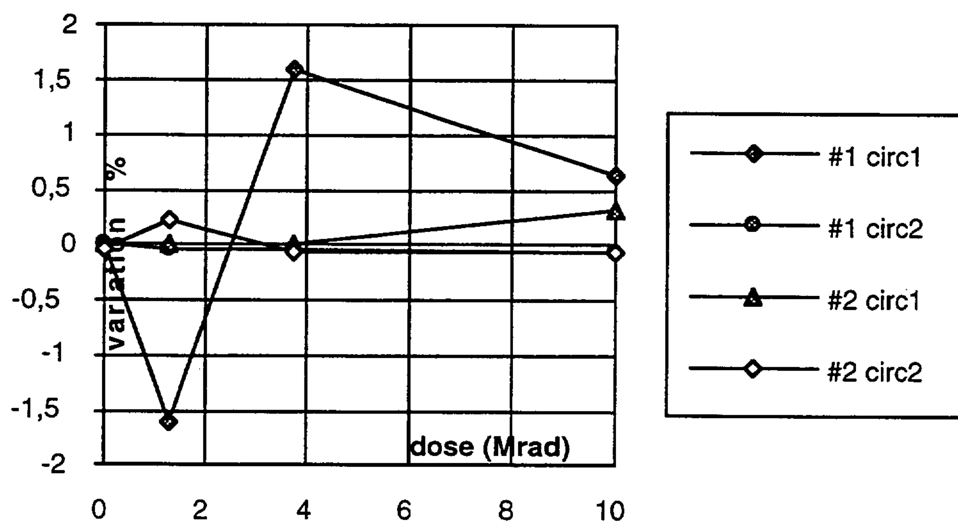


FIG ED1: Relative variation of power consumption with ionizing dose for two circuits from two different sites on a wafer.

a.2. Results from Boson Reticle.

10 Mrad(SiO2) proton irradiation (300 MeV) have been performed on various CMOS digital circuits from Boson reticle, using the Saturne Synchrotron facility (LNS). Results obtained on these circuits are similar to those obtained using an equivalent gamma (^{60}Co) ionizing dose presented in [2].

b/ 16-bits microprocessor.

The improvement of the radiation hardness obtained on DMILL devices in 1994 is clarely confirmed on digital circuits by tests performed on a 16-bit microprocessor up to very high ionizing doses. This microprocessor, which was implemented in each DMILL reticles, is a 29C101 compatible processor; it integrates 11,000 transistors and contains sequential logic, register and static RAM. On reticles processed before 1994 (boson reticle), the failure level was about 30 Mrad. On reticles processed in 1994, the failure level of this circuit is higher than *350 Mrad(SiO2)*.
- On circuits issued from the optimized process, the propagation delay time measured after 150 Mrad is only twice that measured before irradiation.
- One of the most important parameters for device characterization is the minimal supply voltage for complete functionality, Vfmin. Indeed, this parameter is related to the failure level of the circuit. Fig. DAM1 shows the evolution of Vfmin measured on microprocessors from boson (1993, before optimization) and Fermion or Hadron reticles (1994, after optimization). Improvements measured on these circuits are consistents with characteristics measured on transistors.

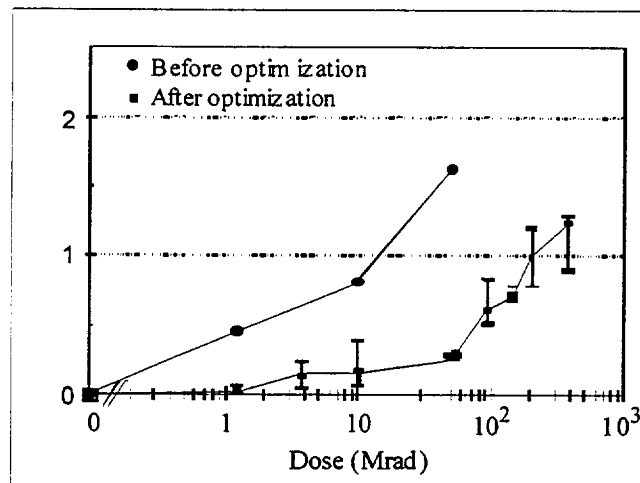


FIG DAM 1: Shift of Vfmin versus ionizing dose.

c/ SEU measurements on a dynamic shift register (design & tests CPPM).

Using a 300 MeV proton beam at LNS facility, we have performed preliminary SEU measurements on a dynamic shift register [13]. The clock frequency was 1 MHz and the dose rate was close to 2.4 10^9 protons/cm^2/s. Fig. LB1. depicts the total number of errors per bit (per D flip-flop) as a function of the integrated flux.

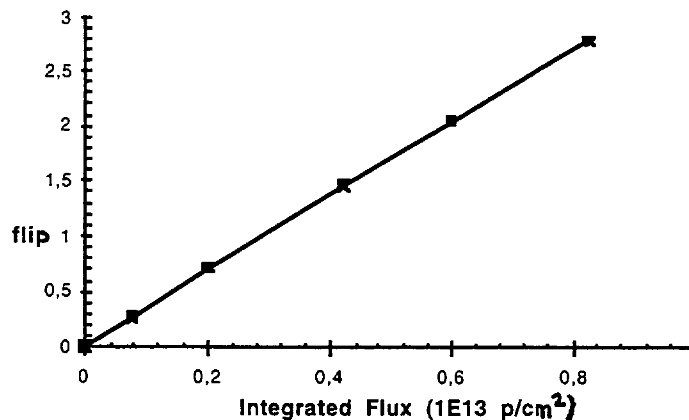


Fig. LB1. Errors per D Flip-Flop

This leads to a cross section of 3.3 10^{-13} errors.cm^2/bit, i. e. 1 error per dynamic D Flip-Flop every 139 hours in ATLAS at 11.5 cm radius from the beam (assuming a nominal luminosity of 10^{34} protons/cm^2/s for LHC) [ref LB2].

If we suppose 10^8 pixels, 2000 pixels hit in one BCO, 10 D Flip-Flop per pixel and a latency of 2 µs for the trigger level 1, the number of 'true' pixels not seen in one BCO is 8.1 10^{-8} and the number of 'false' pixels seen in one BCO is 14.2 10^{-5}. This is totally negligible for pixel application. Nevertheless, further measurements have been carried out. The investigations are carried out to determine how the SEU rate depends from the rise time, the fall time of the clock frequency, and the protons incidence angles.

4.2. Analog circuits.

a/ Charge preamplifiers.

a.1. CMOS and PJFET-CMOS charge sensitive preamplifiers (design & tests Saclay).

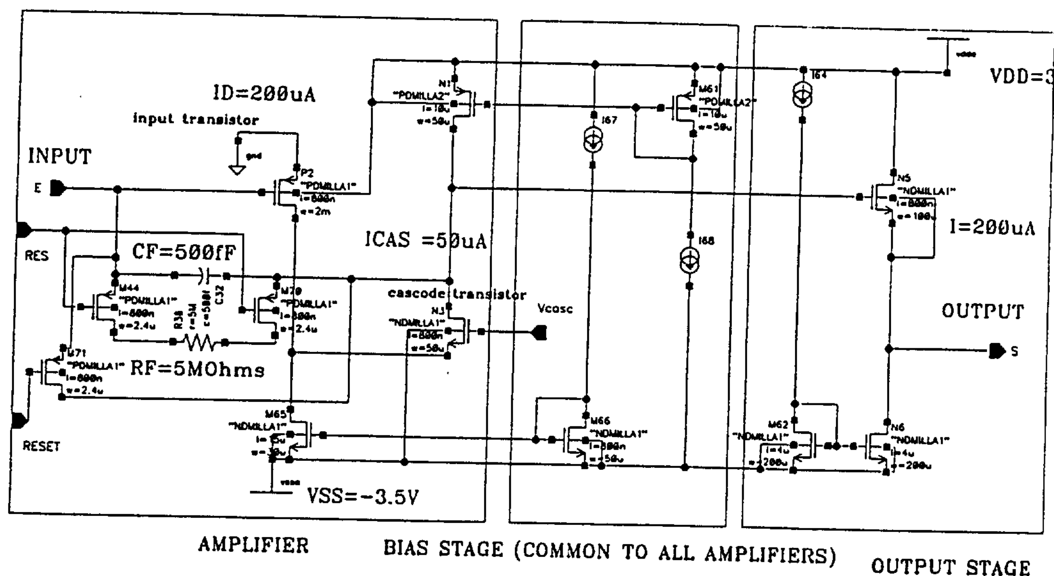


FIG ED2: POTA circuit

Charge sensitive preamplifiers are very well known structures, and are essential part of particle detector readout electronics. Such circuits based on the classical folded cascode structure were already implemented in the boson reticle (1993). We have decided to re-implement these circuits in Fermion reticle, using an improved design (see fig ED2). For these improved circuits, the loads and current source have been more degenerated in order to minimize their noise contribution, and a series of switches has been used in order to allow the use of these circuits with a reset mode or with a very high feedback resistor. To compare the noise performances of the different kind of field effect transistors available in DMILL, three versions of this architecture have been studied : POTA with a PMOS (W=2000µm) input device, NOTA with a NMOS (W=1500µm), and PJFET-OTA with a PJFET (W=2000µm) input device. For the three families, different versions have been implemented with various channels lengths (0.8, 1, 1.2, 1.5 and 2 µm for MOS; 1.2 and 1.6 µm for PJFETs) for the input device.

For all preamplifiers, the input transistor is biased with 200 µA. The NMOS input transistor version operates in moderate inversion.

Measurements performed before irradiation show a good agreement of the transfer function with theory:

(1) Vout= Qin/Cf=0.33μV/e-
where Cf =0.48pF is the feedback capacitance.

The dispersion of this value is less than 1% for different chips of the same wafer.

Theses circuits were irradiated up to 10Mrad(SiO2). They were biased during irradiation as well as during annealing. Measurements after 10 Mrad were performed after a two months annealing at room temperature.

After 10 Mrad(SiO2), the transfer function is unchanged and the DC level shift is less than 100mV.

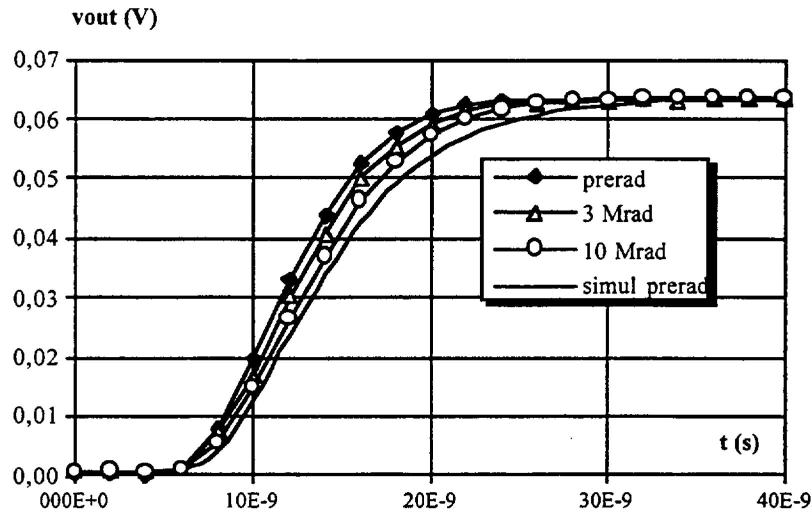


FIG ED3: POTA 1μm: Vout = f(dose) CD=7pF

For all the preamplifiers, the rise time is less than 20ns for a detector capacitance CD=10pF, and is consistent with theoretical values. The little discrepancy with simulation is due to the well known error of the Spice model on the value of transconductance in the moderate inversion region. The variation of this rise time with irradiation is equal to the variation of 1/gm of the input transistor (see fig ED4), as predicted by theory.

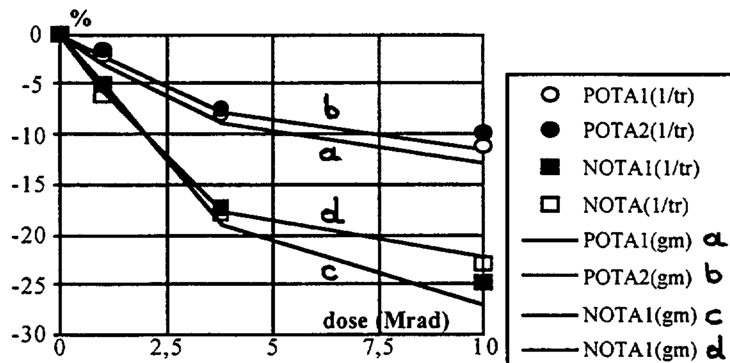


FIG ED4: relative variation of 1/tr and gm with dose (NOTA/POTA)

Noise measurements were performed using the variable time constant CR-RC^2 filter and the measurement set-up developed by C. de la Taille [12]. The fig. ED5 to ED9 show the equivalent noise charge before and after irradiation for the various pre-amplifiers for a detector capacitance of 7pF.

For a same input transistor gate length, although NMOS higher transconductance, the noise performances of POTA and NOTA are equivalent (850 e- rms for tp=25ns). 0.8μm POTA and NOTA performances at high shaping time constants are limited by a high 1/f noise. For fast filtering constants, the most adapted gate lengths are 1 and 1.2μm.

PJFET-OTA noise is higher because of the higher capacitance of the input transistor (almost twice that of PMOS for the same transconductance.) The best geometry for the input device seems to be L=1.6μm.

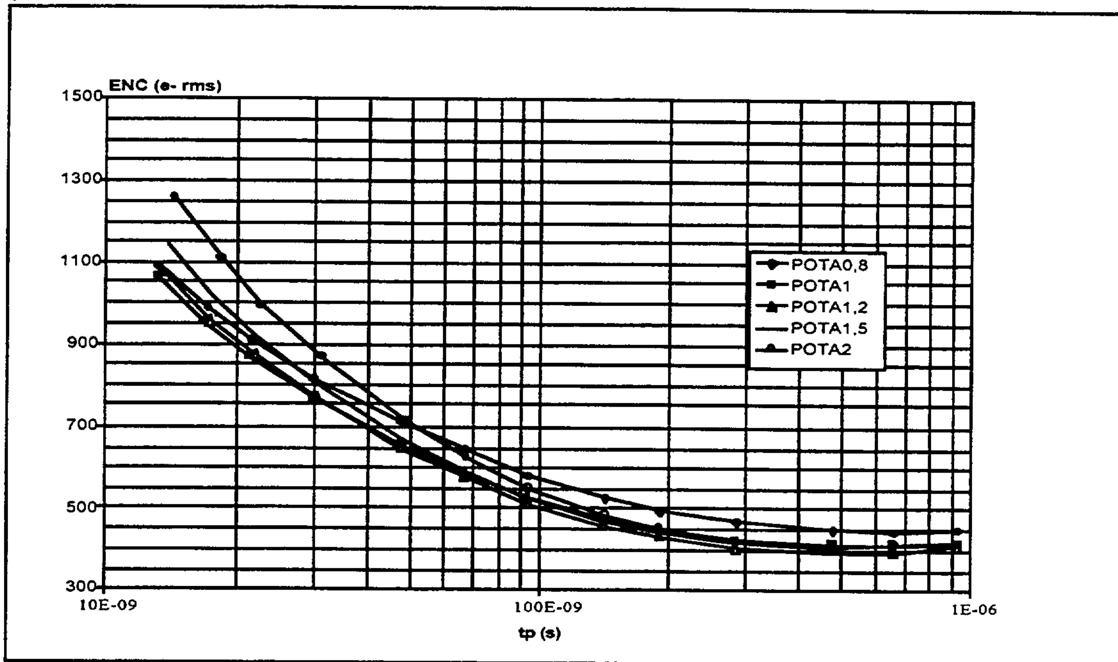


FIG ED5: POTA before irradiation; ENC(tp) vs L (CD=7pF)

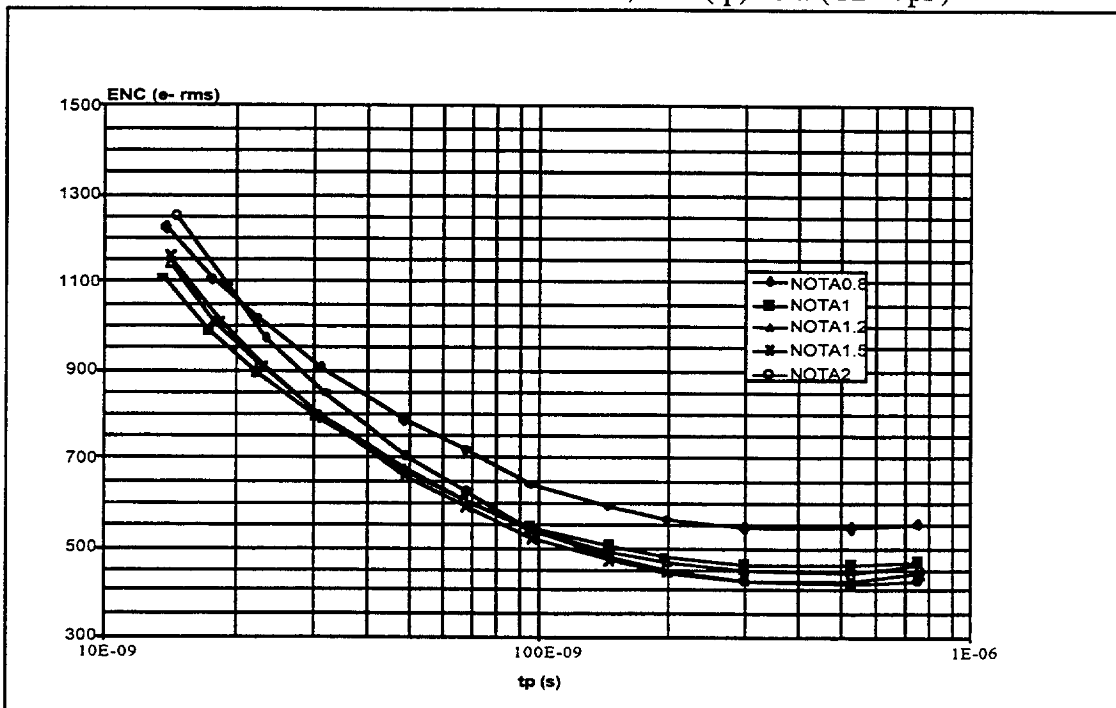


FIG ED6: NOTA before irradiation: ENC(tp) vs L (CD=7pF)

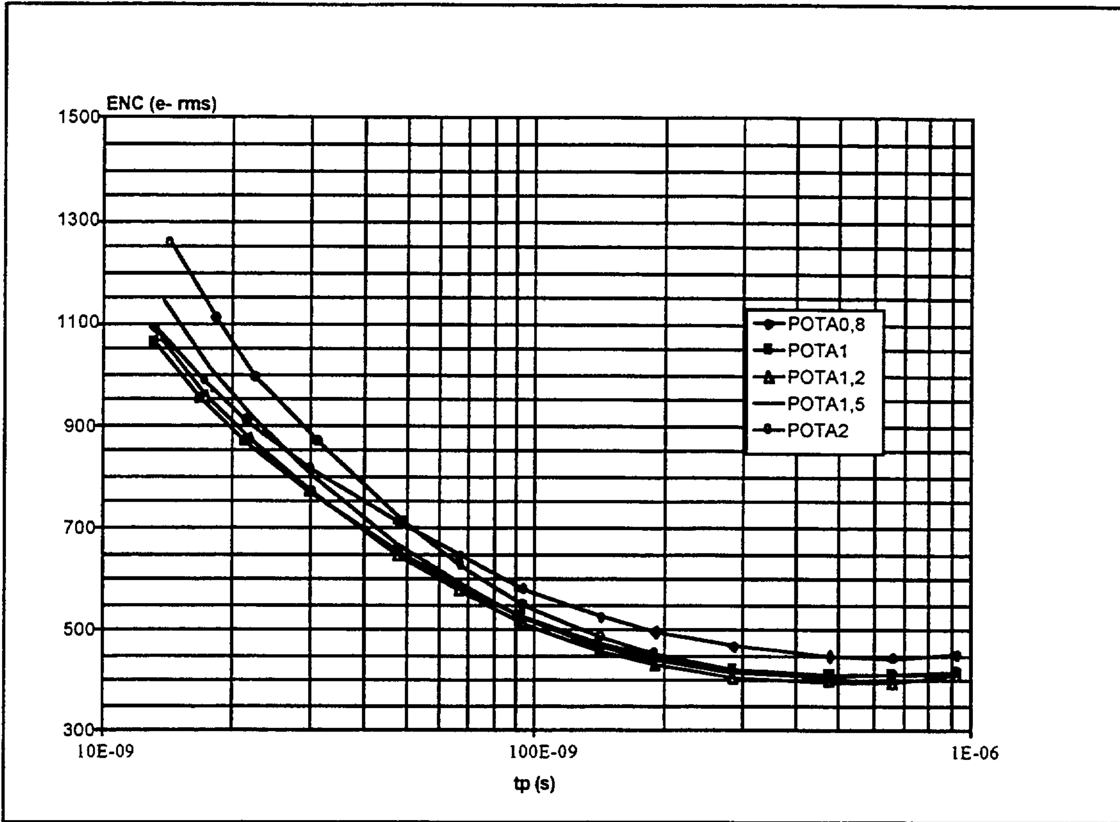


FIG 7: POTA after 10Mrad(SiO2): ENC(tp) vs L (CD=7pF)

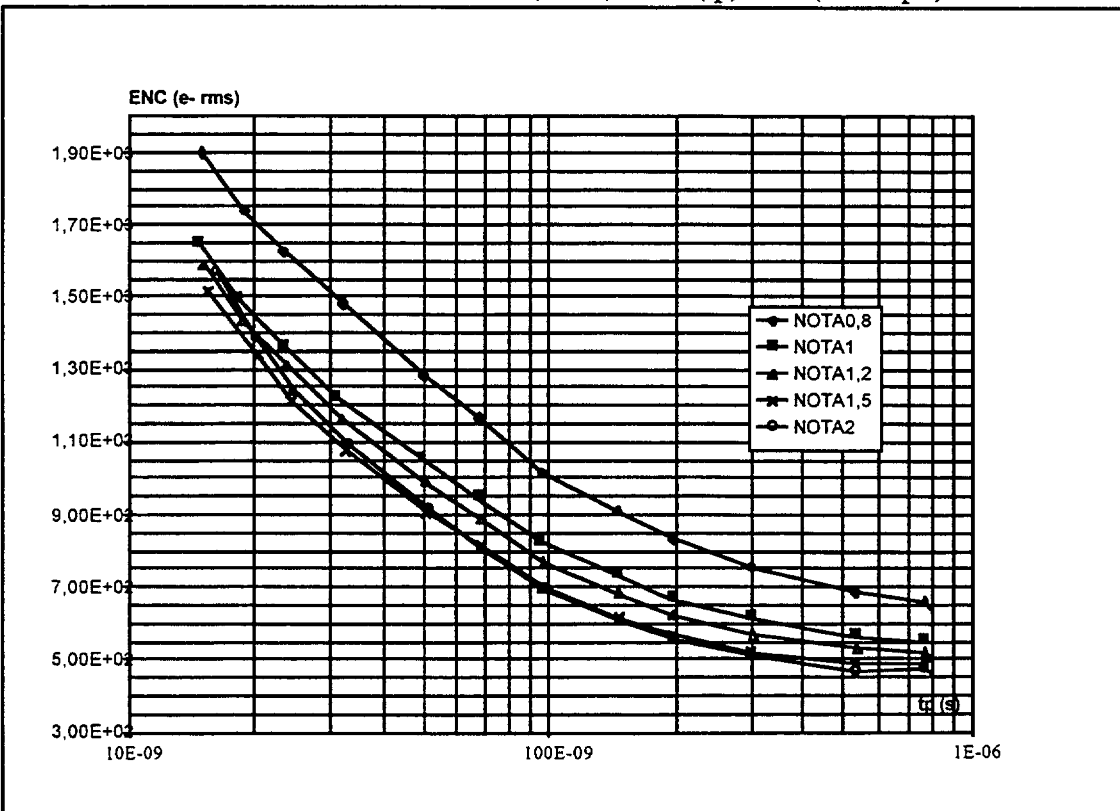


FIG 8: NOTA after 10Mrad: ENC(tp) vs L (CD=7pF)

After a 10 Mrad(SiO2) irradiation, the noise increase is around 15% for POTA and 50% for NOTA. For NOTA, this tendancy is even higher with a submicronic input device. PJFET-OTA noise degradation is only 7%.

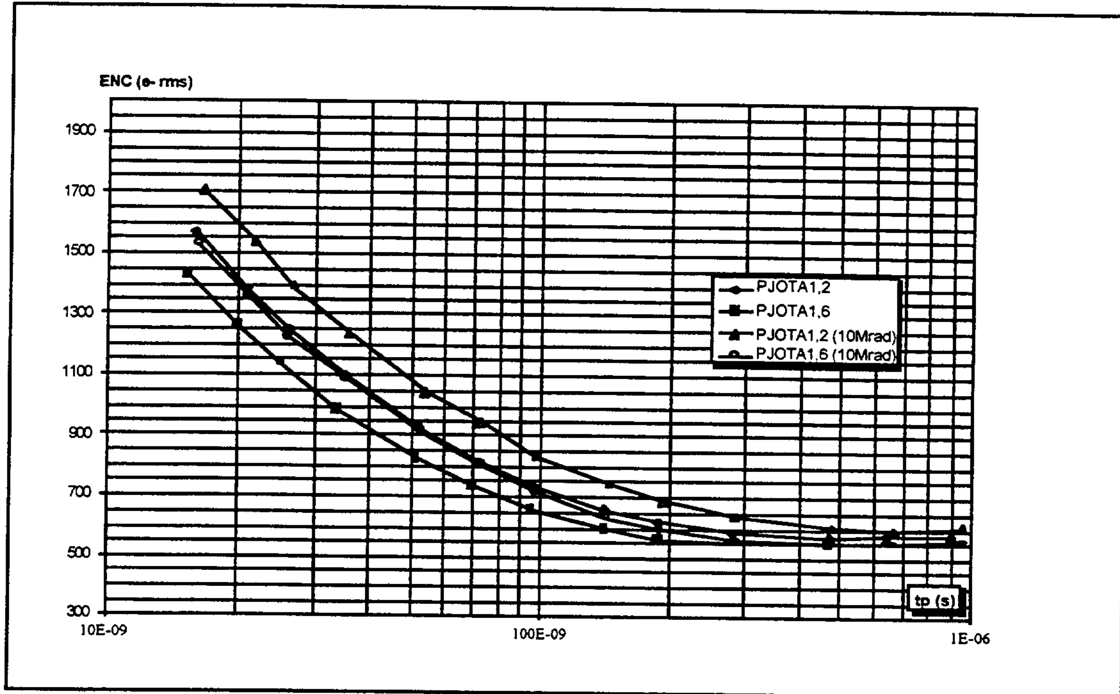


FIG ED9: PJFET-OTA before and after 10Mrad(SiO2): ENC(tp)

The table ED10 presents the ENC versus detector capacitance measured on the various OTA for a tp=30ns peaking time after the filter, before and after 10 Mrad(SiO2) gamma irradiation.

	ENC/pF 0Mrad	ENC/pF 10Mrad	ENC CD=0pF 0Mrad	ENC CD=0pF 10Mrad	ENC(1/f)/pF 0Mrad	ENC(1/f)/pF 10Mrad
PJFOTA1,2	81	91	636	717	16	18
PJFOTA1,6	70	77	622	690	12	15
NOTA0,8	94	151	260	400	50	72
NOTA1	81	125	265	400	38	56
NOTA1,2	78	110	270	390	32	45
NOTA1,5	77	106	290	370	27	37
NOTA2	74	96	354	463	20	26
POTA0,8	82	96	292	341	42	51
POTA1	77	91	216	270	34	45
POTA1,2	76	90	220	260	29	40
POTA1,5	77	87	303	363	25	35
POTA2	75	86	405	491	21	28

Table ED10: ENC vs CD measurements

Because of the fast shaping and of the high value of the feedback resistor, the parallel noise is negligible. So the equivalent noise charge for CD=0 is mainly due to serie noise and preamplifier input capacitance (C of input transistor + Cpad + CF).

This measurements confirm ENC(tp) measurements:
- PJFET-OTAs have a good ENC(CD) slope but a high input capacitance. Their degradation with ionizing dose remains low.
- Before irradiation, for L>0.8µm, all the NOTA and POTA have an equivalent slope. The difference of noise performance come from their input device capacitance.
- After irradiation, The ENC(CD) slope increase is more important for NOTA than for POTA.

The two last columns of this table contain the value of the part of ENC/pF due to 1/f noise. These values have been extracted from a fit on the ENC(tp) curves. They reveals that:
- for tp=30ns, 1/f noise contribution remains negligible even after irradiation.
- the highest 1/f noise is obtained for NMOS input devices whereas the lowest is obtained for PJFETs input devices.
- the increase of 1/f noise with irradiation is more important for NMOS than for other transistors, especially for gate lengths comprised between 0.8 and 1.2 µm.

From the ENC(TP) plots, we have extracted by fit the value of the serial noise density e_n which is only due to the input device. Then we have calculated the noise ideality factor (FIG ED11):

$$\gamma = e_n^2 * gm/4kT$$

where gm is the transconductance of the input transistor extracted on a single device before and after irradiation. This factor should be equal to 2/3 for an ideal PJFET or an ideal MOS operatating in strong inversion and to 0.5 for an MOS operating in weak inversion.

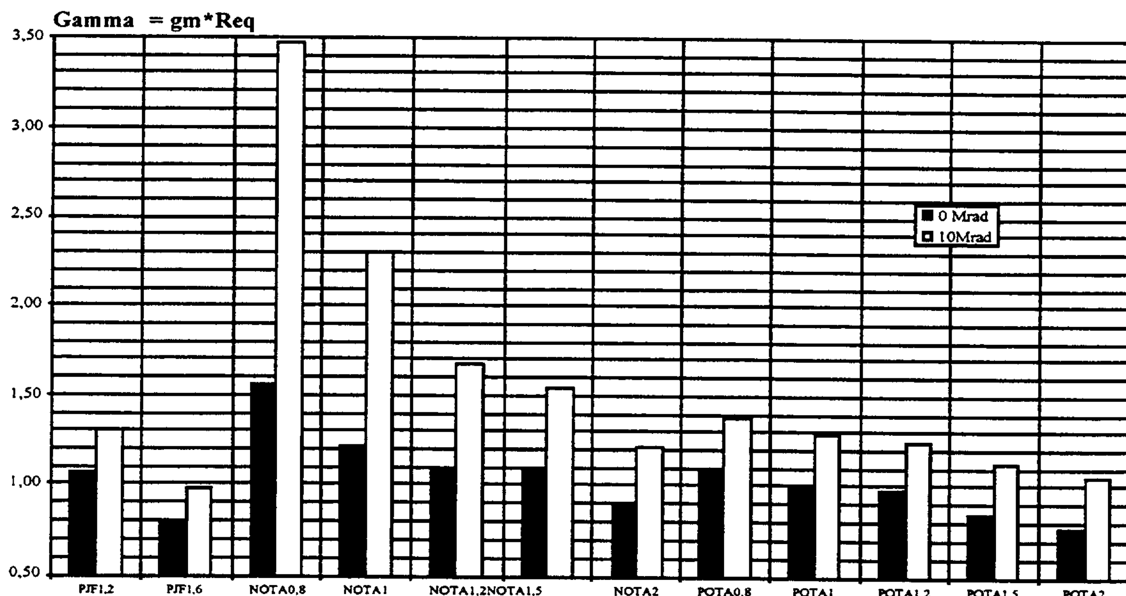


FIG ED11: gamma factor calculated before and after irradiation.

It reveals that:
- 1.6µm PJFETS are very ideal devices.
- PMOS are more ideal than NMOS.
- non-ideality increases when L decreases.
- the noise degradation with ionizing dose is mainly due to the increase of the γ factor (and not to the variation of transconductance)
- the degradation of the γ factor is more important for NMOS than for PMOS.

10 Mrad(SiO2) proton irradiation (300 MeV) have been performed on the various CMOS charge preamplifiers implemented on Boson reticle, using the LNS facility. Results obtained on these circuits are similar to those obtained using an equivalent gamma (^{60}Co) ionizing dose [2].

The first conclusions of this study are:

- For low noise, low CD, low power, fast shaping preamplifiers, the best input transistor is a PMOS with 1 or 1.2 µm gate length.
- Submicronic PMOS or NMOS may be used in applications where noise is less critical (second stages).
- Submicronic NMOS must be reserved to analog applications where a high gm/C ratio is required but where the noise is not critical.
- Because of their bad Gm/C ratio *when biased near the pinch-off voltage*, PJFETs are not suitable for fast, low power preamplifiers. They are more suitable for shaping times larger than 1µs (low 1/f noise) or if they can be biased with a drain current close to Idss (this is possible if there is no power limitation). Works are under progress to reduce the back gate capacitance of PJFETs.

a.2. CMOS charge sensitive amplifier (design & tests LAL).

This amplifier uses only CMOS components; it was designed to be used for low noise read-out of µstrip proportional detectors and Si detectors.

We have performed precise measurements of the equivalent noise charge of this charge amplifier, i.e. the noise contribution of its front-end device (a PMOS transistor in our case). The 1/f noise has also been evaluated. It constitutes the dominant noise of this amplifier at very long shaping times.

Two types of noise measurements have been performed:

- ENC as a function of the input capacitance CD, for a shaping time corresponding to a peaking time tp=450ns
- ENC as a function of tp for a given input capacitance.

From a linear fit, we obtain a total input capacitance (PMOS, strays, package...) of 24,6pF.
The total noise resistance, including the contribution of 1/f noise, is: Rs total = 307 Ohm.
From a fit of the ENC=f(tp) curve, we obtain the value of the noise resistance: Rs=225 Ohm.

The front-end device has a transconductance gm=3.6mA/V at a current of 200µA. The theoretical value of Rs is 0.7/gm = 195 Ohm. That lead to a γ factor of 0.8 which prove the excellent low noise quality of the PMOS transistor.

a.3. PJFET amplifiers (design & tests LAL Orsay; original schematics from F. Manfredi, University of Pavia, Italy)

A collaboration program in the framework of DMILL technology has been set up between the LAL (Orsay, France) and the university of Pavia (Italy). The aim of this program is the realization of low noise preamplifiers tailored to different detector applications and all using a P-channel JFET as front-end element .

A first preamplifier, exclusively based on PJFETs, had already been succesfully integrated and tested in 1993 (boson reticle). It employed at the input a large tetrode-type device (gate width W=50mm, topside and backside gates connected together) to match detector capacitances in the range of hundreds of pF. The preamplifier was proven to have a good noise behaviour and to be adequatly fast. The major limitation in that circuit was the output stage that, being a PJFET source follower, was unable to deal with large signals of both polarities in heavy load conditions.
Besides, the difficulty of realizing an internal voltage shift increased the number of elements that had to be added externally.
As a next step,within the project Fermion, new design solutions were adopted.

First, the all-PJFET preamplifiers was replicated and improved in its load driving capabilities on signals of both polarities by replacing the final source follower with a feedback output stage. The circuit was tested and proven to operate successfully.

In testing 10 samples of this circuit, it was demonstrated that the Idss current reference obtained from the PJFETs whith gate and source connected together has a good degree of reproducibility, about 8% maximum spread for circuits belonging to the same wafer.
Risetime measurements on the CSA have shown that the circuit has a unity-gain angular frequency of about 2.2 Grad/s with the input device (W=50mm) operating at 2.7mA.
Noise measurements carried out on this preamplifier with increased current in the input device have shown that at room temperature, the total white noise refered to the input is consistent with a noise resistance of about 25 Ohm.
Whith 500pF external capacitance and unipolar shaping with 100ns peaking time, the ENC is below 6000e- rms.

Second, a preamplifier employing PJFET and NMOS was tested. In this circuit, the JFETs are employed in the input cascode and in the output stage. The MOSFETs are employed to realize the reference current source which stands in opposition to the input cascode and an internal voltage shift network. The later has the advantage of consistantly reducing the off-the-chip components. Besides, the MOS implemantation of the internal current source was demonstrated to increase the frequency of the dominant pole and therefore to reduce the closed-loop risetime. With an external capacitance of 500pF and 33pF feedback capacitance, the risetime was found to vary between 13ns and 16ns on 9 samples belonging to the same wafer.
The noise performances at room temperature were found to be comparable with those of the previous circuits, which means that the MOS internal current source does not significantly increase the noise.
The PJFET-NMOS preamplifier was tested at liquid nitrogen temperature. The circuit remains perfectly functional and its noise performances undergo a substantial improvement in passing from room to cryogenic temperature. With 500pF detector capacitance, unipolar shaping of 100ns peaking time ENC was measured to be about 3500 e- rms.

As a conclusion, PJFET and PJFET-NMOS low noise preamplifiers realized in DMILL technology were proven to behave according to the simulation and to feature very good noise performances.

b/ BiCMOS transimpedance preamplifiers.

b.1. Fast BiCMOS Front-end for Silicon Strip Detectors (design & tests W. Dabrovsky, University of Krakow, Poland, in collaboration with CERN/ECP division)

A series of protoype front-end circuits for silicon strip detectors has been designed and manufactured using the DMILL technology. The primary goal of this work was to study the performance of this technology with respect to the front-end electronics for long silicon strips, as proposed for the ATLAS semiconductor tracker. It is well known that for large detector capacitances and short shaping times the bipolar devices offer a superior noise vs power figure of merit. They are two critical issues concerning bipolar transistors which determine their low-noise and radiation hardness performances, i.e. the base spread resistance and the degradation of current gain factor ß caused by radiation.

As a basic front-end circuit, a transresistance amplifier based on a bipolar input transistor is chosen. The preamplifier is followed by a simple integrator which is based on a differential amplifier and is ac coupled to the preamplifier. This way, a very good robustness of the circuit against the variations of device parameters and bias voltages has been obtained.

The preliminary measurements performed on the magnufactured structures showed a quite good consistency of the basic circuit parameters with the designed values. The gain of 30mV/fC and the peaking time of about 25ns at the total power dissipation below 1mW has been obtained. The results of noise measurements are shown in Fig DA1. The noise vs input capacitance was measured

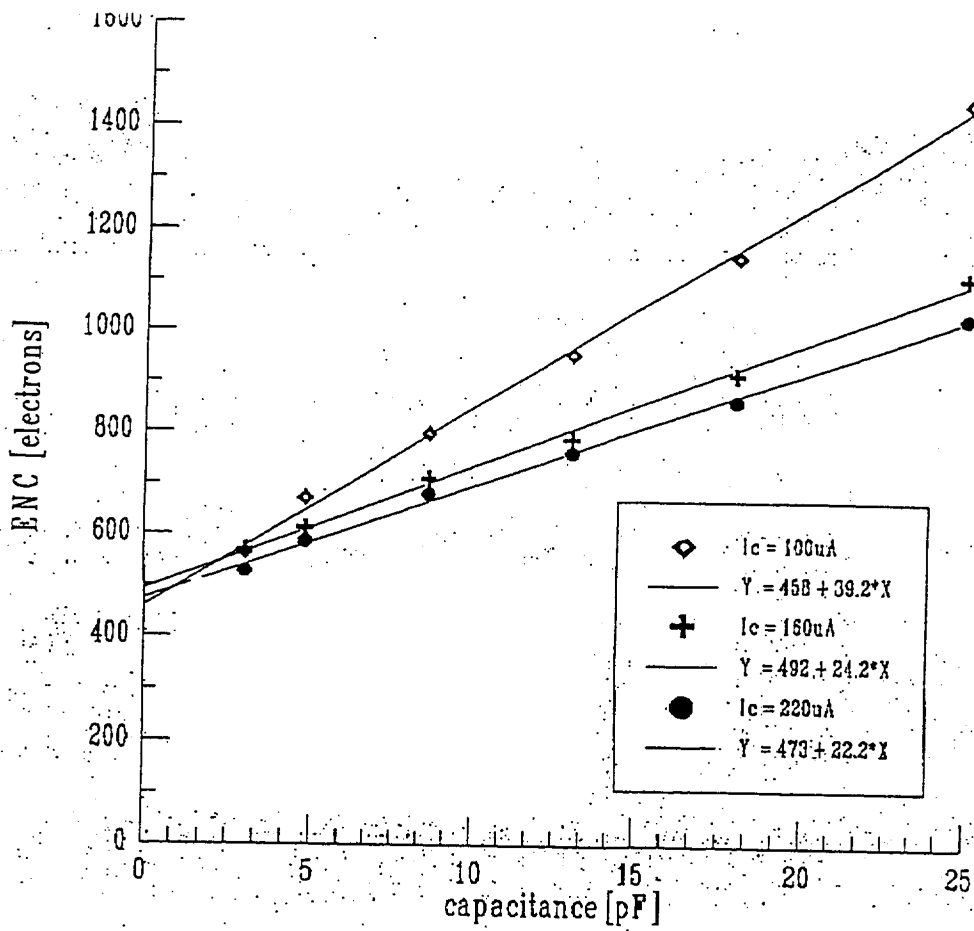


Fig. DA1

Req [Ohm]

1/Ic [1/mA]

NPN_16: 16 x 1.2um x 1.2um
Req = 20.7/Ic + 54
NPN_10: 10um x 1.2um
Req = 21.4/Ic + 202
NPN_4: 4.8um x 1.2um
Req = 20.0/Ic + 402
NPN_2: 2.4um x 1.2um
Req = 19.4/Ic + 668
NPN_1: 1.2um x 1.2um
Req = 21.0/Ic + 888

Fig. DA2

for three different values of the collector current in the input transistor: 100μA, 160μA and 220μA. The emitter area of the input transistor was 1.2*20 μm^2. It should be noticed that the above mentioned collector currents are evaluated with the precision of +/-20% only, since more other circuits are connected to the same bias lines. The noise parametrizations obtained from these measurements are respectively:

ENC=458 e- + 39 e-/pF (IC=100 μA)

ENC=492 e- + 24 e-/pF (IC=160 μA)

ENC=473 e- + 22 e-/pF (IC=220 μA)

The above results show that bipolar transistors available in the DMILL technology are fully suitable for low-noise front-end electronics required for ATLAS semiconductor tracker.

Together with the prototype circuits, a series of individual bipolar transistors of different layouts has been manufactured. These devices are supposed to be used for the noise parametrization and radiation hardness study. From the point of view of noise performance, the very important parameter, which scales with the emitter area, is the base spread resistance rb. On the other side, this parameter can be evaluated properly only from noise measurements. Using a very simple parametrization, the equivalent input voltage noise of a bipolar transistor can be expressed by equivalent noise resistance Req as:

$$Req = rb + 0.5/gm$$

where gm is the transconductance proportionnal to the collector current. Thus, plotting Req as a function of 1/Ic one can evaluate the term rb. The results obtained for a series of devices are shown in Fig DA2. The values of equivalent noise resistance were evaluated from the noise spectra measured over a wide range of frequency. One can make two immediate observations, namely: (1) the rb scales with the emitter area, and (2) a significant edge effect is visible on rb.

b.2. BiCMOS transimpedance preamplifier (design & tests Saclay)

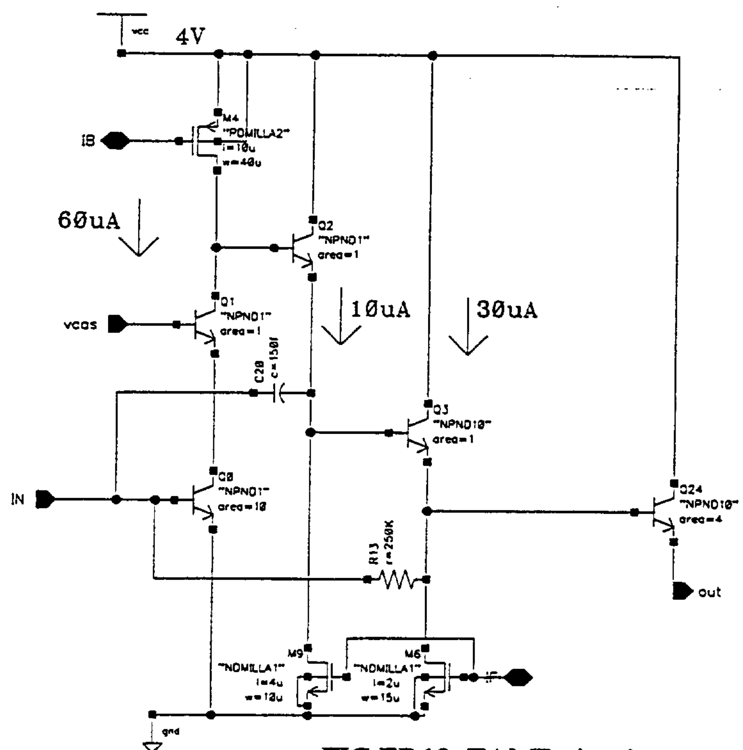


FIG ED13: TAMP circuit

The transimpedance preamplifier of fig ED13 has been implemented on FERMION reticle. It was designed to match low detector capacitances (<20pF). Its power consumption is 400μW.

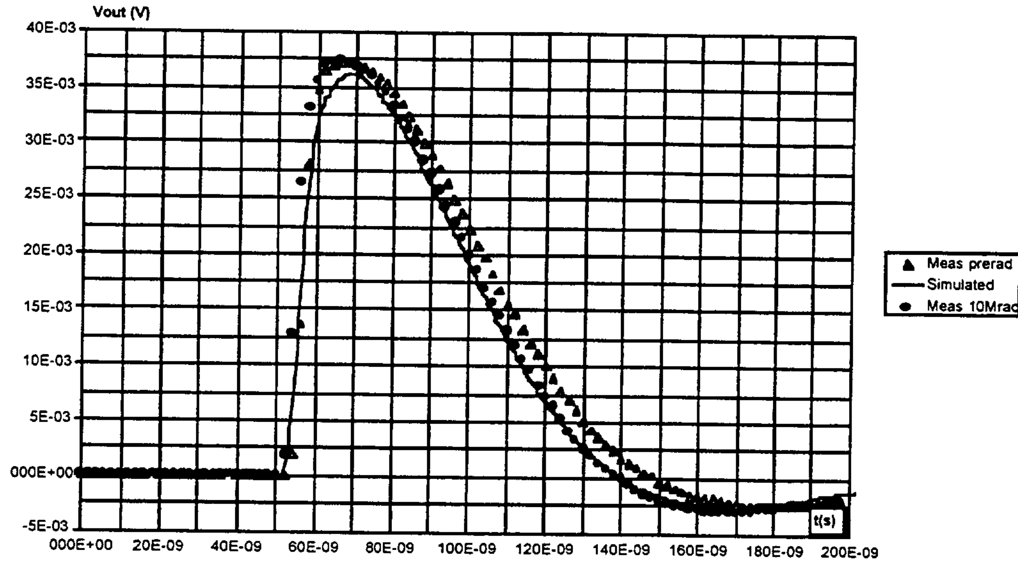


FIG ED14 : TAMP impulse response before and after irradiation

The bias current of the input device is 60µA. The area (12*1.2) of this device results from a trade-off between the collector current density which must be high enough in order to keep a reasonable current gain ß after gamma or neutron irradiation to minimize parallel noise and the value of the Rbb' resistor to minimize the serie noise.

The feedback resistor was designed to be 80KOhm. Due to a temporary problem observed on Fermion and Hadron reticles and explained in chapter 3, its real value is 250 KOhm. This is the reason of the slow fall time of the amplifier impulse response (FIG ED14). The measured transfer function is 1.01µV/e-. The peaking time of the amplifier is 18ns for a total input capacitance of 14pF. This impulse response is quite unsensitive to gamma irradiation, because of the radiation hardness of the npn bipolar transistor (the transconductance remains stable under irradiation) and of the good radiation hardness of resistors and capacitors.

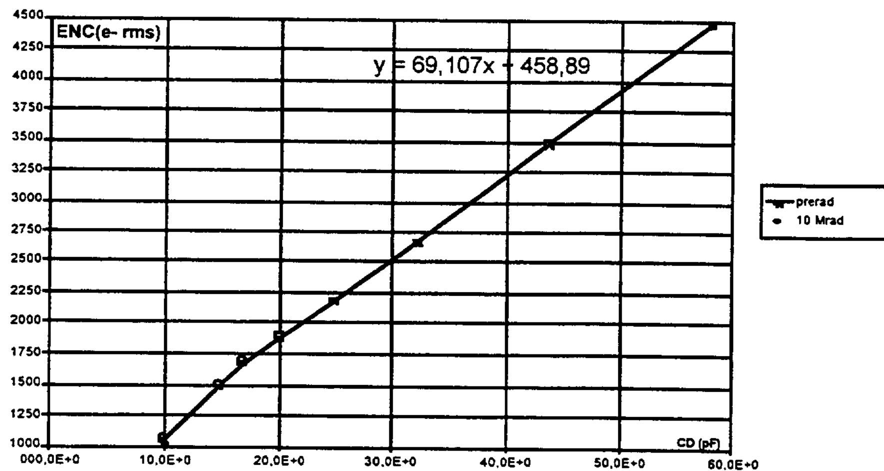


FIG ED15: TAMP ENC(CD) before and after gamma irradiation

The ENC(CD) plot presented in fig ED15 shows that the total noise is dominated by serie noise. This characteristic remains almost unchanged after 10 Mrad(SiO2). This result can be explained by the intrinsic stability of the serie noise under gamma irradiation for the npn input device:

$$e_n^2 = 2kT/gm + 4kT\,Rbb'$$

where gm=Ic/Ut is the transconductance of the input npn, and Rbb' its base resistance;

and by the good stability of the current gain ß under gamma irradiation for the npn input transistor, which lead to a stable parallel noise (determinated by the input current noise density):

$i_n^2 = 2\,q\,Ic/\beta$ remains negligible compared to 1000e- after gamma irradiation.

From the shape of the impulse response, we have computed the serie noise integral, then evaluated the equivalent serie resistance which is Rs=471 Ohm. The contribution of the collector shot noise is 216 Ohm, so the base resistance is 255 Ohm. In the next reticle, this design will be improved by increasing the area of the input transistor in order to decrease the base resistor.

Preliminary results on this circuit point out the interest of a bipolar input transistor for low noise preamplifiers:

- The bipolar transistor has a high transconductance for a small input capacitance (2.4 mA/V for Cin=220fF), and a small area (less than 200μm^2). For the equivalent transconductance at the same current, a PMOS would have a capacitance more than 25 higher. Therefore, bipolar allows low power consumption designs.
- The transconductance of the bipolar is unsensitive to irradiation.

- Its voltage noise density is determined by:
  $e_n^2 = 4kT\ (\mathbf{0.5}{*}gm + Rbb')$
  instead of
  $e_n^2 = 4kT\ \gamma\ gm$ with $\gamma > 2/3$ for MOS transistors, γ increasing with gamma irradiation.
- Its 1/f noise is very low.
- The principal drawback of NPN is its IB current which must be supplied and which is a source of parallel noise. This drawback may be minor if ß is large and stable enough under irradiation, as in the case of the DMILL technology.

The behavior of this transimpedance preamplifier under neutron irradiation is currently under study.

c/ <u>CMOS and BiCMOS comparators (design & tests Saclay).</u>

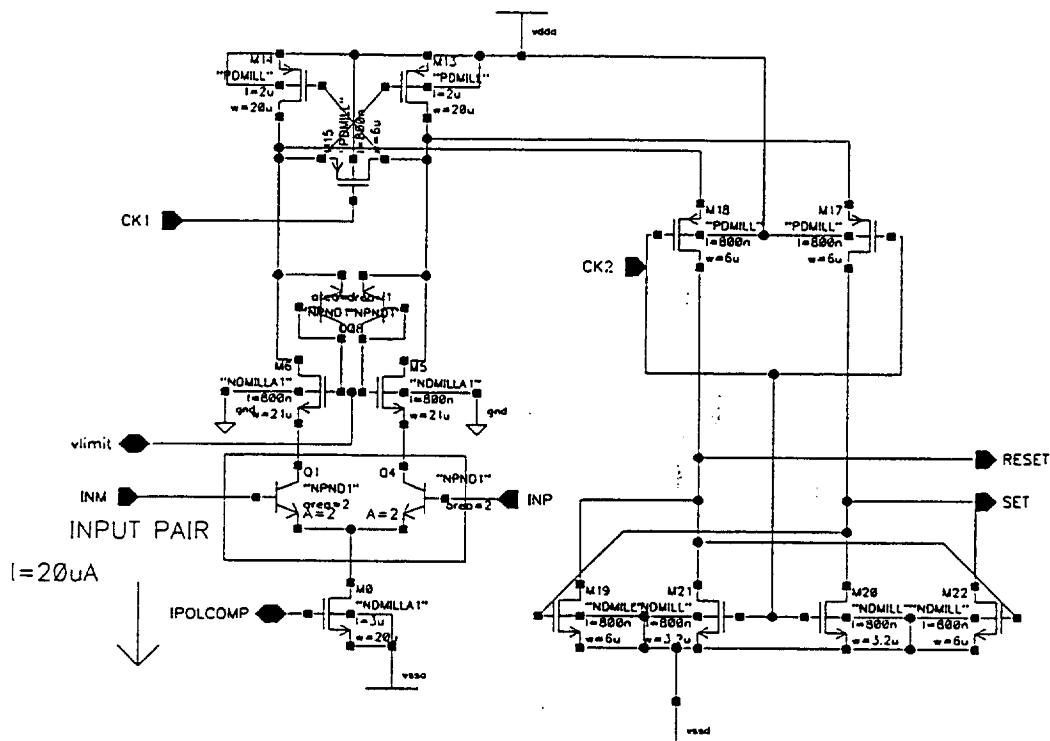


Fig ED16: BiCMOS comparator structure

The comparator presented in fig ED16 has been implemented with three types of input devices: PMOS, NMOS and NPN bipolar transistors. FIG ED17 shows the dynamic response of the BiCMOS comparator for an input signal of +/- 0.5mV

For an operation frequency of 40 MHz, preliminary measurements on 10 samples show that :
- for MOS input, the offset voltage is less than 10mV peak-peak, the noise is 3mV peak-peak.
- for BJT input, the offset voltage is less than 2mV peak-peak., the noise is less than 1mV peak-peak.

This good behaviour of BJT input comparator can be explained by the better matching of NPN device and by their higher transconductance which minimize the effects of mismatchs in loads.

The behaviour of these circuits under gamma and neutron irradiation is currently under study.

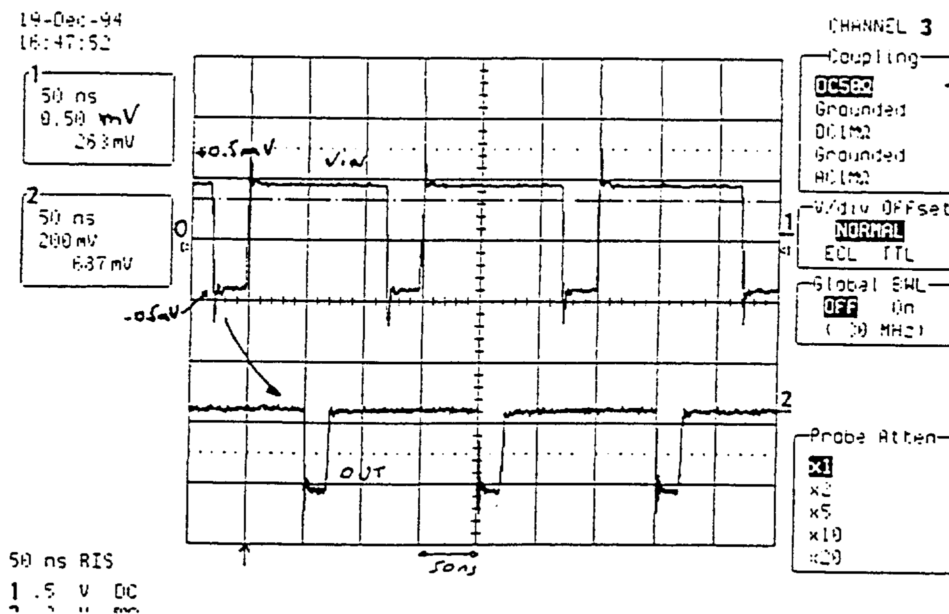
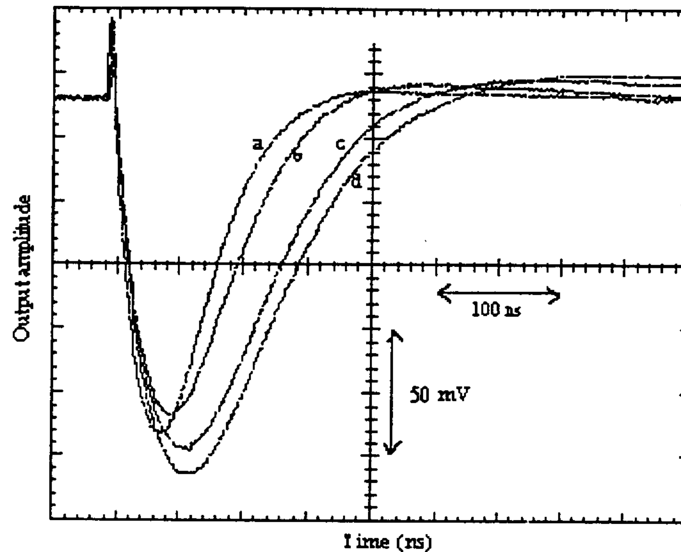


FIG ED17: dynamic response of the BiCMOS comparator for an input signal of +/- 0.5mV (F=6.6MHz, Fclock=40MHz). (The delay between the signal and the output is due to cables)

d/ Electronics designed for pixel detector (design & tests CPPM-Marseille)

d.1. Results from circuits implemented in the BOSON reticle

As described in the previous status report, a charge sensitive amplifier has been implemented in the boson reticle. This amplifier includes all the available transistors of the DMILL technology. It has been irradiated up to 3.6 10^{14} protons (300 MeV)/cm^2 (18 Mrad(SiO_2)) at the Saturne synchrotron facility (LNS) at Saclay, France. Fig. LB2. shows the response of this amplifier at different ionizing doses. The rise time, which is one of the most important parameters for the pixel detector, increases only by a few percent. This indicates that the amplifier behaves successfully even after a dose as high as 18 Mrad(SiO_2). It is, therefore, a good candidate for the pixel detector. Further details can be found in [ref LB1].



a: before irradiation
b: 150 krad(Si) / 3 10^{12} protons(300 MeV)/cm^2
c: 9 Mrad(Si) / 1.8 10^{14} protons(300 MeV)/cm^2
d: 18 Mrad(Si) / 3.6 10^{14} protons(300 MeV)/cm^2

Fig. LB2. Current impulse responses.

d.2. Preliminary results from circuits implemented in the Fermion reticle

i/ Charge sensitive amplifier

An enhanced charge sensitive amplifier has been developped and designed to reduce the power consumption and to increase the gain. Measurements performed on this amplifier give a typical power consumption of 20 µW.
The measured noise is around 90 electrons.
Unfortunately, this design of this amplifier looks to be sensitive to the threshold voltage mismatch and consequently is sensitive to the power supply. The reason seems to be the body effect. The previous version of the amplifier, which has also been implemented, is totally unsensitive to the power supply. It offers the same features except for the gain which is twice lower than the first one.

ii/ A complete analog pixel cell (amplifier + discriminator): DMILLPIX1

This cell includes the previous charge amplifier and a very low offset discriminator. AC coupling between the first stage and the discriminator allows the comparator to be unsensitive to the DC level variation of the input amplifier. Furthermore, this improves the signal to noise ratio.
The silicon area is 50 um x 240 um.
All measurements are performed with a power consumption close to 50 µW.
Fig. LB3. shows the amplitude efficiency of the cell with a threshold current of 15 nA. This curve gives a noise around 80 electrons, which is consistent with the noise found in section e.2.i/.

Considering 50 % efficiency, the amplitude threshold is here 950 electrons for an input threshold current of 15 nA. Fig. LB4. depicts the delay of the output for different input charges.The delay has been normalized with the response of the charge deposited by a MIP in 300 µm of silicon (the cell is in tune with the previous set-up). This is mainly due to how the discriminator is overdrived.

Unfortunately, as mentioned in section e.2. ii/, the cell is sensitive to the body effect. Since this effect is not uniform from chip to chip, threshold spread measurement is difficult to carry out.

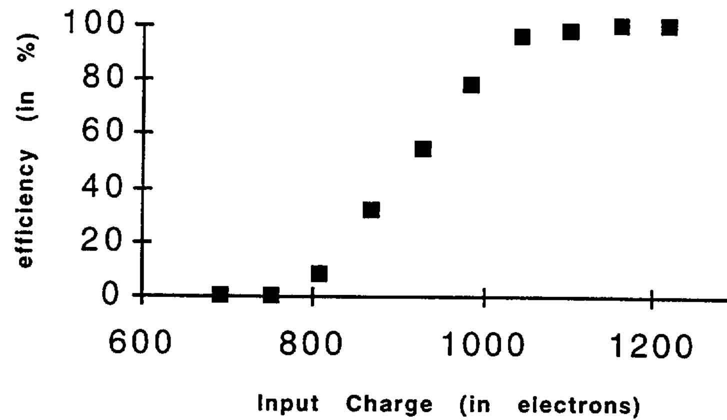


Fig. LB3. amplitude efficiency versus input charge

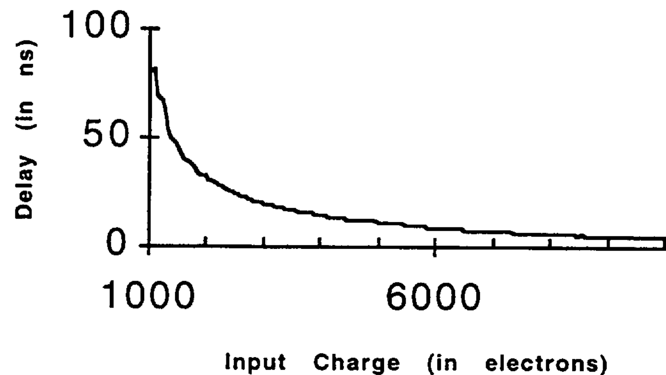


Fig. LB4. delay of the output of the cell versus input charge

iii/ DMILLPIX1 with the previous version of amplifier

DMILLPIX1 also has been inplemented with the previous amplifier version and a study on 12 cells gives the following results:

σ = 503 electrons for a mean threshold of 3070 electrons

σ = 533 electrons for a mean threshold of 6300 electrons

All measurements presented below are performed with DMILLPIX1 implemented with the previous version amplifier. Fig. LB5. shows the amplitude threshold (at 50 % efficiency) versus the input threshold current.
DMILLPIX1 has also been tested with different power consumptions. Considering that the minimum threshold is slightly increased, it works successfully at 38 μW.

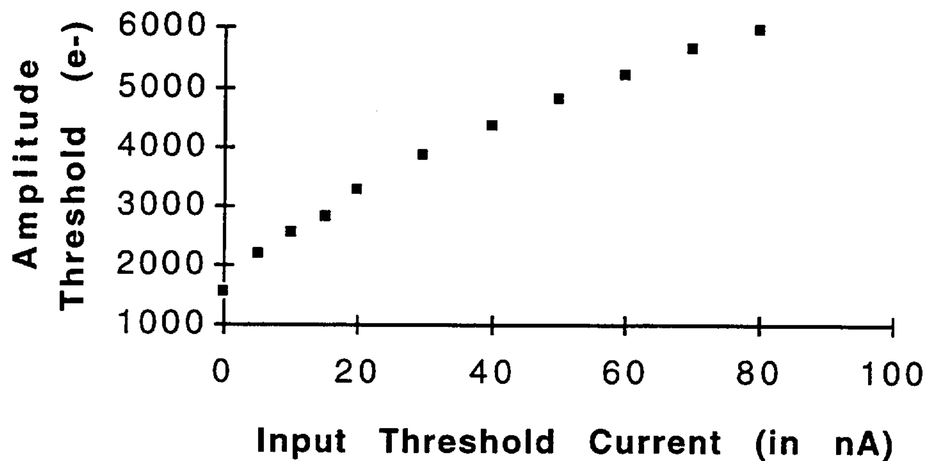


Fig. LB5. amplitude threshold of the cell versus threshold current

iv/ A second complete analog pixel cell: DMILLPIX2.

This cell has been developped to comply with power consumption and silicon area requirements.The silicon area is 50 um x 130 um. Until now, no qualitative measurements have been made but a rough test has demontrated that DMILLPIX2 works successfully with a power consumption of 30 uW.

v/ A prototype (32 * 8) pixel array.

It includes DMILLPIX1 and DMILLPIX2, 4 test-in and input transistors (bipolar structure) used for photo-injection. The middle part (16 * 8) is built to be bump-bonded on a silicon detector. The purpose is to investigate the cross-talk between the analog part and the detector and the coupling between 2 analog parts. Furthermore, we want to study threshold mismatch in putting the pixel cell in its real environment (detector, pad and neighbouring cells). To be totally independant of the digital part, a simple shift register based read-out system has been implemented. Trenches and shields ensure a complete isolation for this part and thus, prevent us from having any problem with logic signals.

vi/ Preliminary results from the circuit implemented in the HADRON reticle

This circuit is a 16 * 8 array with a complete ATLAS requirements read-out system. It includes about 20,000 transistors. The aim is to validate an ATLAS specific prototype. This array includes DMILLPIX1 and DMILLPIX2 and is built to be fully bump-bonded on a silicon detector. Several configurations are implemented to verify if shielding technique is required or not. The logic part outputs addresses of events which are in coincidence with the level 1 trigger. Fig. LB6. shows that the logic part buttering the column works successfully at 50 MHz.

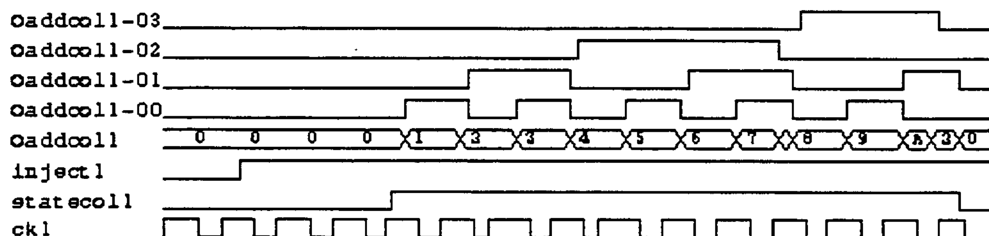


Fig. LB6. Data flow at the end of column (50 MHz)

5. ACCESS TO DMILL TECHNOLOGY

To enable the laboratories engaged in the construction of ATLAS or CMS to continue the development of prototype circuits in DMILL technology for these detectors, the Consortium has organized MPCs (Multi Project Chips) for these users since the end of 1993. Theses MPCs will be maintained to the end of the pre-industrial period.

Design kit

A design kit was furnished to DMILL users, containing:
- DMILL simulation parameters (Handbook)
- DMILL design rules (Handbook)
- 1 floppy disk containing a design rules verification file (see section 2.2), and several examples of designs of components.

MPCs organized in 1994

The first MPC organized for these users was that of the Hadron reticle. This MPC was proposed during the November 1993 MUG to the laboratories working on the development of ATLAS and CMS [14]. The circuit development projects proposed by the candidate laboratories for the use of DMILL were selected on the basis of recommendations of an advisory committee made up of experts working in the LHC environment and independent of the Consortium. Due to DMILL's pre-industrial status, no financial participation was requested of the laboratories using DMILL except for the costs of cutting and packaging their components. In conformity with requests of these users, the Hadron reticle processing was started at the end of June 1994 . This processing was completed 15 weeks later, 20 October. The systematic tests carried out on this batch showed abnormal electrical properties. An in-depth analysis showed that the origin of this problem was an error in the fabrication of two of the masks used in the processing. This fault was due to a malfunction of the quality control procedure used by the masks manufacturer. Following the full identification of the cause of this problem, Leti asked the manufacturer to correct the masks, and restarted the Hadron processing giving it absolute priority. The processing of this new Hadron batch was carried out in 6 weeks and was completed 15 December. After a week of systematic tests, three wafers of this batch were returned to Thomson-TCS for cutting, packaging and distribution in accordance with the users' orders. Preliminary Hadron results were given in section 4.

In parallel with the Hadron MPC for DMILL users not belonging to the Consortium, another MPC was organized for DMILL users belonging to the Consortium. This MPC called Fermion was completed mid-November 1994. Preliminary Fermion results were given in section 4.

The laboratories or collaborations using DMILL are listed in Table MD12. The main functions implemented in the Hadron and Fermion reticles are summarized in Table MD13. The planning for the processing of these MPCs and that for the 1995 and 1996 MPCs is shown in Figure MD14.

MPCs organized in 1995

In 1995, two new MPCs named Higgs and Lepton are organized for DMILL users. The reticles of these MPCs will be shared between members and non members of the DMILL Consortium. They will start 3 April and 15 May, respectively (dates for delivery of circuits designs in GDSII format), and will end, respectively 30 November (Higgs reticle, date for supplying packaged components to users) and 30 September (Lepton reticle, date for supplying packaged components to users). The Lepton reticle, which will be mainly dedicated to users not belonging to DMILL Consortium, will be processed at an accelerated rate (4.5 months). An application form has been sent to all the laboratories using the Hadron reticle in 1994 to ask them to reserve the DMILL silicon surface required for their work in the 1995 Higgs and Lepton reticles. The selection of candidates and the financial conditions for access to DMILL Higgs and Lepton reticles in 1995 are the same as those for 1994. Several Institutions involved in the study of LHC detectors have already reserved on DMILL 95' batches silicon surface for the development of demonstrator circuits including up to 16 or 32 channels, dedicated to ATLAS or CMS. These circuit developments are currently in progress.

MPCs organized in 1996

In 1996, two new MPCs will be organized to make it possible for laboratories to continue the optimization of their prototype circuits started using DMILL technology. The precise date for the processing of these MPCs will be fixed later so as to better meet the users requirements.

Access to DMILL in 1997

In 1997, DMILL will be available in industrial production site for mass production or MPC processing.

6. INDUSTRIALIZATION SCHEDULE

The general planning of development and industrialization of DMILL is given in figure MD15.

Stabilization within the development laboratory

As mentionned in section 2.5, from October 1993 to March 1995, 12 electrical batches have been processed by CEA-Leti to stabilize the DMILL technology. This stabilization is now close to completion.

Industrial transfer and qualification

The start of the industrial transfer is foreseen mid-1995; it will be completed mid-1996. Its main stages will be: transfer of technological modules of DMILL to the industrial production line; processing of numerous batches including technological test modules and analog and digital demonstration circuits; characterization of electrical and hardness performances on test modules and on demonstration circuits; adjustment of processing parameters if necessary; final stabilization of the process.

The industrial qualification of the process will be carried out in the second half of 1996.

Industrial availability

DMILL will be available at industrial site from 1997 onwards for production runs or for the processing of MPCs dedicated to the optimization of prototype circuits.

7. REQUESTS TO CERN

a/ Funding

As explained in chapter 5, the access to the Lepton and Higgs reticles (1995) for the Institutes involved in the development of ATLAS or CMS is free of charge. Many Instituts have already requested a silicon surface in these reticles. These Instituts will submit demonstrator circuits dedicated to ATLAS or CMS. These circuits, which are now for some of them close to final version, will include a large number of acquisition channels and thus will require a large silicon surface. The total surface of Higgs and Lepton reticles, which must be shared between users members of the Consortium and users non members of the consortium, will be very probabely not enough to satisfy all demands. The CEA-Leti has the technical capability to process additional reticles if required. However such reticles are not foreseen in our budget. Therefore, we are asking the LERB to contribute to the availability of DMILL for HEP oriented R&D by a financial help to RD29 collaboration. The amount asked to the LERB for this help is 140,000 CHF, corresponding to the

direct cost payed by the Leti for the set of masks necessary for one reticle.

b/ Beam test

In our proposal and in our previous status report, we have asked the autorization to put samples of circuits designed in DMILL technology in a pion or proton beam at CERN. A such beam is necessary to perform tests of SEU immunity of microelectronics technologies. However, up to now, for reasons of convenience, SEU tests on DMILL technology have been performed using a protons beam from the Saturne Synchrotron facility (LNS). It remains uncertainities on the avalibility of this facility in the future. Therefore, we ask again the CERN to allow us, if necessary, to put samples of 0.3 mm thick of silicon in a 10^9 $cm^{-2}s^{-1}$ beam of pions or protons with an energy between 200 MeV and 1.5 GeV.

8. CONCLUSIONS

DMILL Technology integrates monolithically rad-hard CMOS, PJFETs and NPN bipolar transistors, together with two families of rad-hard resistances and capacitances. These components have been chosen for their complementary properties which offer a large degree of flexibility in circuits design thus making it possible to meet the particularly severe requirements imposed for ATLAS or CMS readout electronics. The electrical and radiation hardness characteristics of DMILL components have been chosen to meet the hard LHC specifications [8,9,10,11].

Last improvements performed on DMILL components have lead to a very high radiation hardness level, Measurements performed on digital circuits (16 bits microprocessor) have demonstrate a radiation hardness higher than 350 Mrad. Measurements performed on both analog and digital LHC oriented circuits confirm the very good adaptation of DMILL to LHC requirements.

To make possible the development of prototype circuits dedicated to ATLAS or CMS by laboratories involved in LHC developments, a first MPC (Multi Project Chip) was organized in 1994 with DMILL technology. Two new MPCs have been organized in 1995 and two other MPCs will be organized in 1996 to allow these laboratories to carry out their works with DMILL up to its industrial availability.

The stabilization of the process in the development laboratory is now close to completion; the start of the industrial transfer of DMILL is foreseen mid-1995, it will be completed mid-1996 and will be followed by the industrial qualification, which will be completed at the end of 1996. DMILL will be available at industrial site for prototyping or production from 1997 onwards, in tune with the schedule of development of LHC detectors.

9. ACKNOWLEDGEMENTS

The DMILL collaboration wish to thank Dr. Wladek Dabrowski (University of Krakow, Poland) for its original study of low noise bipolar preamplifier using DMILL technology and for its contribution to this paper. The collaboration would like also to thank Dr. Francesco Manfredi (University of Pavia, Italy) for its study of low noise preamplifiers using DMILL PJFETs, and for usefull discussions about these devices. Particular thanks are also aimed to Dr. Pierre Jarron, Dr. Walter Snoeys and Franz Pengg (CERN, ECP division) for usefull discussions on the electrical simulation of DMILL components.

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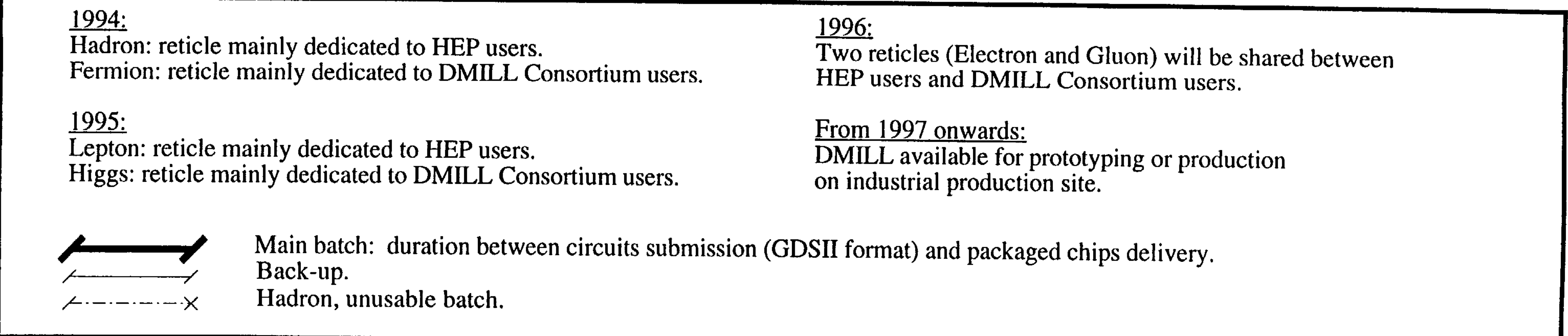
Institution	Country	R&D Collaboration	Application
CPPM (Marseille)	France	RD19	LHC
IPNL (Lyon)	France	RD18 + RD28	LHC
ISNG (Grenoble)	France	RD3	LHC
LAL (Orsay)	France	RD3 + DELPHI	LHC
LEPSI (Strasbourg)	France	RD20	LHC
CEA-DSM (Saclay)	France	RD3	LHC
CEA-DTA (Grenoble)	France	(CEA)	(CEA)
CEA-DAM (Bruyères-le-Châtel)	France	(CEA)	(CEA)
University of Pavie	Italy	RD3 + DELPHI	LHC
University of Lund	Sweden	RD6	LHC
University of Stockholm	Sweden	FERMI	LHC
University of Linköping	Sweden	FERMI	LHC
SICON A.B.	Sweden	FERMI	LHC
CERN	Switzerland	RD18 + RD19	LHC
Rutherford Appleton Laboratory	Great Britain	RD20	LHC
15 Institutions	5 Countries	10 Collaborations = 8 LHC projects + 2 CEA projects	

Table MD12: Laboratories or Collaborations using DMILL technology

Analog Memory with random access (pipeline), 128 cells, 40 MHz.
ADC 12 bits, 40 MHz; ADC 5 bits, 65 MHz.
Analog compressor by 30, range 0-2 volts, 50 MHz.
Charge amplifier + discriminator + readout for pixel detector (32x8 cells).
PLL time measurer.
16 bits microprocessor 29101 type.
Operational amplifiers.
Charge amplifiers.
Current amplifiers.
Latch.
Shaper 12 bits 25 ns.
Analog buffer.
Static and dynamic shift registers.
MOS-ECL and ECL-MOS converters.
PJFET logic gates.
Test transistors.
(...)

Table MD13: Main functionnalities implemented in DMILL Fermion and Hadron reticles.

	1994	1995	1996
	01 02 03 04 05 06 07 08 09 10 11 12	01 02 03 04 05 06 07 08 09 10 11 12	01 02 03 04 05 06 07 08 09 10 11 12
RETICLES MAINLY DEDICATED TO HEP USERS	HADRON, lost batch HADRON, lost Back-up HADRON (new batch) Back-up Hadron	HADRON (new batch) Back-up Hadron LEPTON Back-up Lepton	2 RETICLES SHARED BETWEEN HEP USERS AND DMILL CONSORTIUM USERS ARE SCHEDULED IN 1996
RETICLES MAINLY DEDICATED TO DMILL CONSORTIUM USERS	FERMION Back-up Fermion	HIGGS Back-up Higgs	

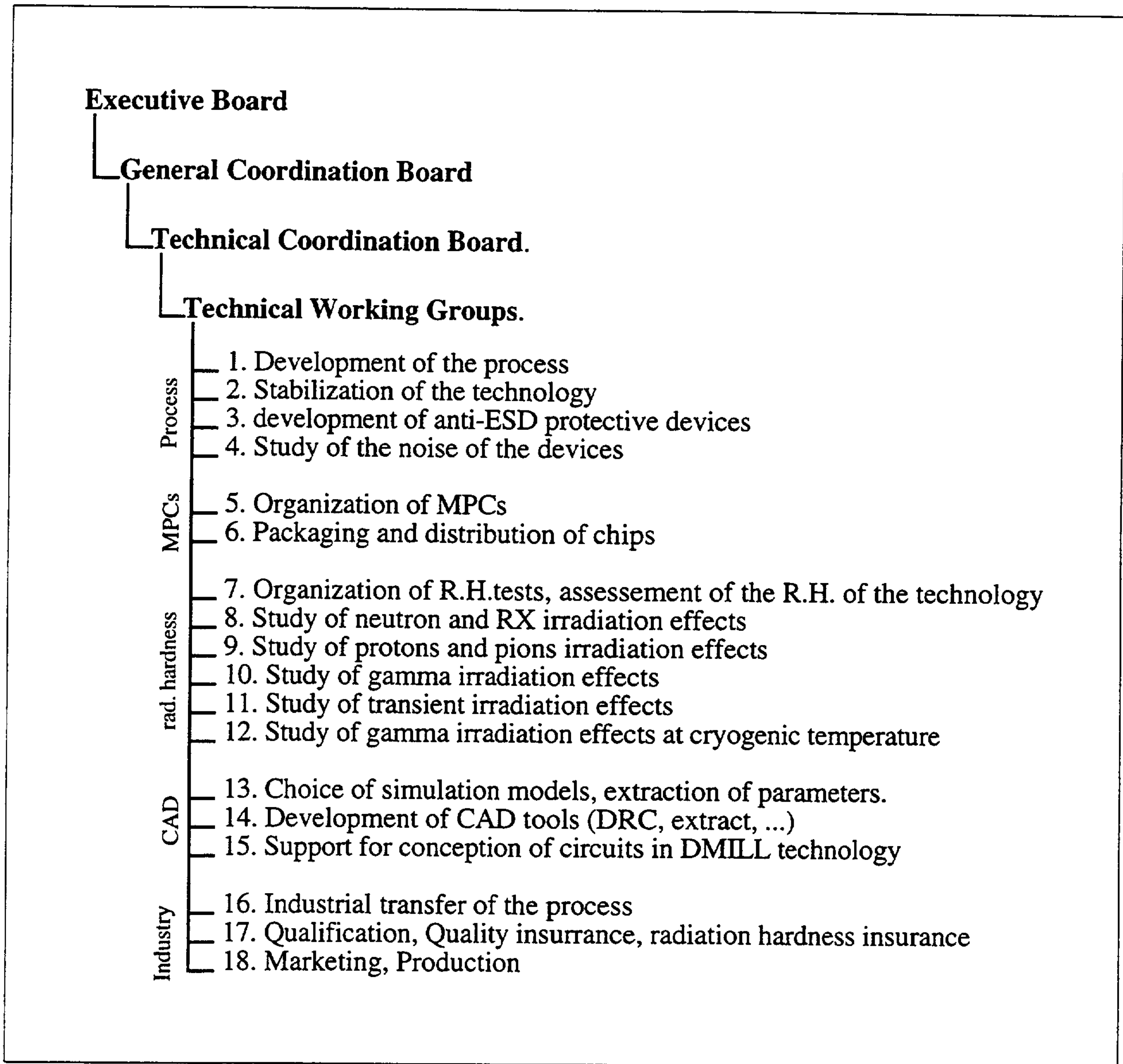


M.D./ CEN Saclay, DSM-DAPNIA-SEI, 03.03.95

Figure MD14: DMILL processes performed in 1994 and scheduled in 1995 and 1996.

YEAR	91	92	93	94	95	96	97	98	99	00	01	02	03
Assembling of the process													
In-lab process stabilisation													
In-lab process o MPCs for HEP users													
Industrial transfert													
Industrial stab. & qualif.													
Availability foı Industrial production													
Availability foı Industrial MPCs													

Fig. MD15: General schedule of development and industrialization of DMILL technology



Annexe 1: Organization of DMILL Consortium.