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Study of common-mode noise of the $SMA^2SH - 64A$ preamplifier array*

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ABSTRACT

Employing a 64-channel CMOS preamplifier array, $SMA^2SH-64A$, we studied its signal-to-noise ratio. Single-channel noise was substantially contaminated with a base-line shift, which was common for all neighboring channels. Subtracting the common base-line shift, we found that the noise level decreased to be acceptable in terms of the design parameters as well as for practical use.

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1. Introduction

In the KEK B-factory experiment, BELLE,[1] a silicon micro-strip detector[2] is going to be employed. In order to provide an appropriate readout circuit, a CMOS preamplifier array[3] is being developed. While checking out a single-channel version,[4] which included a complete chain of the analog-processing circuit, it has been found that the signal-to-noise ratio was much worse than the expected value, even including the min/max range of the design parameters or the process variation. Going back to a SPICE simulation, it was found that the output node of the preamplifier could easily be disturbed by a ripple coming from a power-rail. If this speculation meets the real condition, the disturbance, i.e. an event-by-event base-line shift, should be common for all signal channels, which could be compensated for by appropriate data processing.[5] Since there was no way to extract the common mode for a single-channel chip, a 64-channel CMOS preamplifier array, $SMA^2SH-64A$,[6] was used in this study, which had an identical analog processing chain with the single-channel chip. The SMA^2SH-series preamplifier chips are characterized by an eight-stage built-in analog memory, and a quadruple-correlated noise-filtering capability. With these capabilities SMA^2SH-series preamplifiers could be triggered asynchronous to the operation cycle, and show a low-noise characteristic, even with a conventional switched capacitor-based circuit implementation.

This paper is to provide direct proof for the common-mode base-line shift, to which the excess noise is attributed. In order to cover the subject the description is organized as follows: section 2 deals with points concerning the hardware relevant to the operation of $SMA^2SH-64A$; section 3 provides a data-reduction procedure and discussions concerning the measured electronic noise; and section 4 concludes the discussion.

2. Instruments to measure the electronic noise

2.1. Setup for the noise measurement

Figure 1 shows the setup for measuring the noise in this study. The setup comprises four blocks: a personal computer (PC-9801VX from NEC) with two flash A-to-D converter cards (AD-12H10H from Thamway Co., Ltd.); a test fixture with a packaged $SMA^2SH-64A$ chip; a pulse-timing generator block; a synchronous-trigger generator block; and a pulse generator (HP8131A from Hewlett Packard). Each block is described below separately.

2.2. Flash A-to-D converter

AOUT1 and AOUT2 delivered by the test fixture were fed into 12-bit FADC cards, which were plugged in a backplane of the personal computer. The major parameters of the FADC card are summarized in Table 1. Due to interplay between the input impedance of the A-to-D converter , i.e. 10 $k\Omega$, and the output impedance of AOUT1 and AOUT2, i.e. a few $k\Omega$, the output analogs were compressed by 25%. The typical output scale was 150 mV per 4 fC, i.e. 25000 e's, instead of a nominal value of 200 mV for a high-impedance load. The DC levels of AOUT1 and AOUT2 were located around 2.5 V, which were comfortably accepted by the flash A-to-D converters. The flash A-to-D converters were enabled by CS and analogs were sampled at the trailing edge of REQ, while analog outputs from $SMA^2SH-64A$ were driven at the leading edge of REQ. The readout frequency was 0.5 or 1 MHz per channel. Since the flash A-to-D converter had a pipe-lined organization for an internal signal processing, it took 6 REQ cycles before delivering encoded data at its output.

2.3. Test fixture

Figure 2 shows a schematic of the test fixture. In order to set an operation current of $SMA^2SH-64A$, a 36 $k\Omega$ resistor was applied for the IREF terminal to be connected to V_{SS} (Gnd). The operation current was monitored at the IMON terminal, which had a load resistor of 36 $k\Omega$ connected to V_{DD} (5.0 V).

The test fixture accepted five TTL signals (RESET, CS, REQ, CK and CKB), which were generated at the pulse-timing generator block. Details are described in a later section.

There were five digital outputs (ACKB, CSOUT, HA[2], HA[1], and HA[0]), which were not utilized for the test fixture. ACKB indicates that $SMA^2SH-64A$ is responding with valid data. CSOUT asserts to indicate that there exists no more data for further REQ's, which facilitates to readout several SMA^2SH chips cascaded together. CSOUT continues to assert until CS is negated by RESET. HA[2:0] indicates a stop location of the eight-stage analog memory, which could be employed to compensate for DC offsets associated with the analog memories.

There were five signals related to the test-pulse capability: VTP1, VTP2, TPENB, TPSEL[1], and TPSEL[0]. VTP1 and VTP1 were DC voltages located around 2.5 V, which were applied by external DC sources. The amount of test-pulse charge was defined as

$$(VTP1-VTP2)*(0.2\ pF)\ \ [Coulomb]. \tag{2.1}$$

When TPENB is set as true, an internal test-pulse generator of $SMA^2SH-64A$ was activated at the timing when the 8-th analog memory was selected to record an analog for the first time after an initialization procedure following RESET. TPSEL[1:0] facilitated to select pulsed channels for each fourth channel, which were set by on-board switches. The test pulse was eventually fed into 16 channels out of 64 channels of $SMA^2SH-64A$.

SUB[1] and SUB[0] were to set a distance in time-domain between the "before" and "after" samples, which were set by on-board switches. The test fixture was operated with SUB=1 during this work. This point is considered again in a later description related to the pulse-height deficit. The analog outputs from $SMA^2SH-64A$ were multiplexed in series to be delivered at the terminals AOUT1 and AOUT2.

As for the 8 consecutive analog inputs out of 64 channels, we applied capacitors externally in order to emulate the detector capacitances.

2.4. Pulse-timing generator

The entire system was driven by a 2 MHz and 50%-duty clock pulse from HP8131A. We also tried an 1 MHz operation in this study. The pulse-timing generator block delivered control pulses in sequence. Figure 3 shows an exact circuit schematic of the pulse-timing generator block. When SELECT turns true, CS asserts to be high at the leading edge of CK2M, and continues to assert until SELECT negates itself. While CS is high, REQ toggles with a half frequency of CK2M. When SELECT turns false, RESET is delivered during an one-clock period of CK2M. CK and CKB have same frequency with CK2M and are complementary for each other.

2.5. Synchronous-trigger generator

In order to avoid one-clock jitter between the RESET and CS timing, we prepared a synchronous-trigger generator block. Figure 4 shows an exact circuit schematic of the synchronous-trigger generator block. This block employs an 8-bit counter, which comprises two 74LS169's, and an 8-bit comparator, which comprises two 74LS85's. When the counter reaches a preset value selected by an 8-bit on-board switch, i.e. D[7:0], the A=B output of the 8-bit comparator sets a D-flip-flop. The D-flip-flop is reset by a ripple carry-over of the 8-bit counter. Eventually, the output of the D-flip-flop (SELECT) is completely synchronized with the timing of

CK2M. In practice,1 the synchronous-trigger generator block is operated with a complementary signal of CK2M, i.e. CK2MB, to avoid any timing hazard at the pulse-timing generator block.

3. Extraction of intrinsic electronic noise

3.1. Common-mode subtraction

We assume that the measured analog output for the $i-th$ event at the $j-th$ channel can be written as

$$A_{i,j} = e_{i,j} + p_{i,j} + c_i + a_{i,j}, \tag{3.1}$$

where $e_{i,j}$ is the electronic noise, $p_{i,j}$ the pedestal, c_i the common-mode noise, and $a_{i,j}$ the real signal. Since c_i is common for all signal channels by definition, it has no dependence on j. In order to discuss the noise problem we can take $a_{i,j} = 0$ without loosing any generality. Taking an average of $A_{i,j}$ over events we obtain

$$< A_{i,j} >_i = < e_{i,j} >_i + < p_{i,j} >_i + < c_i >_i, \tag{3.2}$$

where the first and third terms should tend to zero when the number of events is sufficiently large. The second term provides a finite value (P_j), which is indexed by j. We try to take a mean-square of $A_{i,j} - P_j$ over an ensemble for many events as

$$\begin{aligned} < (A_{i,j} - P_j)^2 >_i = & < e_{i,j}^2 >_i + < p_{i,j}^2 >_i + < c_i^2 >_i \\ & + 2 < e_{i,j} c_i > + 2 < e_{i,j} p_{i,j} >_i + 2 < c_i p_{i,j} >_i - P_j^2 \end{aligned}, \tag{3.3}$$

where we find two things: one is an excess due to a common-mode noise (c_i); the other comes from an event-by-event pedestal fluctuation ($p_{i,j}$). If the pedestal is

stable for each channel, i.e. has no event-by-event effect, and hence no dependence on i, the above equation tends to

$$< (A_{i,j} - P_j)^2 >_i = < c_{i,j}^2 >_i + < c_i^2 >_i + 2 < e_{i,j} c_i >, \tag{3.4}$$

where c_i only is the source of the excess noise. As a next step we take the average of $A_{i,j}$ over the channels, which yields

$$< A_{i,j} >_j = < c_{i,j} >_j + < p_{i,j} >_j + c_i. \tag{3.5}$$

The first term should tend to zero again when the number of channels employed for the average is sufficiently large. The second term provides a finite value (Q_i) which is indexed by i. We define the event-by-event pedestal as

$$Q_i + c_i. \tag{3.6}$$

The pedestal-corrected amplitude ($\tilde{A}_{i,j}$) is defined as

$$\tilde{A}_{i,j} = c_{i,j} + p_{i,j} - Q_i. \tag{3.7}$$

Taking the average over an infinite number of events on $\tilde{A}_{i,j}$, we obtain

$$< \tilde{A}_{i,j} >_i = P_j - < Q_i >_i, \tag{3.8}$$

which is not necessarily zero as long as event-by-event pedestal shifts exist. An origin of the event-by-event pedestal comes from a jitter of the trigger timing. For each time of the trigger the analog memories assigned for the readout are generally random, which have some offset for each other, e.g. $\pm 20mV$. In order to evaluate the intrinsic electronic noise, we should take precaution to prevent any timing jitter during a measurement. The instrument described in the previous section has a mechanism to maintain the synchronization of the entire system. Any external noise induces some non-uniform pick-up over neighboring channels, and, hence, contributes to a non-zero $< \tilde{A}_{i,j} >_i$, in which condition c_i must be redefined as $c_{i,j}$.

3.2. Decrease in the pulse height for a larger input capacitance

Figure 5 shows the behavior of the pulse height versus the input capacitance. Due to an interplay between the preamplifier's feed-back characteristics and the input capacitance, the signal's rise time of the preamplifier is degraded for larger input capacitances. The amount of pulse-height loss is generally called the pulse-height deficit. In terms of a quadruple-correlated sampling, the pulse height relative to the zero input capacitance could be approximated as

$$\eta = \frac{1 - \{exp(-m\tau/t_0) + exp(-(m-1)\tau/t_0)\}/2}{1 - \{exp(-m\tau/t_c) + exp(-(m-1)\tau/t_c)\}/2}, \tag{3.9}$$

where τ is the sampling interval, t_0 the intrinsic rise time of the amplifier chain, t_c the rise time under the influence of the input capacitance, and $m\tau$ defines the peaking time for the effective pulse shape. The numerator and denominator come from the normalization constant appearing in Eq (A.4) of ref. 4 for amplifier rise times of t_0 and t_c, respectively. In practice we chose to set $\tau = 500\ ns$, $t_0 = 250\ ns$, and $m = 4 - SUB = 3$. The experimental data for the pulse height variation on the input capacitance provided

$$t_c = t_0 + (5.9 \pm 0.9\ k\Omega) * C_D + (0.011 \pm 0.021\ k\Omega/pF) * C_D^2 \quad [ns] \tag{3.10}$$

with 1% accuracy for the vertical scale of η, where C_D is the input capacitance for the preamplifier (measured in pF). From a circuit analysis we obtained the output impedance of the preamplifier as

$$Z_{out} = \frac{C_D + C_F}{C_F g_m} \quad [\Omega], \tag{3.11}$$

where C_F is the feed-back capacitance of the preamplifier, i.e. 0.2 pF, and g_m is the transconductance of the input FET, i.e. 2.5 mS nominally. Z_{out} couples to the input capacitance (C_L) of the gain stage located next to the preamplifier, which is

2 pF. Eventually, the time constant is described as

$$Z_{out} * C_L = \frac{C_L(C_D + C_F)}{C_F g_m} \rightarrow (4.0^{+1.0}_{-0.7}\ k\Omega) * C_D \quad [ns], \tag{3.12}$$

where C_D is measured in pF. The coefficient for C_D is reasonably consistent with the linear term in Eq (3.10). The range of error comes from an expected min/max values for g_m quoted from ref. 4. The second term in Eq (3.10) as well as a better agreement for the first term could be completely explained by an exact SPICE simulation.

3.3. Input capacitance

In order to set the values for the input capacitance of the preamplifier, we employed a C-V meter (Model 590 from Keithley). The capacitance measured at the external terminal located at the test fixture was 12 pF, which includes the stray capacitance on the chip together with the gate capacitance of the input nMOS FET, the package capacitance including the bonding wire, and the capacitance for the copper trace on the printed-circuit board. The capacitances for each section were identified to be 3 pF, 3 pF, and 6 pF, respectively. In order to evaluated the higher capacitance region, we applied additional lumped elements for 8 consecutive channels of the preamplifier array, over which the common-mode noise was defined.

3.4. Electronic noise

The electronic noise charge is defined as

$$enc = \frac{v_{rms}}{(150\ mV) * \eta} * 25000 \quad [electrons], \tag{3.13}$$

where η is the pulse height relative to the zero-input capacitance, as defined in Eq (3.9); v_{rms} is the rms voltage for $AOUT1 - AOUT2$; and 150 mV is a nominal pulse height for 25000 electrons of the input charge. Figure 6 shows the electronic

noise measured in this study together with the old data quoted from ref. 4. Since the electronic noise for 1 MHz and 2 MHz operation behaved in a similar manner, except for capacitances larger than 40 pF, we regarded that the effect of the shot noise inherent for the amplifier itself was very small. The discrepancy between the two at the higher capacitance end could be interpreted in terms of the effect of η, i.e. the pulse-height deficit. Assuming a measurement error of $\pm$50 e's for each data point, we obtained a noise slope of 19.2$\pm$2.5 e's/pF and 21.5$\pm$2.5 e's for 1 MHz and 2 MHz operations, respectively, while the older data without the common-mode subtraction was fit with 39.2$\pm$1.8 e's/pF. We recognize here that the older data were contaminated with external noise, to which we attributed the common-mode base-line shift. We mention here the design values for the noise slope were 27.8, 20.7, and 16.8 e's/pF for the worst, typical, and best parameter sets, respectively, which were extracted from Figure 4 (a) in ref. 4. It was clearly shown that the intrinsic electronic noise of the SMA^2SH-series preamplifiers was consistent with the design parameters.

There could be noise contributions from digitization noise and incomplete extraction of the common-mode base-line. The first one comes from the finite digit of the A-to-D conversion, which amounts to $203/\sqrt{12}$ electrons. The inaccuracy of the common-mode extraction is about $1/\sqrt{8}$ of the rms noise for each channel. For example, it is 354 electrons even for an rms noise of 1000 electrons for each channel. Eventually, the digitization noise and the effect of the incomplete extraction of the base-line could still be regarded as minor.

4. Summary

We have provided direct proof that the excess noise observed for a single-channel chip could be identified as a common-mode base-line shift. After subtracting the common-mode noise on an event-by-event basis, the noise slope was improved to be about 20 e's/pF, which was consistent with the expectation from the design parameters. We had attributed the origin of the common-mode noise to the interplay between the biasing circuit and the power-rail disturbance. Since the actual chip for the B-factory experiment, i.e. $SMA^2SH - 128$, should include a sparse readout, we have no way to compensate for the common-mode noise if it may exist. Instead of an off-line compensation we need an essential way to eliminate the common-mode noise completely. An assessment to suppress the common-mode noise has been examined, which will be submitted for fabrication in practice.

ACKNOWLEDGEMENTS

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TABLE CAPTIONS

1: Parameters of the FADC card

Table 1. Parameters of the FADC card

Input interface	single-ended
Input impedance	10 $k\Omega$
Input range	0 to 5 V
Frequency band-width	DC to 5 MHz (-3 dB)
Full scale count	4095
Integral non-linearity	$\pm$ 2.5 LSB
Differential non-linearity	$\pm$ 0.5 LSB
Sampling frequency	100 Msps (max)

FIGURE CAPTIONS

1) Setup for the noise measurement

2) Schematic of the test fixture

3) Schematic of the pulse-timing generator block

4) Schematic of the synchronous trigger generator block

5) Decrease in the pulse height versus the input capacitance
   The solid line is a fit to the data points with a second-order polynomial.

6) Electronic noise measured in terms of input capacitance
   The open circles (2 MHz) and squares (1 MHz) employ common-mode subtraction. The asterisks are the old data for the single-channel amplifier chip.

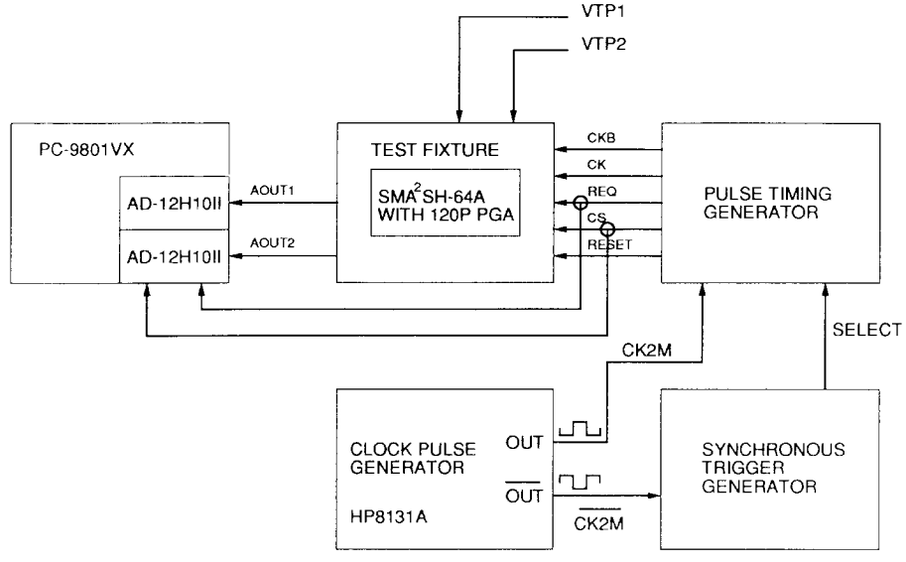


Fig. 1

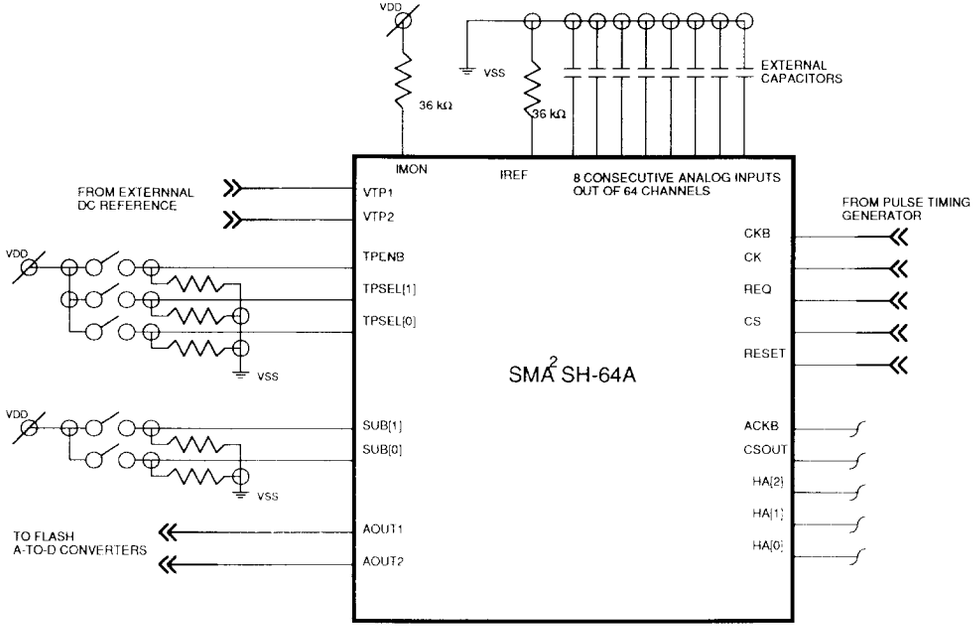
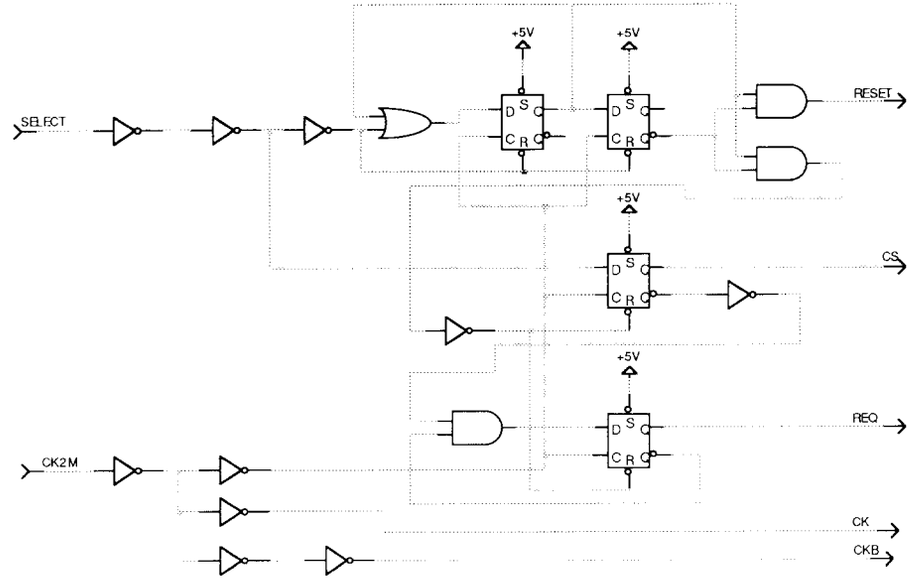

VDD
VSS
36 kΩ
36 kΩ
EXTERNAL CAPACITORS
IMON
IREF
8 CONSECUTIVE ANALOG INPUTS OUT OF 64 CHANNELS
FROM EXTERNNAL DC REFERENCE
VTP1
VTP2
TPENB
TPSEL[1]
TPSEL[0]
SUB[1]
SUB[0]
AOUT1
AOUT2
TO FLASH A-TO-D CONVERTERS
FROM PULSE TIMING GENERATOR
CKB
CK
REQ
CS
RESET
ACKB
CSOUT
HA[2]
HA[1]
HA[0]
SMA2 SH-64A

Fig. 2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SELECT
RESET
CS
REQ
CK2M
CK
CKB
D
S
C
R

Fig. 3

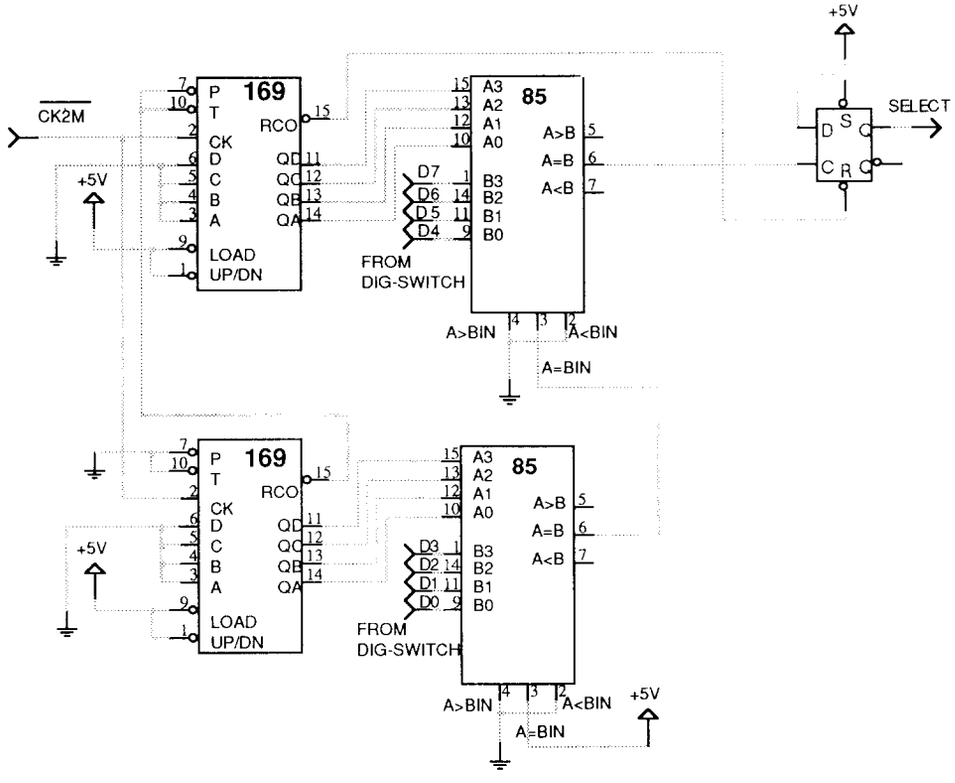
CK2M
+5V
169
P
T
CK
D
C
B
A
RCO
QD
QC
QB
QA
LOAD
UP/DN
85
A3
A2
A1
A0
B3
B2
B1
B0
A>B
A=B
A<B
D7
D6
D5
D4
D3
D2
D1
D0
FROM
DIG-SWITCH
A>BIN
A=BIN
A<BIN
SELECT
D
S
C
R

Fig. 4

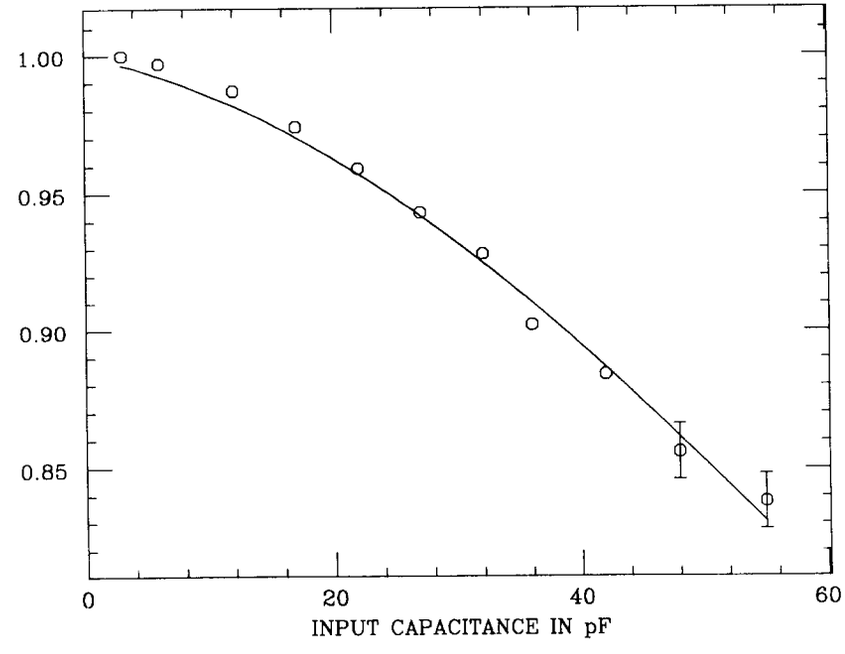
PULSE HEIGHT EFFICIENCY IN %
1.00
0.95
0.90
0.85
0
20
40
60
INPUT CAPACITANCE IN pF

Fig. 5

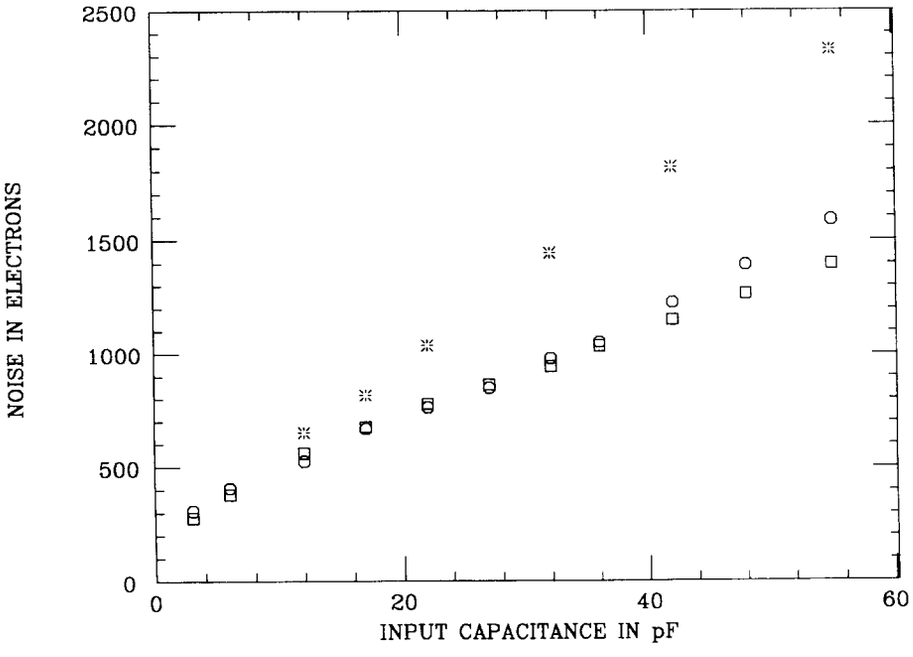
NOISE IN ELECTRONS
2500
2000
1500
1000
500
0
0
20
40
60
INPUT CAPACITANCE IN pF

Fig. 6