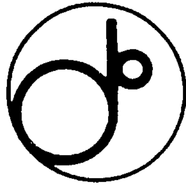
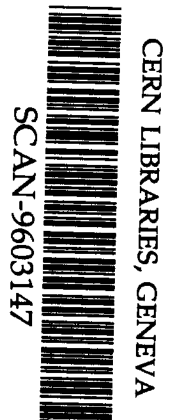
D)



KEK Preprint 95-147
November 1995
H

Fabrication of a Double-sided Silicon Microstrip Detector with an ONO Capacitor Dielectric Film

Y. SAITOH, T. AKAMINE, M. INOUE, J. YAMANAKA, K. KADOI, R. TAKANO, Y. KOJIMA, S. MIYAHARA, M. KAMIYA, H. IKEDA, T. MATSUDA, T. TSUBOYAMA, H. OZAKI, M. TANAKA, H. IWASAKI, J. HABA, Y. HIGASHI, Y. YAMADA, S. OKUNO, S. AVRILLON, T. NEMOTO, I. FUKUNISHI and Y. ASANO


CERN LIBRARIES, GENEVA
SCAN-9603147

SW9612

Submitted to
the 1995 Nuclear Science Symposium, October 21 - 28, 1995, San Francisco, CA, U.S.A.
and
to be published in IEEE Trans. Nucl. Sci.

National Laboratory for High Energy Physics, 1995

KEK Reports are available from:

Technical Information & Library
National Laboratory for High Energy Physics
1-1 Oho, Tsukuba-shi
Ibaraki-ken, 305
JAPAN

Phone:	0298-64-5136	
Telex:	3652-534	(Domestic)
	(0)3652-534	(International)
Fax:	0298-64-4604	
Cable:	KEK OHO	
E-mail:	Library@kekvax.kek.jp	(Internet Address)

Presented at the IEEE Nucl. Sci. Symposium,
October 21-28, 1995, San Francisco, California

Fabrication of a double-sided silicon microstrip detector with an ONO capacitor dielectric film

Y. Saitoh, T. Akamine, M. Inoue, J. Yamanaka, K. Kadoi, R. Takano
Y. Kojima, S. Miyahara and M. Kamiya
Seiko Instruments Inc.

H. Ikeda, T. Matsuda, T. Tsuboyama, H. Ozaki, M. Tanaka, H. Iwasaki
J. Haba, Y. Higashi and Y. Yamada
KEK, National Laboratory for High Energy Physics

S. Okuno
Department of Industrial Engineering and Management, Kanagawa University

S. Avrillon
Department of Accelerator Science, The Graduate University for Advanced Studies

T. Nemoto, I. Fukunishi and Y. Asano
Institute of Applied Physics, Tsukuba University

Abstract

Double-sided silicon microstrip detectors (DSSDs) in which integrated coupling capacitors containing an ONO (oxide-nitride-oxide) dielectric film were fabricated using newly developed processing techniques. We report the processing techniques and some characteristics of the detectors fabricated in this study.

I. INTRODUCTION

A silicon vertex detector (SVD) [1] for use in a KEK B-factory experiment (BELLE collaboration) consisting of detector units, which are assembled by the FCB method [2] and are a superlayer structure, will be constructed. The double-sided silicon microstrip detectors (DSSDs) to be used in the detector units will have not only bump electrodes but also require the same high level of quality as the other HEP experiments. In order to implement higher unit capacitance together with higher reliability and lower defect density, we proposed an ONO (oxide-nitride-oxide) dielectric film as a structure of an integrated coupling capacitor in the silicon microstrip detector [3, 4, 5]. However, the manufacture of the DSSDs still requires a high level of process engineering, such as the defect density of the dielectric film (strip yield) of the capacitor, the integration of high resistivity elements (bias resistors) and its uniformity, increasing the number of steps of the process (leading to possible defects or contamination) and particularly increasing the junction leakage current of the ONO situation [6]. In this study, we report the processing techniques and some characteristics of the fabricated detectors.

II. PROTOTYPE DSSD SPECIFICATIONS

The design geometry and target process parameters for the prototype DSSDs are as follows. A view of a part of the n-side design layout is shown in Fig. 1.

Parameter	Value
Si Substrate: n-type, <100>, 4 inches, 300 ± 15 μm	
Resistivity	4 - 8 kΩcm
Design parameters:	
Chip size (detector size)	34 x 67 mm
P-side:	
Strip width (diffusion)	5 μm
Strip pitch (diffusion)	25 μm
Strip pitch (readout)	50 μm
Number of strips (diffusion)	640 x 2
N-side:	
Strip width (diffusion)	5 μm
Strip width (active)	16 μm
(this forms the field plate structure [7])	
Strip pitch (diffusion)	50 μm
Strip pitch (readout)	50 μm
Number of strips	600 (x 2 blocks)
Process target parameters:	
ONO capacitor:	
Top oxide thickness	around 40 to 50 Å
Intermediate Si_3N_4 thickness	1500 ± 200 Å
Bottom oxide thickness	420 ± 20 Å
Bias resistor (both sides):	
Poly Si sheet resistivity	100 kΩ/□
(this composes 20 MΩ resistivity of bias resistor)	
Inter metal dielectric film (n-side):	
Polyimide thickness	5 μm

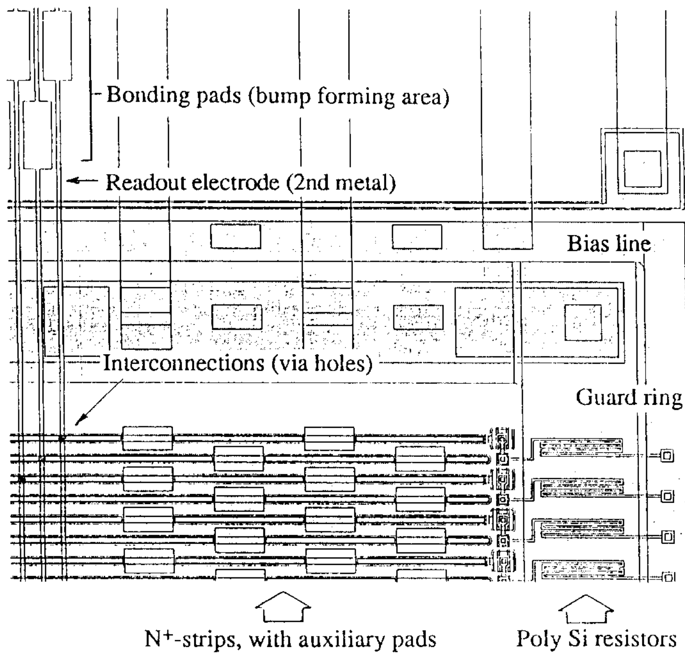


Fig. 1 A view of the n-side design of the detector.

II. FABRICATION

Newly developed features of the fabrication process are as follows:

- An ONO dielectric layer was formed as 420 Å thermal oxide at the bottom, 1500 Å CVD Si_3N_4 in the middle, and around 40 to 50 Å thermal oxide of Si_3N_4 at the top. This composition of thickness is to possibly achieve the highest unit capacitance (1.7 times larger than that of single layered SiO_2 [3, 4, 5]) within our application. The ONO layer was formed at the same time for both the p and n-sides.
- A poly Si gate is employed as an electrode of the integrated capacitor, instead of an Al metal gate. Directly after forming the capacitor insulator, both sides of the poly Si layer are deposited at the same time. From the MOS manufacturer's point of view, the poly Si gate is superior to the Al gate in order to prevent capacitor insulator failure and contamination.
- A poly Si high resistor is employed as a bias resistor for both sides. In this respect, the poly Si layer formed is identical to the gate poly Si (poly Si one layer process).

After deposition of the poly Si, blanket phosphorous ion implantation to the poly Si (control the resistivity) is carried out [shown in Fig. 2(a)]; next, partially N^+ ($POCl_3$) doping (with mask CVD SiO_2) is done [shown in Fig. 2(b)]; and then pattern forming of both the capacitor gates and the resistors is done at the same time.

The N^+ doped contact area at the interconnect of the metal and the poly Si is to prevent the forming of a contact barrier between the metal and the high resistivity poly Si.

- Si_3N_4 film removal on the field except the gate area is carried out as being self aligned to the poly Si gate (using RIE etching), using the remaining photoresist [shown in Fig. 2(c)]. This removal is to prevent an increase of junction leakage current [6] without an increase of mask steps (leading to possible defects and contamination). Together with the poly Si one layer process, this removal process (poly Si self align SiN removal) could be the only way to arrange the bias resistors above the guard ring region because it can be done without a reduction of gate oxide underneath the bias resistors, which leads to a minimization of nonsensitive areas.

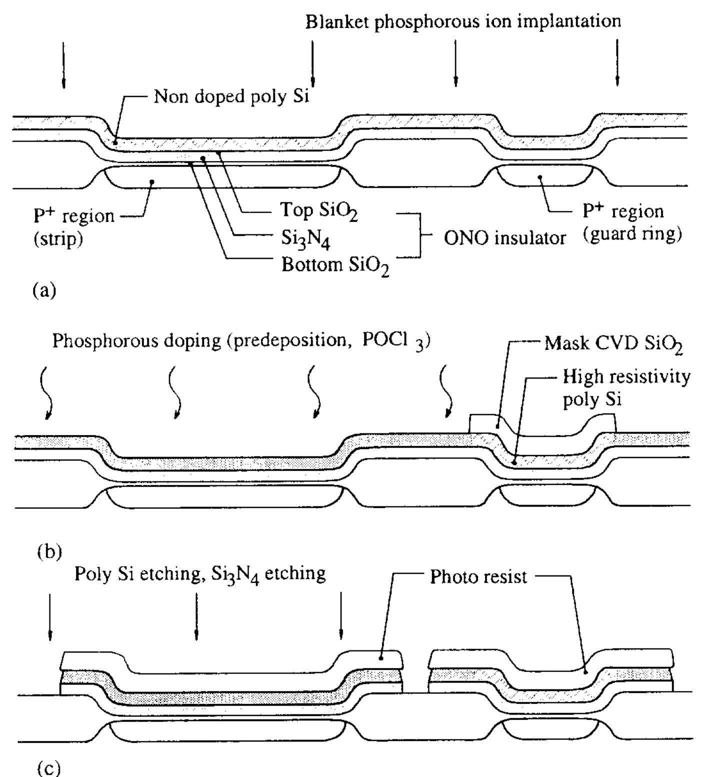


Fig. 2 Process flow of the poly Si one layer process and the poly Si self align SiN removal process.

The other features of the process are as follows: LOCOS SiO_2 is employed as a thick oxide within an inter strip along with the current CMOS process, in order to form the P^+, N^+ region using ion implantation as being self aligned to thick oxide and to prevent failure of the field oxide (CVD SiO_2 has many flakes). Multi layered polyimide is employed for the inter metal insulator film on the n-side, with multiple sizes of via hole (leading to sufficient metal-via hole step coverage). This is to prevent a stray capacitor between the 1st metal and the 2nd metal. Au bumps are formed on the pads of the detector unit assembly using the FCB method [2].

Fig. 3 shows a schematic cross sectional view of the detector fabricated in this study. Photo 1 shows the fabricated detector and test elements on a 4" Si wafer. Photo 2 shows the poly Si high resistors. Photo 3 shows the interconnections between the 1st metal and the 2nd metal on the n-side. Photo 4 shows the Au bumps arranged in double columns at 100 μm pitch.

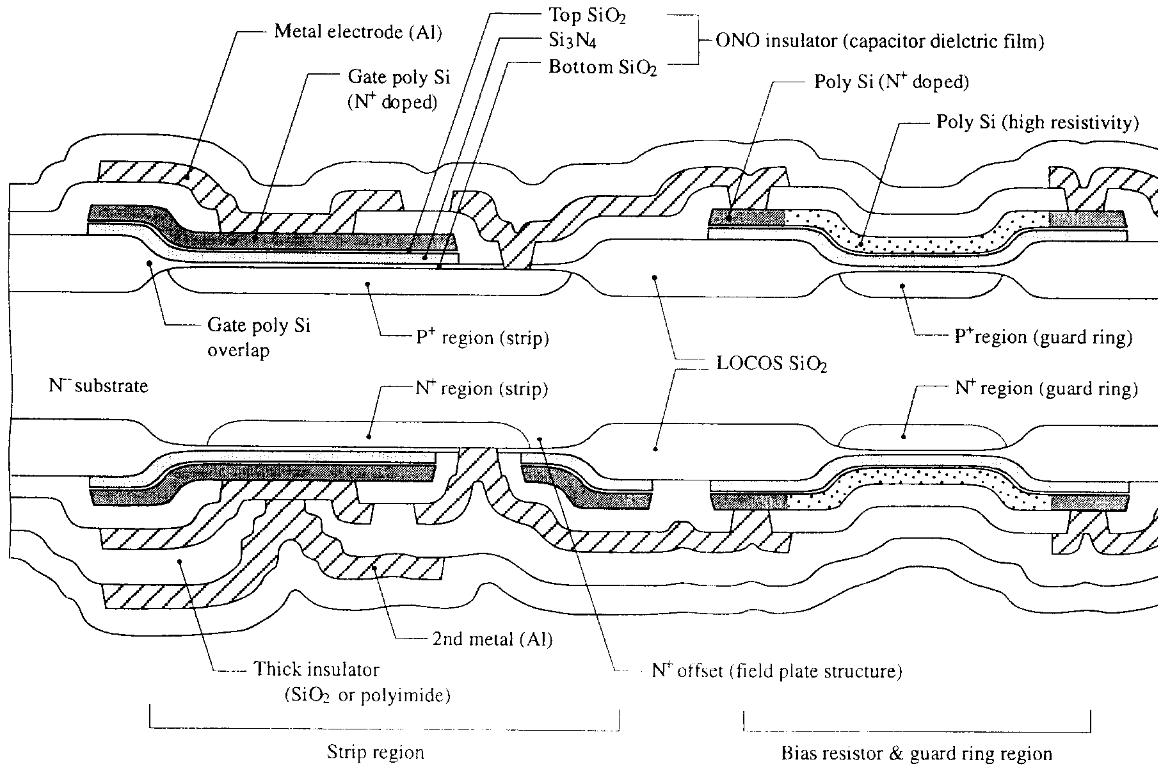


Fig. 3 Schematic cross sectional view of the fabricated detector.

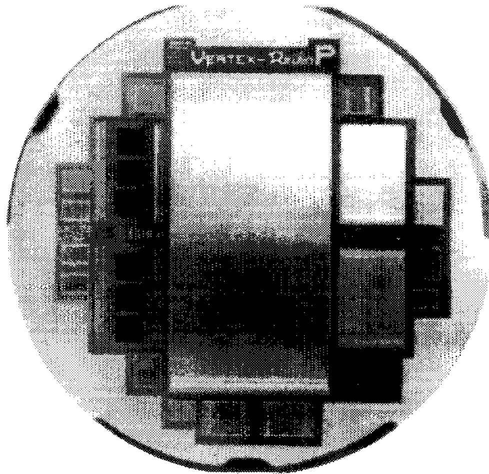


Photo 1 Fabricated detector and test elements on a 4" Si wafer.

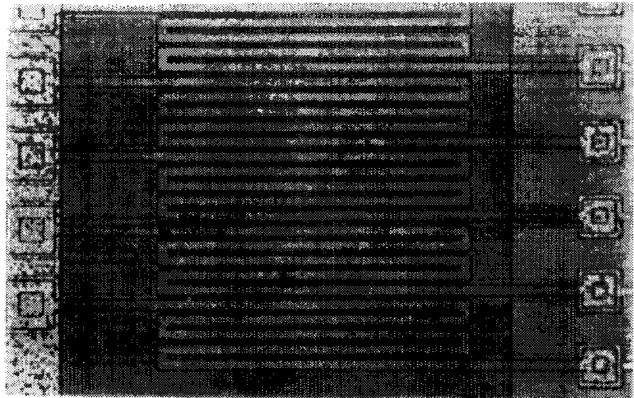


Photo 2 Poly Si high resistors.

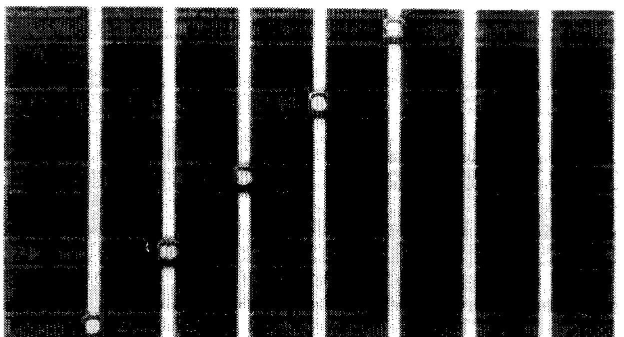


Photo 3 Interconnections between the 1st metal and the 2nd metal on the n-side.

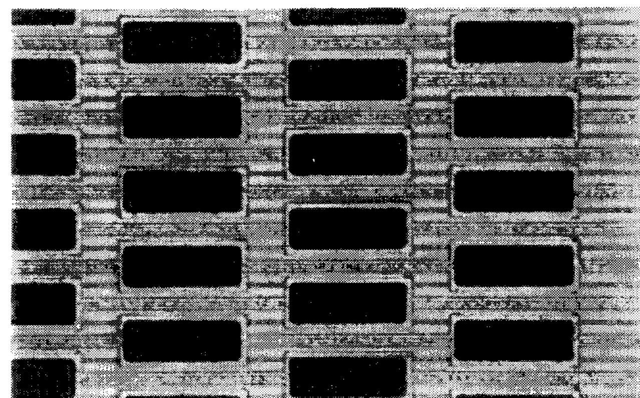


Photo 4 Au bumps arranged in double columns at 100 μm pitch.

III. Performance and Discussion

A. Strip yield and leakage current

The average strip yield and bias leakage current of the detectors fabricated in this study (ganged 640 x 2 strips through the bias resistors) is shown in the following table. While the criteria current for strip failure is above 1E-8 A, the actual data are normally below 1E-10 A.

Strip yield:	
P-side	98 - 99 %(at 80 V, 1E-8 A criteria)
N-side	(average 0.4 % reduction of p-side, with double metal configuration)
Junction leakage:	1 - 8 μA (at 60 V, while full depleted voltage was typically 40 V) (≈ 20 μA without SiN removal)

B. Poly Si bias resistor

Phosphorous ion implantation dosage to shoot the target resistivity of 20 MΩ was substantially obtained, the standard deviation (σ) of each detector was about 6 - 10%. Fig. 4 shows the controllability of resistivity and its uniformity as a function of phosphorous dosage and passivation. The double-sided process has repeated steps of heating around 430°C after metalization. Thus, the horizontal scale of heating process time (430°C) represents the reproducibility and stability of the poly Si bias resistor. Assuming the penetration of hydrogen from the P-SiN (SiN passivation film deposited by plasma enhanced CVD) into the poly Si, P-SiN passivation causes the instability of resistivity. As a result, we figured we should employ another type of passivation, e.g. polyimide film.

The partially N^+ ($POCl_3$) doping provided sufficient metal-poly Si contact without any unexpected barrier.

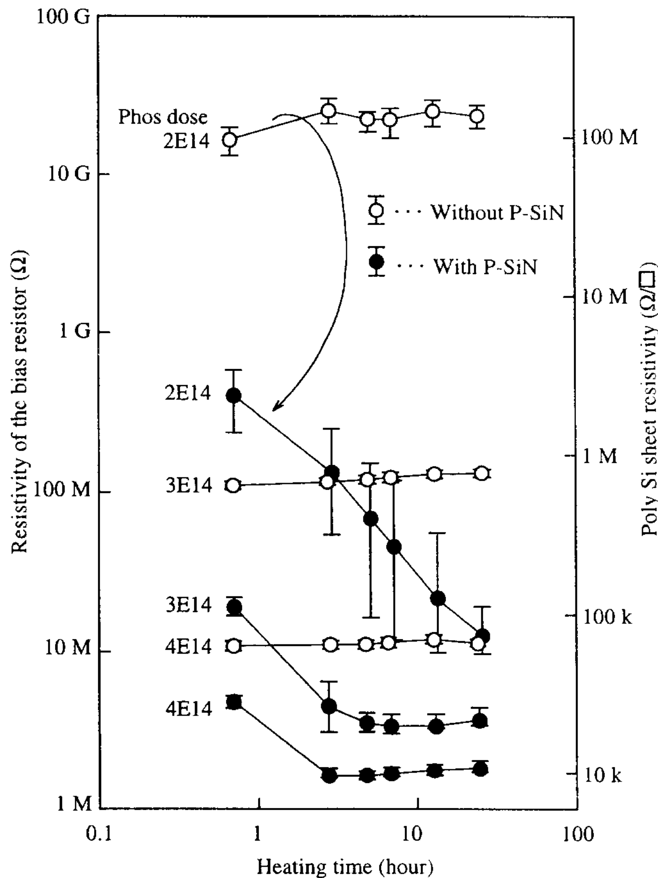


Fig. 4 Controllability of the poly Si bias resistor.

C. Signal response and related phenomena

Using newly developed SMA^2SH preamplifier chips [8, 9], the charge responses observed for a collimated IR light were adequate for our application [9, 10] (Fig. 5).

However, an increasing of the charge signal was observed along with an increasing of the leakage current in the over depleted voltage region. When the readout electrodes (field plates) for the n-side are biased to a voltage exceeding 50 V, the charge signal begins to markedly rise [10] (Fig. 6). We have not yet determined whether or not this increasing of the signal (not noise) is signal amplification.

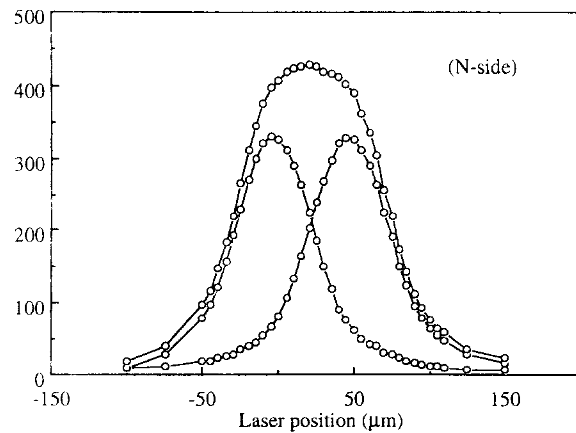


Fig. 5 Charge response of the DSSD measured with SMA^2SH chip. The data from two strips and their sum.

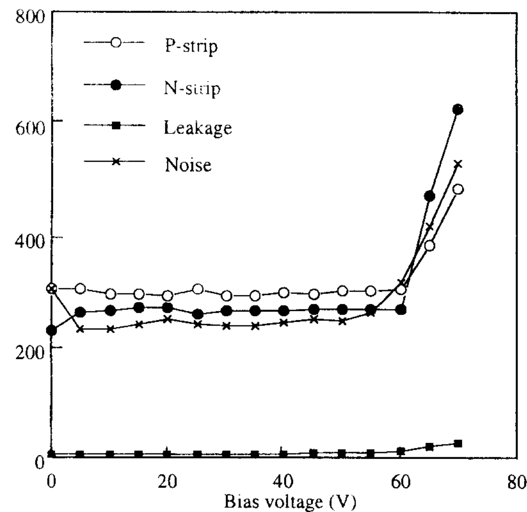


Fig. 6 Pulse height and the noise along with the bias voltage. The readout electrodes for the n-side are grounded.

straight line; (V_{NG}: the voltage difference between a N^+ strip and a field plate, I_N: the leakage current of a N^+ strip).

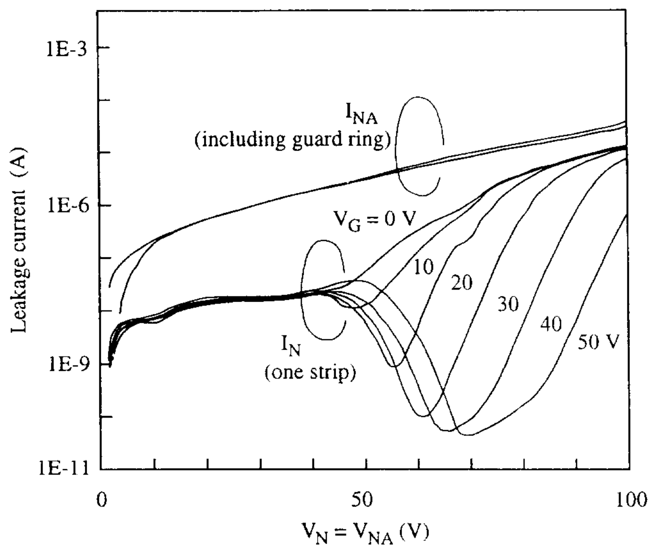


Fig. 7 Leakage current of one n-strip as a function of the field plate biasing.

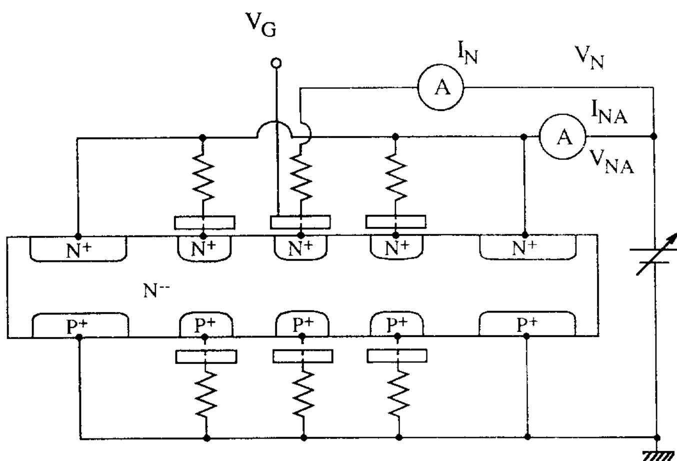


Fig. 8 Circuit configuration for the leakage current measurement.

Fig. 7 shows the leakage current of one n-strip as a function of field plate biasing. Fig. 8 shows the configuration of the circuit for the measurement of the leakage current. One strip and one readout are biased and the rest of the strips are all ganged, but the rest of the readouts are floating. The remarkable increasing of the leakage current along with the increasing voltage between the readout electrode and the N^+ strip region underneath, accompanied with a momentary dropping. This dropping is understood to be caused by the increasing of the inter strip resistance depending on above mentioned increasing voltage between the readout electrode and the N^+ strip region. Some people have suggested the relevancy between this kind of leakage current and the microdischarges of the P^+ strips [11]. However, we have understood this current is a BBT (Band to Band Tunneling; [12]) current. Because the calculation of $1/(V_{NG}-1.2)$ versus $\log I_N/(V_{NG}-1.2)$ fall on a

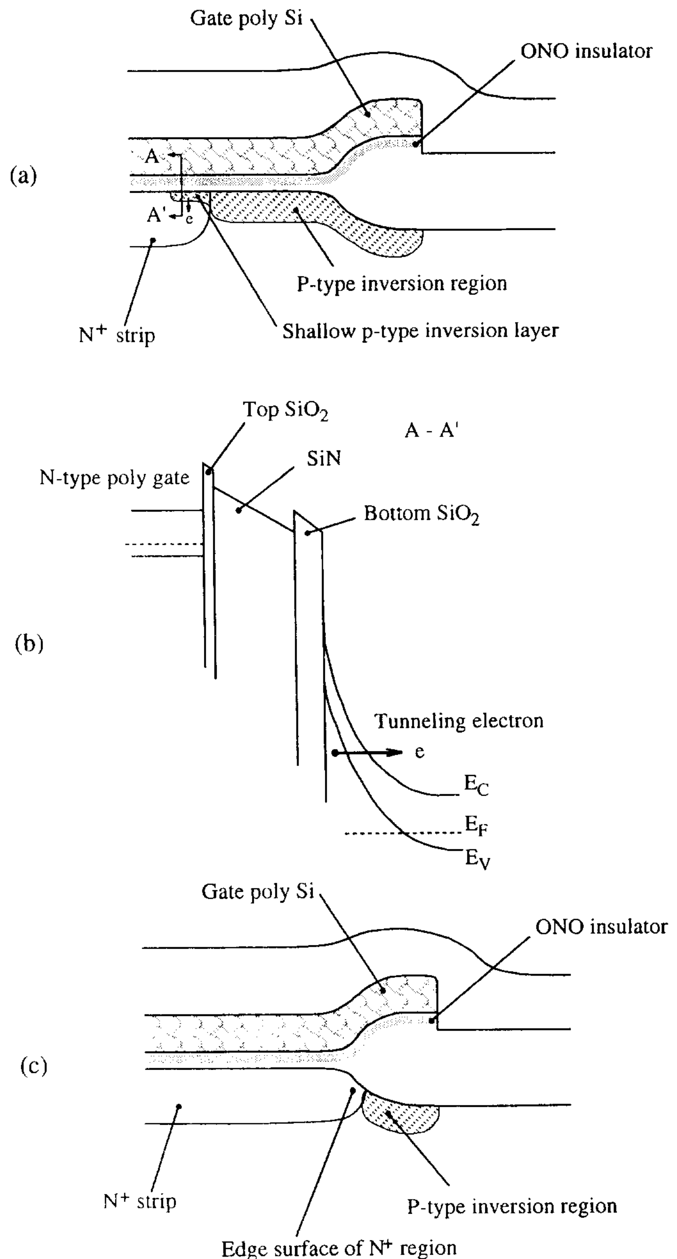


Fig. 9 Band bending at the N^+ edge surface.

The higher electric field of the ONO insulator seems not only to lower the voltage (around 15 V) in order to form sufficient inter strip resistance [10], but also to form an inversion layer encroaching onto the surface of the edge of the N^+ region [see Fig. 9 (a)]. Fig. 9 (b) shows a cut out (A - A') of the supposed energy-band diagram of Fig. 9 (a). Tunneling electrons flow from the shallow p-type inversion layer, a band which was strongly bent by the high electric field, into the N^+ region. The electrons from the shallow p-type inversion layer are provided through the outer p-type inversion layer which

touches a full-depleted region of the substrate. Therefore, this current (Field plate assisted BBT current; FBT current) is not expected to have enough energy to cause the microdischage phenomenon.

Fig. 9 (c) shows the plan of the modified N^+ strip and field plate structure. When the ion implantation to form the N^+ region is to be done as being self aligned to the LOCOS edge in the same manner as the p-side, the surface of the edge of the N^+ region is not strongly affected by the electric field due to the thick oxide above it. On the other hand, the surface of the N^{--} substrate and just underneath the field plate portion is expected to be affected and sufficiently inverted by the electric field, because the readout electrode the poly Si gate is N^+ type and a substrate is very low concentration N^{--} substrate. If we call the current N^+ strip structure in which the gate poly Si extending overlaps onto the N^{--} substrate through the thin insulator (ONO) "active field plate", we call the modified scheme above the "moderate field plate" structure.

The main advantages of the ONO insulator such as higher unit capacitance has not been evaluated in a signal detection, yet.

The micro breakdown noise supposed to be caused by microdischage [12] has not yet been found [9, 10]. This might be due to the p-side structure in which the gate poly Si extending overlap region has thicker oxide being self aligned to the P^+ region edge.

IV. CONCLUSION

The prototype DSSDs in which an ONO dielectric film within integrated coupling capacitors using newly developed processing techniques particularly the combination of the poly Si one layer process and the poly Si self align SiN removal process could achieve the acceptable specification for HEP application in terms of strip yield, leakage current, bias resistors and inter strip isolation.

Although the prototype DSSDs together with newly developed SMA^2SH preamplifier chips could eventually provide sufficient charge responses for a collimated IR light, they could not yet exhibit the main advantages of the ONO insulator, i.e. higher unit capacitance in our current signal detection system.

While the ONO dielectric film (thickness composition for highest unit capacitance) together with the field plate structure for the N^+ strip could provide very low voltage for forming sufficient inter strip resistance, an FBT current could occur and represent a limitation to the biasing configuration. The modified "moderate field plate" structure is to be carried out on another occasion.

The increasing (amplification) of the charge signal seemed to be caused by the FBT phenomenon and is to be examined.

V. ACKNOWLEDGMENTS

The authors wish to thank Dr. P. Weilhammer, CERN/PPE and Dr. R. Horisberger, PSI, for introducing us to the field of microstrip detector engineering, we also wish to thank all the people of BELLE collaboration.

VI. REFERENCES

[1] BELLE collaboration, "A Study of CP Violation in B Meson Decays (Technical Design Report)", KEK-Report 95-1, April 1995

[2] Y. Saitoh et al., "Development of Novel Fabrication Techniques for a Silicon Micro-Vertex Detector Unit using the Flip-Chip Bonding Method", IEEE Trans. NSS, Vol. 40, No. 4, 1192-1196, August 1994

[3] S. Okuno, H. Ikeda, T. Akamine, Y. Saitoh, K. Kadoi and Y. Kojima, "New Insulator Film of Integrated Capacitor for Silicon Strip Detector", 1993 IEEE Conf. Record, Nuclear Sci. Symp. and Medical Imaging Conf., Vol. 1, p. 48, October 31- November 6, 1993.

[4] S. Okuno, H. Ikeda, T. Akamine, Y. Saitoh, K. Kadoi and Y. Kojima, "A Stacked Dielectric Film for a Silicon Microstrip Detector", Nucl. Instr. and Meth., A 361 (1995) 91-96

[5] S. Okuno, "Stacked Dielectric Film for a Double-sided Silicon Microstrip Detector", Doctor thesis, the Graduate University for Advanced Studies, 1995

[6] S. Holland, "An Oxide-Nitride-Oxide Capacitor Dielectric Film for Silicon Strip Detectors", IEEE Trans. NSS, Vol. 42, No. 4, 423-427, August 1995

[7] R. Brenner et al., "Results from double-sided silicon microstrip detector with field plate separation", Nucl. Instr. and Meth., A326 (1993) 198-203

[8] H. Ikeda et al., "Single-channel prototype of a CMOS SVD preamplifier for the B-factory experiment, BELLE", KEK Preprint 95-89, July 1995

[9] H. Ikeda et al., "Charge partitioning study of a wide-pitch silicon micro-strip detector with a 64-channel CMOS preamplifier array", Presented in the 1995 IEEE NSS, San Francisco, Oct 1995

[10] T. Tsuboyama et al., "Test of a new double-sided double-metal silicon micro-strip detector with an ONO insulator", Presented in the 1995 IEEE NSS, San Francisco, Oct 1995

[11] J. Matheson et al., "Radiation damage studies of filed plate and p-stop n-side silicon microstrip detectors", Nucl. Instr. and Meth., A362 (1995) 297-314

[12] J. Chen et al., "Subbreakdown Drain Leakage Current in MOSFET", IEEE Electron Device Letters, Vol. EDL-8, No.11, November 1987

[13] T. Ohsugi et al., "Microdischarges of AC-coupled silicon strip sensors", Nucl. Instr. and Meth., A 342 (1994) 22-26