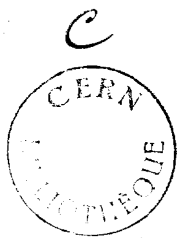
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R&D Proposal
Development of hybrid and monolithic silicon micropattern detectors

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Abstract

A collaborative effort is proposed to continue the development, which started in the framework of the CERN-LAA project, of a true 2-dimensional semiconductor particle detector with micrometer precision and with on-chip signal processing, a so called micropattern or pixel detector, for use in high luminosity colliders like the LHC. Different institutes will pursue in a complementary way both the hybrid approach and the monolithic approach. If the Silicon - On - Insulator (SOI) technology can be shown effective, both approaches could merge into a single effort. The first experimental devices can be tailored to serve intermediate physics experiments with fixed target or at the LEP collider, thus verifying the feasibility of the pixel detector technology.

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1. Introduction.

1.1 History

The use of one-dimensional silicon diode microstrip detectors, introduced about 10 years ago[1], has become widespread because they combine several crucial properties: particle localization with ≈5 μm precision in one coordinate, double hit separation better than 100 μm, geometrical precision better than 1 μm, signal charge collection in less than 20 ns, bias voltage below 100 V, easy installation and reliable operation. The production of silicon detectors is based on the microelectronics planar manufacturing technology. Progress in this technology is driven by considerable economic interests and ever smaller, more sophisticated electronic structures are becoming feasible. Therefore, it is now realistic to consider as a natural extension to the microstrip detectors the development of unambiguous two-dimensional particle detector arrays which incorporate the first stages of the signal processing electronics in an area equivalent to the detecting area. Following the terminology developed for optical imaging devices, the basic cell (picture element) in an array is called a 'pixel', whence 'pixel detectors'. Chips which have signal processing as well as a certain degree of data reduction can be called **micropattern detectors**[2]. Such detectors should produce unambiguous two-dimensional position information for selected events only.

1.2 Serial vs. parallel pixel detectors

Photodiode arrays and Charge Coupled Devices (CCD) are already used as pixel detectors for electronic imaging. The speed required for most optical applications allows serial scanning of the array, and the on-chip signal processing (e.g.Correlated Double Sampling) can be restricted to a single output channel. In a CCD the signal charge is transferred to the output node by physically shifting it through a row and a column of pixels. In Direct Read-Out devices (DRO) the pixels are serially addressed and read via a bus. In some devices the addressing may be selective as in a Random Access Memory (RAM). In the former architectures the readout time is several ms e.g. for a 500 x 500 pixel array.

Serial readout can be used in linear collider experiments, e.g. at SLC [3] , but it is inadequate for the high luminosity hadron colliders, and for on-line trigger decisions in fixed target experiments. It remains to be seen to which extent the LEP experiments can continue to use serial readout for the present microstrip detectors in the high-luminosity option. For these high rate environments new, parallel signal processing structures and information readout architectures have to be developed.

1.3 Motivation

True two-dimensional detector arrays with geometrical precision of a few μm and time accuracy of a few ns will be of paramount importance to resolve an otherwise unmanageable number of ambiguities in space and time, which will be encountered in a high luminosity hadron collider. The physics applications will be discussed in ch. 2. Some proposed physics experiments in LHC are supposed to be less critical regarding spatial precision on tracking However, one certainly cannot afford to delay the technological development until more exact requirements and specifications are known, i.e. only once the first experiments have started.

One aspect of our proposal is to establish the advantages that true two-dimensional detection presents over the use of detectors with projective geometry, like wire chambers, single or double-sided silicon microstrip detectors or scintillating fibers. Complementarity of pixel and projective detectors is evident.

1.4 Program of development

The development of micropattern detectors will require a significant effort over a relatively long time period, but it will be facilitated by synergetic developments going on in other fields of imaging, in particular X-ray and Infra-Red (IR) imaging. We intend to follow the trends in optical image processing to incorporate 'on-chip' advanced information processing operations for pattern recognition, for example edge detection and contrast enhancement. For some manipulations one can design device structures that operate in the charge domain. The alternative is to implement an on-chip ADC and use digital signal processing.

We propose here the development of a first generation pixel detector with on-chip signal processing and sparse data readout. We take the already existing experimental readout chip [4], developed in the framework of the LAA program as the starting point. An introductory discussion of the characteristics of pixel detectors is given in chapter 3. In the chapters 4, 5 and 6 the plans for the development work are explained in detail. It is our intention to design the next pixel detectors such that they can be tested under real conditions in a fixed target experiment. The testing of these experimental devices is discussed in chapter 7. Another version will be adapted to application in LEP, in order also to provide for extensive testing in a realistic collider situation. While testing devices in these intermediate applications we keep in mind to include those features needed to make the micropattern detector suitable, in particular regarding its speed, for vertex detection in the future high luminosity Large Hadron Collider (LHC).

The influence of radiation damage effects must be carefully evaluated, because the viability of semiconductor systems close to the interaction region will strongly depend on the available rad-hard semiconductor processing technology and the rad-hard design possibilities. A discussion is given as part of chapter 3.

2. Applications of high resolution pixel detectors.

2.1 LHC tracking, vertex detection and time-tagging

The most important application of semiconductor micropattern detectors will be vertex detection and tracking inside experiments at a high luminosity hadron collider, using the configuration which has been called 'point-back hodoscope'[5]. At small radii the particle track density in the cone of a decay is several 10^2 per cm^2 which is too high for microstrip detectors, which have typically 400 elements per cm. The true two-dimensional information of a micropattern detector solves the position ambiguity problems inherent to one-dimensional detectors. The fast signal collection time in the low-capacitance silicon detector elements allows detection of events up to a rate of 70 MHz and the exact time-space correlations ('time-tagging') from the pixel detectors may therefore also be helpful in solving ambiguities in slower devices elsewhere in the experiment. Signal processing and memory functions as well as selection of useful information should be integrated into the device in order to reduce the amount of data to be transmitted to the data acquisition system. However, the cost of pixel detectors is likely to be high, even taking into account a diminishing unit manufacturing cost at large numbers. Therefore, an economic approach may be the combination of one or two layers of pixel detectors with several layers of projective detectors, like silicon microstrip detectors or scintillating fiber detectors.

2.2 B-tagging in LHC

Whereas some of the physics phenomena expected at the TeV hadron colliders are supposed to be detected easily without any high resolution tracking, other phenomena resulting in enhanced numbers of charm and beauty decays predictably will need it. Because these decays proved to be a clear signature for new physics, many of the present collider experiments and fixed target experiments have introduced high resolution silicon devices, either in the original set-up or as a later upgrade. In particular, Bedeschi et al. in the ECFA Workshop in Aachen [6] discussed in some detail the B tagging for top quark studies. This will be an essential method in order to improve the signal/background ratio. Detailed argumentation in favor of the use of pixel detectors in hadron colliders has been given also in the SSC R&D proposal by Arens et al. [7].

2.3 Vertex detection in fixed target experiments

In the NA32 fixed target experiment it has been shown[3] that the use of a pixel detector, which consisted in that case of a slow readout CCD, leads to considerable improvements in track separation, pattern recognition and therefore background rejection. In a fixed target experiment the pixel detector can be used as a 'point-back hodoscope' but also in a 'direct decay detector' configuration, as used originally in NA1 and for some time also in NA32.

Even a relatively modest pixel detector could be tested and would find immediate application in a fixed target experiment such as WA92 which is designed to identify beauty decays within an array of silicon microstrip detectors. In this experiment the needed spatial precision is provided by 10 μm pitch microstrip devices. The role of the pixel detector would be to reduce the ambiguities of space track reconstruction. The faster readout speed (compared to the CCD) would be essential in a beauty hadroproduction experiment because of increased event rate.

2.4 Heavy ion physics in a fixed target experiment and at the LHC

Another area in which high resolution two-dimensional pattern detectors are being considered is the heavy ion research program, which aims to achieve, in the collision of two heavy nuclei at relativistic energies, the condition for a phase transition from hadronic matter to a plasma of quarks and gluons. CERN has already a fixed target heavy ion program and the possibility is now under study of using the future LHC to collide beams of lead ions at 3 TeV per nucleon. The large event multiplicities expected, of several thousand tracks per event, suggest the use of micropattern detectors for tracking and vertex detection. In particular the detection of hyperons and cascade decays, which is of importance to study the behaviour of hadronic matter under the extreme conditions necessary for a phase transition, cannot be envisaged at LHC without this type of detector.

It will be very useful in any case to evaluate the first experimental devices in a high multiplicity fixed target experiment. These tests could be performed in the Omega WA85 heavy ion experiment, and this would also fit well in their experimental program.

2.5 LEP collider experiments

It is important to proceed in an early stage with the testing of pixel devices in a collider environment. Amongst the LEP experiments there is a big interest in testing specially adapted prototypes of the silicon micropattern detector. The DELPHI experiment is considering the option of building a silicon pixel detector layer to be used with the existing structure of the microstrip vertex detector recently built. In addition to the existing layers of microstrip detectors and the upgrade with double-sided detectors a pixel detector might enhance the pattern recognition. A further discusion will be given in section 7.

2.6 Readout of scintillating fibers

Silicon CCD have been mounted within a vacuum electron tube in order to detect accelerated electrons coming from a photocathode. Instead of using CCD with their inherently slow readout cycle one could mount a silicon pixel detector inside the tube, provided the connections have vacuum-compatible properties. It should be relatively straightforward to detect 30-50 keV electrons in the pixels, having already demonstrated [4] a noise performance of 4 keV FWHM.

3. Characteristics of a silicon micropattern detector.

In this chapter an introduction is given to the various technical aspects of pixel detectors: their construction, the detector function, the 'on-chip' signal processing electronics and the hierarchical organization of a detector system.

3.1 Monolithic and hybrid devices.

There are two approaches to the realization of a semiconductor pixel detector : the detector function and the signal processing electronics can both be located in the same **monolithic** piece of silicon, or these two functions can be implemented in two separate chips which are afterwards connected into a **hybrid** device. Several technologies for these two approaches are illustrated in fig.1 [8]. The hybrid approach receives more attention in this proposal because in our experience the potential for quick progress towards practical devices is greater when using a hybrid system. The benefits of a monolithic detector, however, are considerable and we propose also to continue a parallel development.of high resistivity silicon processing, aimed at Silicon - On - Insulator (SOI) devices. Ultimately, in a SOI pixel detector many properties of monolithic and hybrid devices may be merged.

3.1.1 Hybrid structures

The advantage of a hybrid construction is the independent choice of readout chip and detector material. This makes it much simpler to adopt easily-accessible, standard manufacturing methods for these components separately. However, the complications are then shifted towards the connection between detector chip and readout chip, in which we have in Europe until now little experience. Several interconnect processes have been developed in specialized industry, but the tooling cost is considerable and in most cases the status is still experimental rather than ready for mass production. The metallic interconnect bumps may increase the radiation length of the device, and yield of good connections and long term reliability are of concern. A conceptual mechanical design illustrated in fig.2 shows how arrays of hybrid devices can be built to provide nearly hermetic detection in a collider.

The program related to the hybrid interconnection technology and packaging will be detailed in ch. 5.

3.1.2 Monolithic high resistivity silicon detectors

By constructing all functions in a single substrate of high resistivity silicon the overall detector material thickness may be reduced, the construction may be simplified and even the manufacturing cost might be lower than in the case of hybrid devices. The most important advantage probably is the reduction of stray capacitance at the amplifier input, which should improve the noise performance.

Compared to the development of a hybrid device, more work has to go into the development of a non-standard CMOS processing technology for high resistivity silicon, and the individual performance of electronics and detector may not be optimal. In order to evaluate the practical aspects of such a development, a collaboration has been initiated between CERN and IMEC (Leuven) several years ago[9]. An experimental process has been developed in which one is allowed to design CMOS compatible analog circuits as well as particle detector diodes. The resistivity of the starting material is practically not degraded by the processing and low-leakage detector elements can be produced. The first experimental structures have been manufactured recently [10] and an extensive progress report is provided in the thesis of G. Vanstraelen [11].

It is our intention to continue this line of development within the framework of the present proposal, but including now also possibilities which are offered by the SOI technology. In order to achieve 'mass-production' of devices, a transfer of the experimental processing to an industrial environment has later to be envisaged. The objectives for the work until the end of 1992 are described in ch. 6.

3.2 Pixel size, detector manufacturing and detector operation.

The granularity of the pixel detector has to be chosen to fulfill a number of contradictory requirements. Detection precision and double track resolution are dictated by the experimental **physics** application. Depending on the magnetic deflection, it may be sufficient to have a good precision ($\approx 10\ \mu m$) in one dimension only. An elongated pixel shape then enables the necessary signal processing electronics to be accomodated. The occupancy in the high luminosity environment, in conjunction with the time needed for the first level trigger decision, determine the probability for a single pixel to be hit twice. Smaller pixels have a smaller double hit probability. If multiple hits may occur, the electronics has to be more complex, which will increase its size. Therefore, smaller pixel area may be desirable.

An important aspect of the pixel detectors is the **power** dissipation. It has been remarked already on several occasions[e.g.12], that a finer segmentation leads to lower power consumption in the analog front-end part, for a given noise performance. Again, this leads to favour small pixels. Obviously, the digital control part is increased in size and power and a trade-off has to be made.

The size of the pixel, the detector thickness and the connection pad determine the effective input capacitance and thereby to a large extent the **noise** of the input amplifier circuit. The lower this noise, the thinner the active detector layer can be. A chip thickness of 150 μm is probably at the limit of handling possibilities for hybrid fabrication. A 150 μm thick Si detector delivers a signal of $\approx$12000 e-h pairs and has a capacitance of 7×10^{-7} pF per μm^2 or 2 fF for a 30 μm x 100 μm pixel, which causes a small contribution to the overall noise.

In the presently proposed hybrid devices the pitch is determined by the size of the **electronics** circuit, and the existing experimental chip has a 200 μm pitch. The ultimate pitch most likely will depend on the precision of the bump bonding process, rather than on the space needed for the circuit. The most advanced technologies may allow a pitch of 20 or 25 μm , but 50 to 100 μm is achievable at present.

The area needed for the electronics functions obviously depends on the desired complexity. In a full analog design the area needed may be significantly larger than in a simple digital design with immediate discrimination. In this proposal we should like to pursue both designs in order to make a cost/benefit analysis.

A final consideration for the pixel size comes from the expected leakage current degradation due to the high dose irradiation. This is discussed in the following section. A realistic aim for the pixel size in the next experimental device is 75 μm x 200 μm. Ultimately, one should like to achieve 20 or 30 μm in the smaller dimension.

The manufacturing of test detectors is currently undertaken in the collaborating laboratories in Bologna/Modena[13] and in Pisa. Test samples also have been ordered from the Senter for Industriforskning, Oslo. Once the next array designs have been finalized, the specifications for prototype detectors will be defined and offers will be invited from the usual European manufacturers.

3.3 Detector degradation by radiation effects.

Radiation damage is a major concern for the application of semiconductor detectors in supercolliders[14]. The effects are: increase of leakage current, carrier removal which modifies the effective material resistivity, and signal charge trapping.

The **reverse diode current** increases linearly with the dose received but no definitive agreement exists as yet on the precise value of the coefficient. This current causes increase of detector noise and saturation of the DC level of the signal processing circuit. The amplifier can be made tolerant to the increase of current up to a level of 100 nA[4]. We adopt here the same current coefficients as in [15], i.e. 10^{-17}A cm^{-1} for minimum ionising particles (mip), and 10^{-16}A cm^{-1} for albedo neutrons. Lindström et al.[16] have recently made detailed studies of the current increase by neutron and proton irradiation. Their results indicate that the number for minimum ionizing hadronic particles may be slightly higher than the coefficient given above, which was based on lepton irradiation, whereas the neutron number may be lower due to the previous neglect of the neutron energy dependence. The effects of an identical dose by high energy electrons or by muons are not equivalent, and certainly the same photon dose (e.g. from ^{60}Co) gives several orders of magnitude lower current increase.

Using the preliminary coefficients given above a radiation induced leakage current of 100 nA will be reached in a pixel volume of 30 µm x 100 µm x 150 µm after ≈ $2x10^{15}$ neutrons/cm^2 or 550 Mrad of ionizing mip radiation, which are accumulated in LHC after ≈ 10 years of operation. Note that this current would correspond to 3 mA at 60 V bias or ≈ 0.2 W per cm^2. Eventually, the power dissipation in the detector will become equal to that in the electronics readout. The current increase in a detector element can be limited by lowering the temperature, by chosing a smaller pixel size or ultimately by using a higher bandgap semiconductor, e.g. GaAs.

The modification of the **detector resistivity,** eventually even the reversal from n-type Si to p-type Si has recently been studied by Li and Kraner [17]. It has to be taken into account from the outset, probably by providing channel stops between the pixel elements. The signal **charge trapping** has not been studied sufficiently to determine if it represents a problem for fast detector operation. Increase of bias voltage may be sufficient to counter the trapping effect and also the cooling of the detector will have a beneficial effect.

The radiation effects in the **readout electronics** are supposed to be easier manageable, given the extensive experience in this field in specialized industry. Various contributions [18] in the ECFA-LHC Workshop in Aachen have illustrated the state of the art. In advanced rad-hard digital integrated circuits 10 to 100 Mrad of ionizing radiation can be tolerated as well as 10^{15} neutrons/cm^2. This is comparable to the tolerance of the small-size pixel elements at room temperature. The development effort needed and the cost involved may still be substantial, however. Separate projects are currently being proposed for these studies[19].

3.4 Signal processing electronics.

In a preliminary feasibility study it has been concluded that fast (10 MHz) circuits can be designed within the power and space budgets [20]. Subsequently, an experimental direct readout circuit has been designed [21] and tested up to 10 MHz [4]. The properties of this existing circuit are described in table 1, and a comparison is made with the projected characteristics of a micropattern detector for high luminosity colliders.

Table 1 Characteristics of a silicon micropattern detector.

parameter	[4]LAA experimental DRO chip	vertex detector collider
pixel size	200 µm x 200 µm	30 µm x 100 µm
array size	9 x 12	256 x 128
functionality	comparator,digital memory	comp., analog+digital memory
readout	external	sparse,time-stamps
chip size	2 x 2.5 mm^2	15 x 15 mm^2
technology	3 µm SACMOS	<1 µm SOI or GaAs
typical input charge	10 000 e^-	10 000 e^-
clock frequency	synchronous, 10 MHz	70 MHz
signal peaking time	30 ns	5 -10 ns
analog memory time		10 µs
„ „ dynamic range		100 000 e^-
comparator response time	100 ns	20-30 ns
power supply voltage	3 V	3 V
power dissipation per pixel	30 µW	30 µW

The development in signal processing electronics has to focus on the design of faster circuits which still achieve low noise and low power consumption. For the moment, a 2 µm or 3 µm technology still can be used for prototype studies, but eventually rad-hard, sub-micron processing will have to be adopted.

The choice of combined analog-digital or pure digital signal processing depends on the objectives of the experimenters, the actual feasibility of digesting the amount of analog data in off-line analysis and the capability of the circuit designers to compact all circuitry into the small space available. In the first experimental circuit [4] only digital output has been implemented.

In this proposal we should like to develop also a combined analog-digital solution. Details will be discussed in ch. 4.

Development of readout circuits for a hybrid pixel detector is also undertaken by an SSC collaboration[7, 22, 23]. They opt for analog storage and readout, and have even studied a processor architecture[24] which would calculate track segments for all SSC events, for use in the first level trigger decision.

3.5 Hierarchical detector organization.

A possible mechanical layout for a LHC hybrid pixel detector array is sketched in fig.2. The **chip size** of an individual pixel detector chip is unlikely to be bigger than 15x15 mm^2. This size is dictated by the availability of photolithographic equipment in the normal CMOS processing. Some companies project the use of chips of a square inch by the turn of the century, using direct writing on wafer, either with electron beams or synchrotron X-ray beams. The cost of such methods for small scale productions of less than thousand wafers is prohibitive. Present factories using optical masks may process up to 1000 wafers per day, which corresponds to over 10 m^2 of Si and about 100 000 chips [25].

The area to be covered by a microvertex detector in LHC is of the order of a few m^2 for each layer. This corresponds then to $\approx 10^8$ pixels per layer, on about 10^4 chips. If the same pixel detectors would be used for tracking at larger radii, these numbers could be 10 or 100 times as high.

An attractive approach to the readout of the numerous pixels would be to organize them hierarchically, like is tentatively illustrated in table 2. The hierarchy may have to be modified in view of physics requirements or mechanical constraints. The basic construction blocks are the detectors, each carrying 8 readout chips, like sketched in fig.2. The detectors can be grouped in regions, which can be planar or can be organized in a tower structure. Each region will contain about 2 million pixels on 64 detectors, and can be controlled by a supervisor circuit. Regions probably should be matched to the geometry of calorimeter towers or other tracking devices [15]. Regions also could be construction units of the system, and communications between regions, layers and the rest of the detector could be channeled via the supervisor circuits. Drivers for longer distance, possibly using optical fibers, can be located near or on the supervisor rather than on the detector devices.

Table 2 Hierarchy in a silicon micropattern detector system.

hierarchical level	description	number of elements
system	16 radial segments	
radial segment	16 regions per radial segment	
region	8 detectors per region of $\approx$ 60 cm^2 supervisor chip over 64 readout chips several layers or single plane ?	256 regions in total
detector	80 mm x 9 mm, 8 readout chips per detector	2048 detectors total
readout chip	chip size 7.7 mm x 13 mm = 255 x 128 pixels + area for logic : 13 mm x 13 mm	16384 chips total
row of pixels	row of 255 pixels	128 per chip
pixel	basic unit, e.g. 30 μm x 100 μm	128 per row, 32768 pixels/chip total 5.4 x 10^8 pixels

4. Plan for development of signal processing circuits in CMOS.

4.1 Analog electronics

Considerable experience has been gained in the course of the feasibility studies [10,11], the subsequent design work and the measurements on the first experimental circuit. New insights and new ideas now await implementation .

The basic building blocks in the pixel circuit are the front-end amplifier, shaper, peak detector, comparator and memory elements for the analog and digital data. Rather than looking at these building blocks separately, we will design them with an overall optimization in mind, and it may be possible to combine several of the functions in order to reduce the number of transistors [26]. To decrease the influence of matching inaccuracy, in particular for the comparators, a high gain in the front-end stage is desirable. On the other hand, calibration techniques e.g. using a dummy pixel element in a 'master/slave' approach, may be introduced to automatically tune a number of pixel circuits locally. The matching problems become more severe as device geometry decreases and as the distance between the elements to be matched increases.

It is planned to design in the first phase of this proposal a new, asynchronous pixel circuit with minimal size and digital output only, still using the 3 µm CMOS technology of Faselec, which can be easily accessed via the Multi Project Wafer service of CSEM. The block diagram of this circuit is illustrated in fig.3. In addition, a modified circuit will be made which also has analog storage and output, but this cell will certainly be bigger in area. Speed, noise and power are expected to remain about the same as in the earlier, experimental design. A 16x64 array will be constructed using this new pixel circuit, and together with the previous 9x12 array and a number of test structures it will be manufactured in a special engineering run at Faselec.

In the second phase a design similar to that of the first phase will be made, but using a more advanced and, if possible, radiation tolerant CMOS technology, e.g. 1.2 µm of ES2 or the SOI-CMOS technology of Thomson TMS [19]. These technologies have not been used by any of the collaborators as yet, and some work is therefore needed to set up technology files and to measure and evaluate circuit simulation parameters. We want to incorporate in this second phase also some test circuits to study the calibration techniques mentioned above.

4.2 Readout electronics circuits

In the first version of the 16x64 array a simplified readout scheme will be implemented, as illustrated in fig.4. After an external trigger signal is received all the data of the corresponding event will be shifted out in parallel in digital form, organized in 16-bit words, at 5 or10 MHz. A digital delay of 500 ns in each pixel cell allows pipelining of all signals until this first level trigger decision.

In the final LHC pixel device the trigger speed and the number of pixels in a detector (hundreds of millions) are such that it is mandatory to read only the hit pixels instead of all the pixels. A fast selective readout scheme has already been made and simulated at the Collège de France, to be included in a separate version of the 32x16 array. The principle of this system is illustrated in fig.5. Each pixel is regarded as a position memory cell and if a pixel is hit, the memory is set and a connection between X-Y row and column bus lines is made. Rows and columns are scanned and encoded according to priority. The system includes management for multi-chip priority. This enables a sparse data scan of the hit pixels in a few microseconds. Each chip which has at least one hit announces his address and the addresses of X and Y coordinates to be read. For high speed operation shift registers can be added to each row and column in order to pipeline data for successive events. Finally, also the readout of analog information can easily be incorporated in this architecture

5. Plan for development of interconnections and packaging.

5.1 Industrial bump bonding techniques

In the development of hybrid pixel devices the interconnection technique is a critical point, because practically no experience exists with such techniques applied to particle detectors. Preliminary discussions have been conducted with the Tape Automated Bonding (TAB) department of EM Microelectronic-Marin SA in Neuchatel, with the Centre for Manufacturing Technology CFT of Philips in Eindhoven, with the Allen Clark Research Centre of Plessey Research, Caswell and with Thomson TMS in Grenoble, who commercializes an indium bump process developed by LETI. Several more European companies may also have an experimental bump bonding process, because this is becoming the interconnect technology of choice for flat screen displays. In the USA the technology has been developed mainly for military applications in sensors, and Hughes Aircraft Co. is working on a hybrid silicon pixel device, in the framework of an SSC development contract [23].

The techniques presently considered are quite different from one another. The simplest and oldest 'flip-chip' connection scheme is the solder bump technique, which has been developed originally by IBM [27]. **Plessey** is capable of depositing solder bumps on 10 µm diameter wettable pads on a 50 µm pitch [28]. Special barrier layers have to be deposited electrochemically on the readout wafers as well as on the detector wafers, and the solder is deposited on one side only. After cutting, chips are roughly aligned on a special double-sided tool and fine aligned by the surface tension of the molten bumps, after heating. Precision is a few µm. An illustration of the LETI solder bump process is given in fig.6, which also shows the first results obtained in the Centre de Physique des Particules de Marseille (see below).

For TAB-like techniques, as employed by **EM-Marin** and **Philips,** straight wall gold bumps are grown electrolytically on the electronics chips on selected pads, while the rest of the area is covered by a thick polyimide photoresist layer [29]. The thickness of the gold bumps is ≈25 µm. Although 60 µm pads at 100 µm pitch are preferred, 30 µm pads at 50 µm pitch are also possible. After cutting the electronics chip and the detector chip are aligned on a special tool and connected by thermocompression.

The previously mentioned techniques all need a relatively high temperature at the moment of compression. The indium bump technique at **Thomson/LETI** has been developed primarily in view of the thermal constraints imposed by a several infra-red sensitive materials, and contacts can be obtained by compression only. The other characteristics of this process are very much like the solder bump or gold bump techniques.

An example of bump-bonded detector chips (consisting in this picture of IR sensitive Cadmium-Mercuric-Telluride) is shown in fig.7. Detectors are placed only on good readout chips, after the electronics wafer has been tested on a wafer probe station. The height of the metal bumps is often several tens of µm in order to accomodate lateral shifts occurring if the thermal expansion coefficients of chip and detector are different. In our case of Si-Si connection the thermal expansion does not play an important role, and in principle somewhat thinner bumps might be used.

We intend to make a first prototype interconnected hybrid with two different companies. We will provide readout wafers and detector wafers. As a function of the test results we then can determine with which of these companies a further development can be undertaken.

5.2 Laboratory scale interconnect techniques

In parallel with these industrially oriented techniques, which are currently still relatively immature and expensive, we are developing a laboratory scale approach for quick hybridization of small arrays (100 pixels) at the C.P.P.M. (Centre de Physique des Particules de Marseille). This should allow us to characterize samples of the new DRO circuits well before the industrial bump bonding has been executed, with flexible and fast feedback at significantly lower cost. The procedure will make use of point-by-point glue deposition by stamping and subsequent solder ball deposition. A micropositioning table and manipulators have been installed and the first trials have been done. Drops of conductive epoxy have been laid on a matrix of 50 µm x 50 µm pads, on which tiny solder balls provided by Extramet, SMD soldering technology, are then positioned. An illustration is shown in fig.6.

A second approach uses multilayer stamping of B-stageable epoxies. The epoxy dries but does not cure until the short heating at the time of the bonding step itself. The problem with

this method is to achieve glue dots of uniform thickness over a large area and thick enough to provide contacts on all pads. The advantage is to avoid the highly complicated task of manipulating the tiny solder balls.

Although all these methods can be to some extent automated, they are not amenable to large production as is the case for the lithographic methods discussed before.

Specialized equipment is commercially available for the alignment of the detector and readout chips, and this is used by the industrial manufacturers. This equipment is quite expensive, and for the lab-scale tests in the C.P.P.M. a simplified, but µm accuracy system has been designed which allows alignment of both chips with 6 degrees of freedom, using stepping motor driven micromanipulators. We hope to acquire a split-prism viewer, which allows to see both chips to be aligned from in-between.

6. Plan for monolithic pixel detector development.

Since 1985 several groups have been working on the adaptation of standard CMOS processing for high resistivity substrates as used for silicon detectors. The effort undertaken at IMEC, in collaboration with CERN, has resulted in the HRCMOS3 process which allows the construction of n-channel transistors in a deep p-well and also p-channel transistors directly in the lowly doped substrate [6]. Several circuits have already been built in this process and more detailed results will be available in the thesis of G. Vanstraelen.

A notable effort has been going on at Lawrence Berkeley Laboratory, and this has recently resulted in the first integrated front-end amplifier, which showed quite acceptable noise performance[30].

Other groups are at work in Munich[31] and at Stanford[32], each with a different approach aiming at a modified CMOS process directly on the high-resistivity wafer.

We want to redirect our line of development of a monolithic device towards the very promising and radiation-hard Silicon - on - Insulator (SOI) technology. This structure will eventually combine standard rad-hard CMOS electronics with customized sensor structures, separated by an intermediate oxide layer. Such a structure resembles a hybrid device, while being essentially monolithic, with the advantages of small input capacitance and ease of mechanical mounting. The SOI layer has to be fabricated on a high resistivity silicon detector substrate and the first tests are currently in progress at IMEC and LETI under sponsorship of INFN/Pisa. Because IMEC has a 125 mm standard processing line the limited availability of Si wafers is a handicap.

The IMEC activities will proceed in two phases: the feasibility study of **phase I** will decide on the most appropriate SOI production method: SIMOX (separation by implantation of oxygen), laser recristallization of a deposited silicon top-layer or strip-heater recristallization. Not considered for this moment is waferbonding, because it is still regarded to be insufficiently mature. It would present the advantage of low temperature processing, and in the future may become a more attractive choice. Detector diodes and other test structures will be used for evaluation of these various SOI processes. The quality of the high resistivity material will be measured and special attention will be given to sidewards leakage of the diodes. Phase I may be finished after 6-9 months.

In phase II, which will be executed in 12-18 months following a positive outcome of phase I, the recently developed proprietory IMEC 3 µm SOI-CMOS process will be executed on the high resistivity material. Some modifications and additional processing steps will have to be included for this special material. It is essential to have 125 mm diameter wafers for this work in order to guarantee a quick turnaround time. Besides the regular test structures one may include in the mask design also some analog and digital CMOS building blocks as well as particle detector diodes.

7. Plans for testing of experimental devices.

7.1 Laboratory testing

The design of the experimental devices includes one row of pixel cells which can be electrically stimulated via a built-in capacitor. This allows to verify the signal processing properties of the circuit, threshold uniformity, etc. [4]. The first stages of testing proceed in the laboratory, using a wafer probe station or simple mountings, as shown in [4]. Laser or ionizing radiation testing can be performed even with a regular microstrip detector, by just placing the detector chip beside the readout and connecting it via ultrasonic wire bonds. To check simple particle response a 3.5 MeV electron source like ^{106}Ru is sufficient. The noise performance can be determined in absolute scale by using gamma ray sources like ^{109}Cd, ^{241}Am or ^{57}Co with respective energies 22.2 keV, 59.5 keV and 122 keV.

Several participating laboratories have acquired equipment and experience in such testing, both for detectors and for electronic chips. In Milano I-V and C-V measurements can be performed on a wafer probe station and various other tests can be performed there. In Pisa extensive test equipment is available, although presently heavily used for the Aleph work. At the CPPM (Marseille) a complete probe test station is being set up for evaluation of wafers, hybridized chips or prototype subsystems. This setup includes a pulsed solid-state laser irradiation bench and a data acquisition system. With this facility it will be possible to perform high precision localization measurements. The red wavelenth of a GaAs solid-state laser is effective in creating e-h pairs in a well-known superficial layer, inducing a localized amount of signal charge. Moreover, it is very easy to modulate the light of such a laser, as opposed to the regular HeNe gas laser. This can be done at a rate of 10 MHz, comparable to the frequency used for testing the experimental DRO chip. The collimated beam (about 2 mm in diameter) of the laser can be focused using the camera eyepiece input of the microscope in the set up. A spot of 20 µm diameter is easily obtained and work is going on to reduce the size further to 5 or 10 µm without too much halo. For the test devices described earlier [4], a full DAQ chain has been set up at the CPPM, allowing e.g. histogramming of data from scanning strip detectors. In the following DRO chip a small (5 µm x 5 µm) photodiode will be implanted for testing the preamplifier input. This will allow to evaluate and select chips by laser irradiation before bonding of a high-resistivity detector. This setup, coupled to a computerized x-y table, allows precise position resolution measurements, cross talk investigation, gain and threshold dispersion evaluation,etc...

7.2 Beam testing

The testing of geometrical precision, detection efficiency and realistic readout schemes need a more elaborate **testbeam setup**. A requirement is high beam intensity, > 10^5 per burst, and sufficiently high energy in order to not be limited by multiple scattering in the relatively massive prototype detectors: at least 100 GeV hadrons or muons. In view of the short radiation length of the devices it seems possible to perform beam tests parasitically, e.g. upstream of a secondary target, like e.g. in the H3 beam or directly in a beam like H1.

7.3 Testing in an Omega heavy ion experiment

Technical tests of a small prototype can be performed during 1991-92. The minimal approach for the readout will be a complete scan of all pixels after an external trigger has been received. More evolved solutions are under study, as has been pointed out in sect.4.. For the 1994 running period the experiment would like to install a more complete coverage, using state-of-the-art experimental detectors. In the ideal case one needs 5 planes of 2.5 cm x 5 cm for the measurement of particle spectra. A setup of 4 planes of 2 cm x 2 cm can be considered as an intermediate step but is less attractive. These tests should allow to obtain operational experience with the devices in the short term. The cost relative to the production of the devices over and above the unique development prototypes must be covered from the budget of an approved heavy ion experiment.

7.4 Testing in DELPHI

With high luminosity at the Z^o peak, the LEP machine will be essentially a B-meson factory. Possibility of deeper study of the B-meson properties (rare decays, lifetime separation of various kinds of B, asymmetry in decays, etc...) and of reaching interesting challenges (B_s oscillations, etc...) are proposed in the DELPHI experiment [33]. Then, unambiguous track-vertex assignment and precise localization is needed for the different vertices observed in the B production and decay.

Currently, in the DELPHI experiment, there are already operational two layers (at 9 and 11 cm from the beam) of single-sided strip silicon detectors [34]. A third layer at 6.5 cm is planned for data taking in 1991 but it is foreseen to be replaced by double-sided strip detectors in 1992. However, pixels of size less than 50 μm, if possible at least for one dimension, would be interesting.

At high energy (2 x 95 GeV) in LEP, event multiplicity and synchrotron radiation induced background will increase the ambiguities. Moreover, at that time, in 1993-94, a still smaller beampipe of radius 4 cm is planned which allows to install another new layer of silicon detectors at 4.5 cm. The small area of the pixel elements and the enhanced signal/noise ratio allow to cope with the expected increase of radiation damage.

In other respects, the increase of the LEP luminosity through higher beam current and more bunches will require a high speed readout. The circuit to be proposed for DELPHI should include a fast sparse data scan in order to read only the pixels hit.

The layout of a pixel layer in the DELPHI microvertex detector can be similar to the one of the strip layers. An illustration is shown in fig.8. A composite pixel detector element can be of about the same length as the present strip detector unit, i.e. 58 mm, by bonding e.g. 5 electronic chips on a single detector substrate. Four such detector elements can then be glued on a carbon fiber support to make one ladder as it is done in the present detector. At the edge of the ladders thin ceramic supports can be glued to mount the ladders on a high precision aluminum end ring which contains also the cooling for the electronics.

8. Summary of the proposal.

The use of smart silicon pixel or 'micropattern' detectors will be essential for tracking and vertex reconstruction in high luminosity experiments, in particular at the Large Hadron Collider. The characteristics of the existing experimental devices and the extensions needed for future detectors have been described. Short references have been made to the work already performed by the institutes participating in this proposal. Basic circuit development has proceeded in the EPFL/CERN collaboration [4,20,21], readout study has been made at the Collège de France, technology development and study of readout organization have been performed at IMEC [8,9,10,11], prototype detector manufacturing and testing has been done by the Bologna/Modena/Milano group, participants of both Delphi and Aleph silicon microvertex detectors have operational experience with collider detectors, and the CPPM has been producing the first results of bumping interconnect technology.

The plans for the development work have been described: in chapter 4 for the circuit design, in chapter 5 for the hybrid interconnect technology and in chapter 6 for the monolithic integration. The development will proceed in several stages and testing in real experiments will verify the functionality of devices along the way. The testing is described in chapter 7.

9. Timescale and budget.

A budget for the period until end 1991 and an estimate for 1992 is presented in Table 3. For comparison it should be mentioned that expenditure in 1990 for the pixel detector development amounted to 240 kSF, divided between CERN, 100 kSF, and the other laboratories, 140 kSF. The contribution asked from CERN for the activities at CERN during 1991 is 175 kSF. Contributions for the French laboratories are subject to approval by IN2P3 and may require prior approval by the DRDC. The activities of the Italian laboratories in the framework of this project are to be understood as independently undertaken, but coordinated with the other participants. The SOI development in IMEC will be financed for 2/3 by internal funding.

The planning includes an engineering production run in 3 µm CMOS in the first half of 1991, followed by the first bump-bonding trials. Testing of bumped devices could take place in the Autumn of 1991. A second manufacturing run is planned late in 1991, and the advanced rad-tolerant processing should proceed afterwards. Depending on the results, a similar program of manufacturing runs can be foreseen for 1992.

Some experimental devices for use in the Omega vertex detector setup may be available in September 1991, provided the first run has proceeded without problems. A more specific device could then be produced in the second manufacturing run by the end of 1991. If problems are encountered, this date will shift by roughly a half year.

It should be noted that this proposal is concerned with the efforts needed for the development work on new prototype devices only Specific cost related to the actual implementation of pixel detectors in the intermediate 'stepping stone' experiments will have to be covered by these experiments themselves.

Table 3 Budget estimates (kSF)

activity	1991	1992
circuit design and verification	30	30
test circuit manufacturing	45	60
full wafer engineering run	60	70
high resistivity process development	240	250
chip testing	20	15
detector chip manufacturing	40	30
bump bonding	100	80
radiation testing	10	15
beam test	p.m.	p.m.
total	**545**	**550**

Table 4 Activities in participating institutions

institute	activity	contribution 1991 * sous reserve d'acceptation IN2P3	1992 all to be defined
CERN	design array,test	requested 175	(180)
CdF	design logic	*(40)	(40)
EPFL/SSS	design front-end	--	--
ETHZ	beam testing	50	(50)
IMEC	high resistivity technology	160	(160)
INFN Milano	detector testing, labo + beam	20	(20)
INFN Bologna	test structure manufacturing		
INFN Pisa	SOI technology,.proto testing	50	(50)
Marseille	bump bonding, proto testing	*(50)	(50)
total		**545**	**550**

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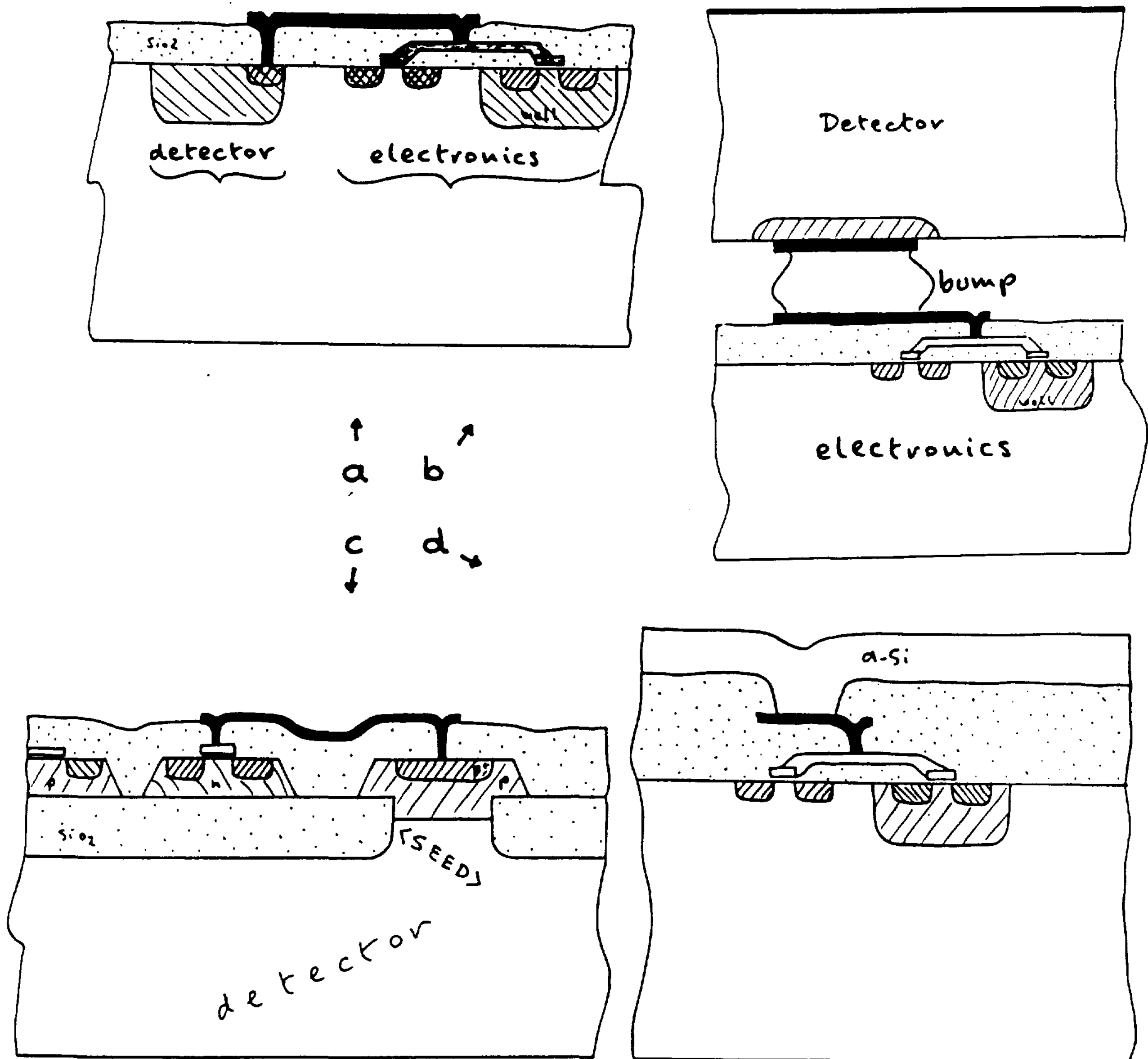
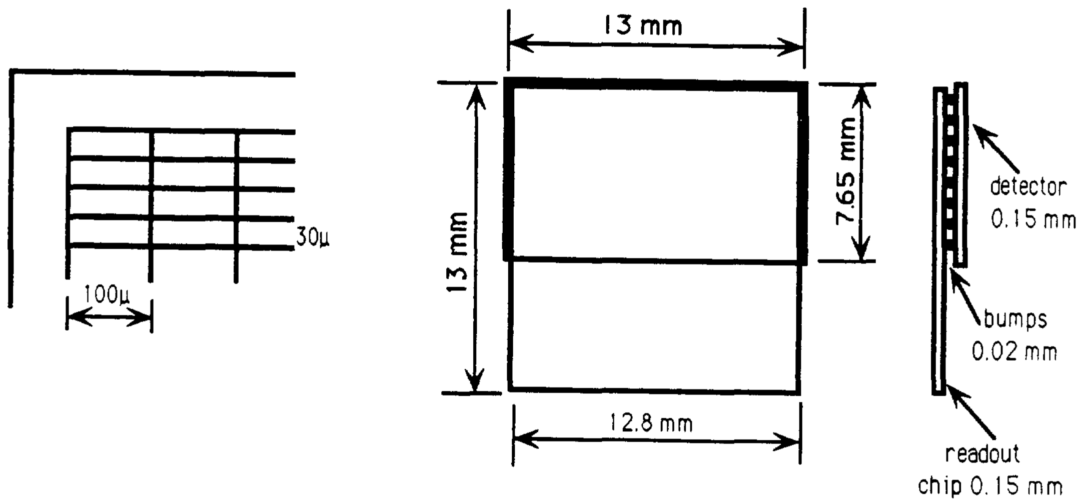


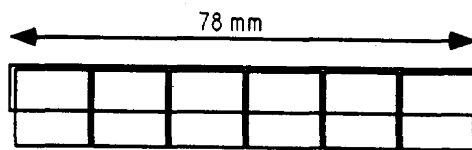
Fig.1 Cross section showing various detector-readout interconnect techniques [8]:

a) Monolithic integration of electronics within the detecor substrate
b) Hybrid integration of different chips using bump bonding
c) Monolithic integration of electronic circuits in a Silicon top layer, grown On an Insulating oxide (SOI), using seed openings. The substrate is the high-resistivity detector chip.
d) The detector layer is a thin amorphous Si layer, deposited on top of the insulating oxide, which may be useful for of highly ionizing particles or visible/ultraviolet light. The substrate is a regular Si chip, containing the readout electronic circuits.

(a) BASIC UNIT HYBRID PIXEL DETECTOR



(b) LADDER USING SINGLE 78 x 7.7 mm ^{2} DETECTOR



(c) TURBO DETECTOR

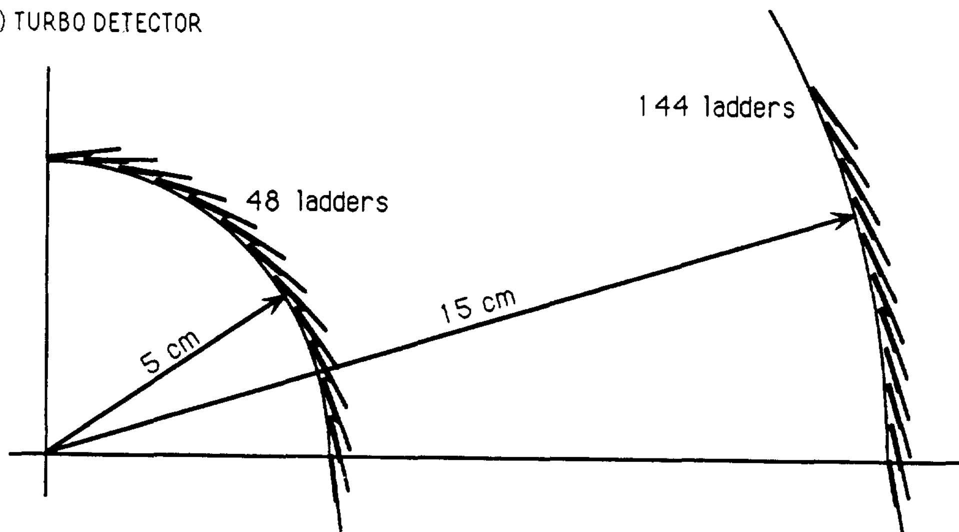


Fig.2 Sketch of pixel detector array for LHC.

a) Design of the basic unit consisting of a detector chip (left top corner) with 30 μm x 100 μm pixels. The readout chip will have to be much larger than the detector chip to accomodate the readout logic circuits, and both are connected by bump bonds (not to scale).

b) Up to 6 readout chips can be assembled on a single detector unit, cut from a 100 mm wafer.

c) Two detector barrels in the form of a 'Turbo Detector'. An inner barrel at 50 mm radius would contain 48 ladders and an outer barrel at 150 mm radius 144 ladders, with a small overlap in active area between successive detectors.

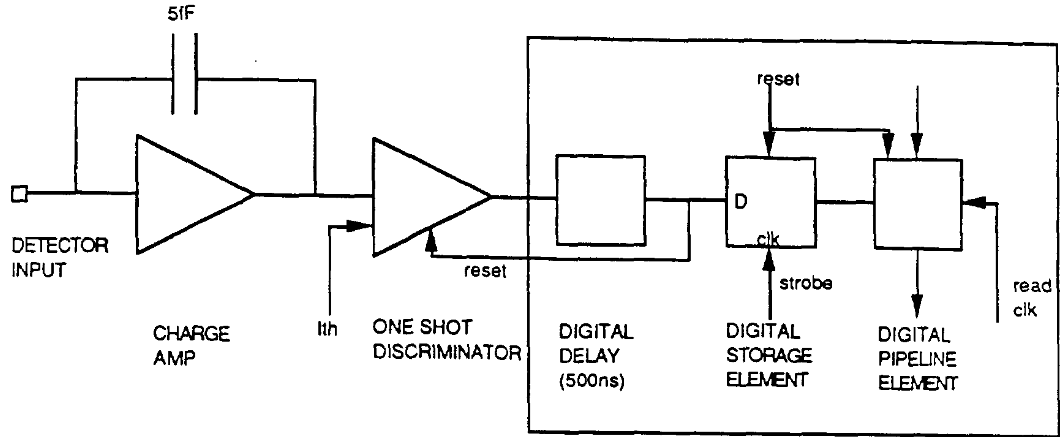


Fig.3 Block diagram of the digital pixel element for the 16x64 pixel array. The dimensions will be appr. 75µm x 300µm. The amplifier and comparator have been designed already.

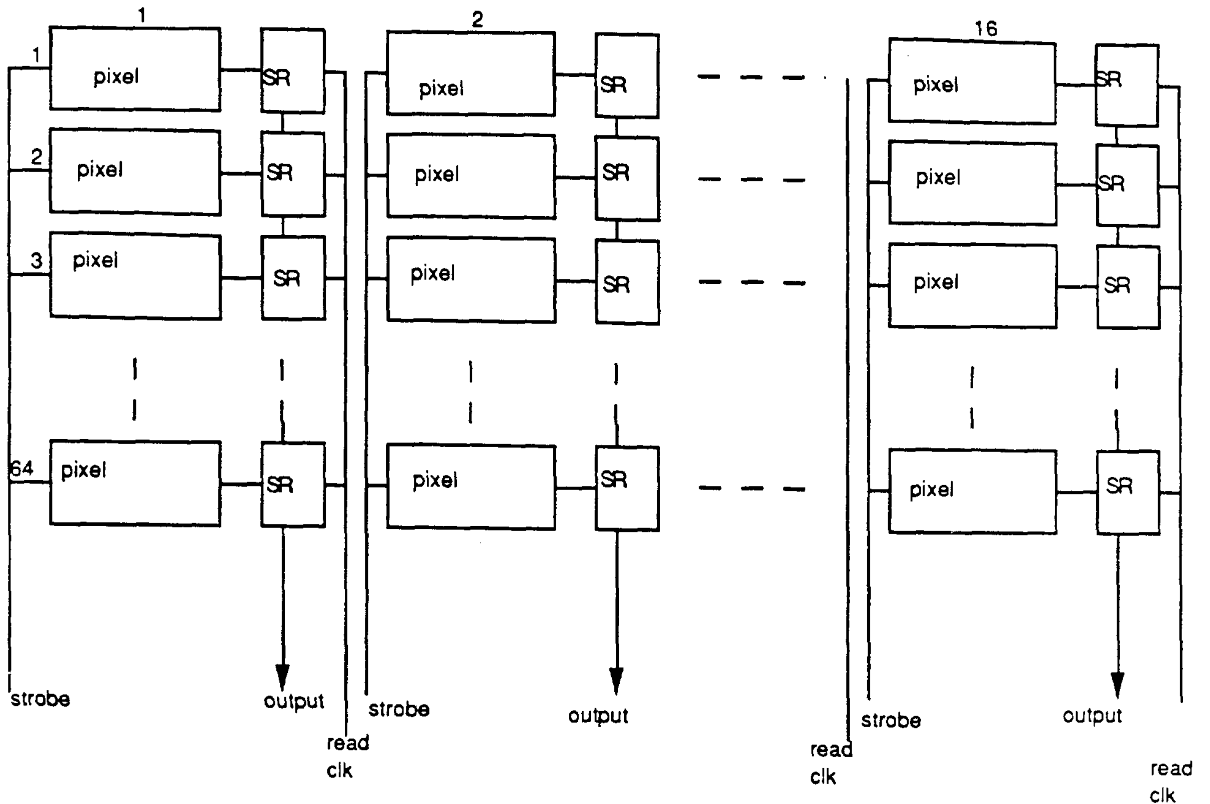


Fig.4 Block diagram of the readout of the 16x64 pixel array. 16 columns can be read out in parallel, at 5(10) MHz

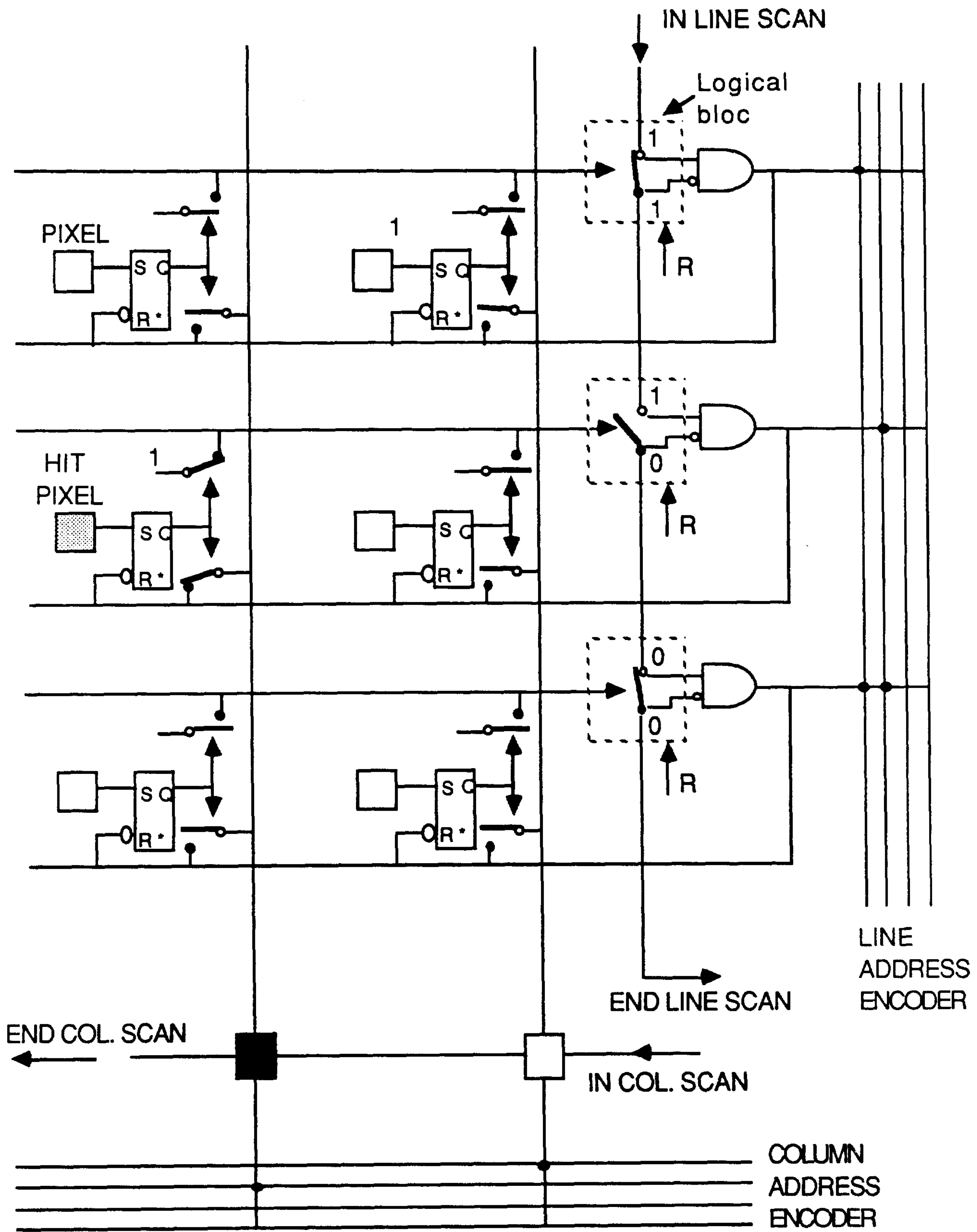
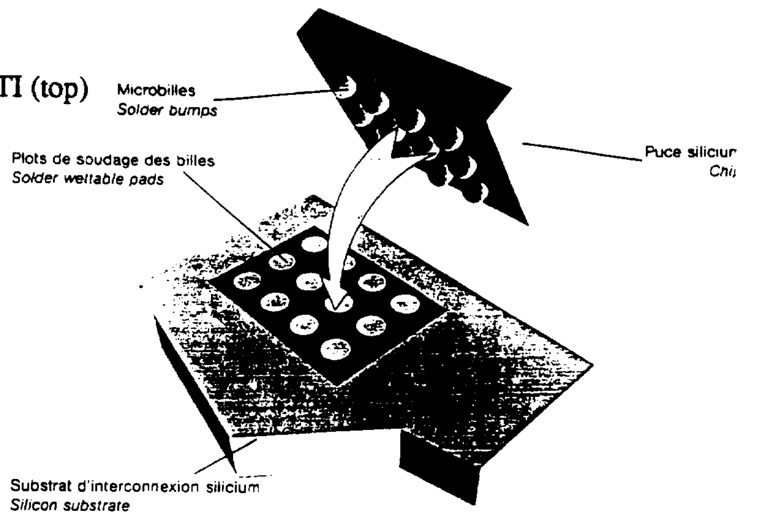


Fig.5 Schematic for two-dimensional sparse data scan

Fig.6 Solder bump process results obtained in LETI (top) and in the CPPM (bottom).



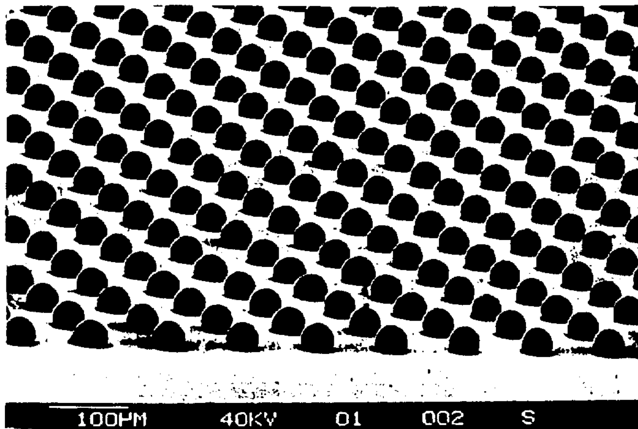
SOLDER MICROBUMPS FOR INTERCONNEXION OF DETECTOR AND ELECTRONIC CHIPS

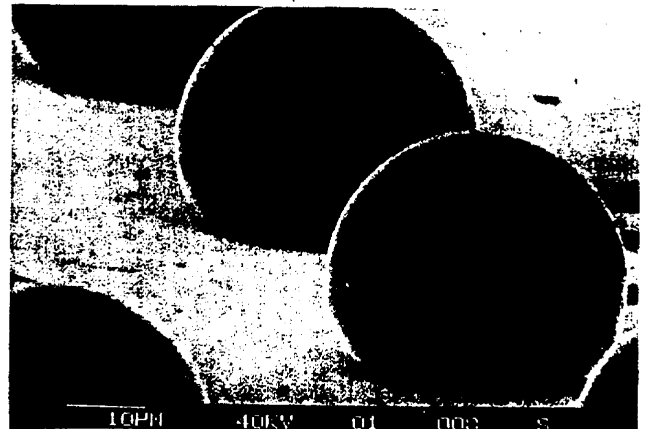
Solder bumps obtained by industrial methods

CEA COMMISSARIAT A L'ENERGIE ATOMIQUE

DIVISION LETI

INSTITUT DE RECHERCHE TECHNOLOGIQUE ET DEVELOPPEMENT INDUSTRIEL

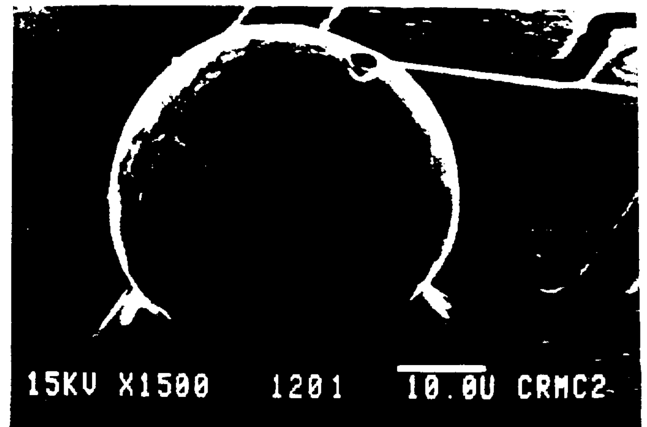




And first in-lab results ...

CNRS IN2P3 UAM II

CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE



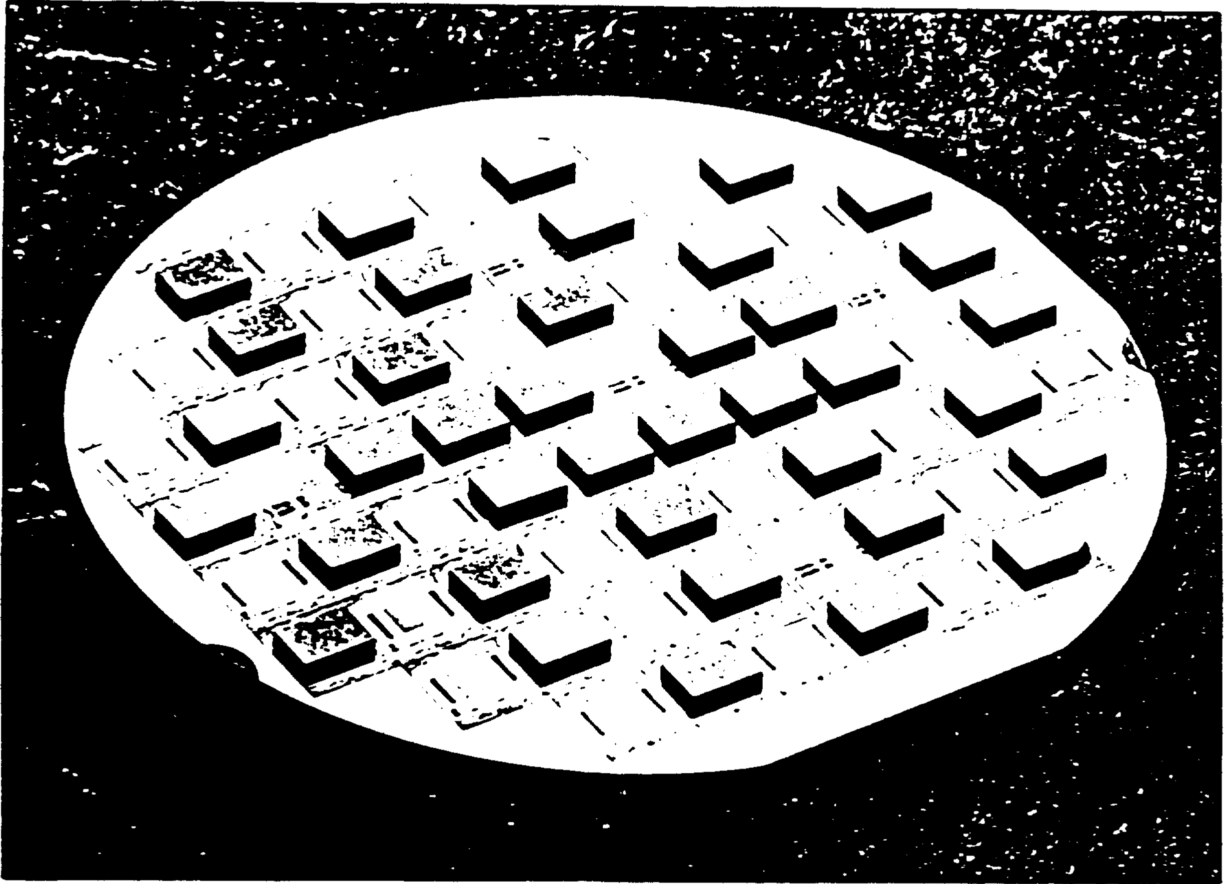


Fig.7 Individual Mercury Cadmium Telluride (MCT) detector chips for IR detection on a wafer with Direct ReadOut (DRO) circuits. Detectors are mounted on good chips only.

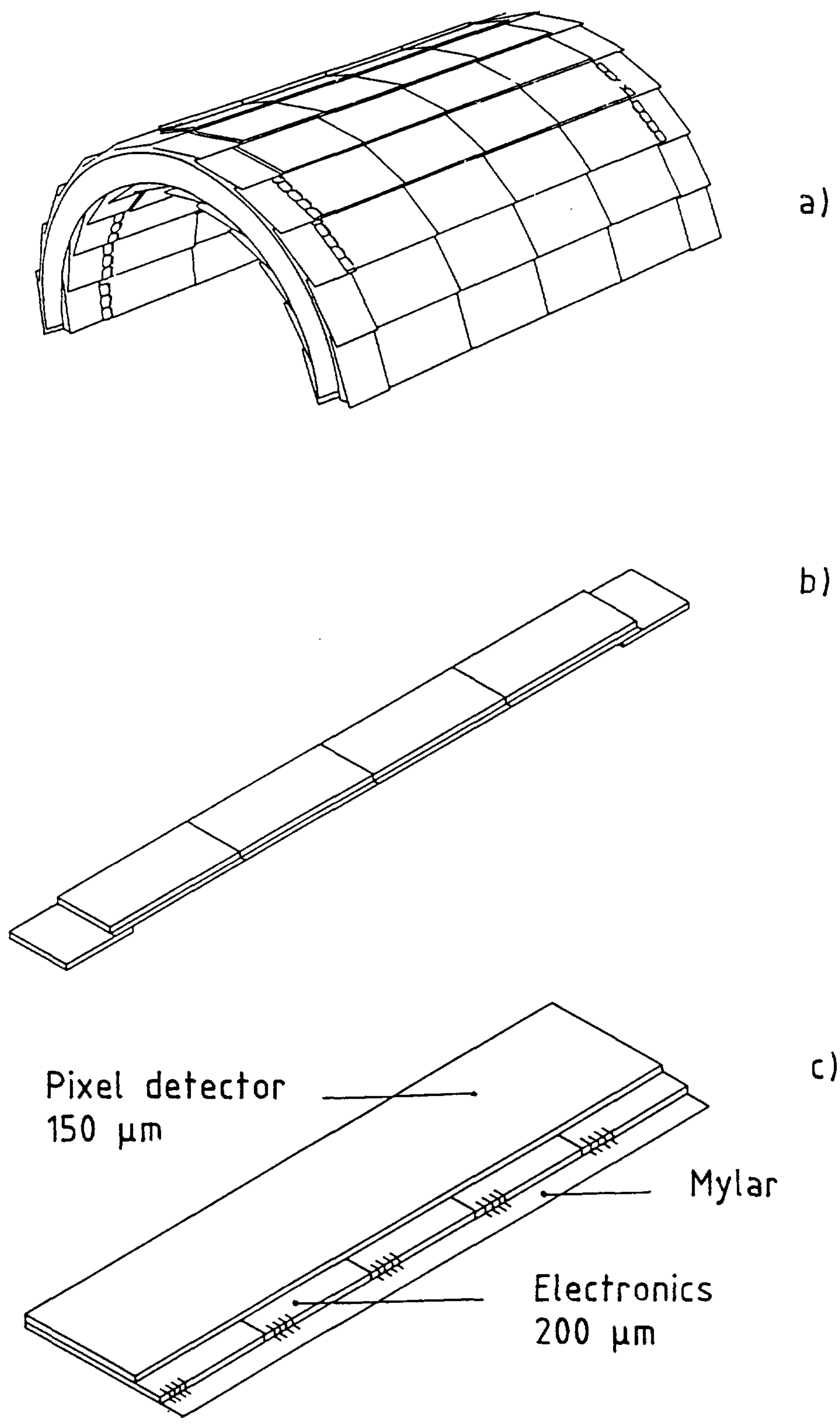


Fig.8 a) Delphi microvertex detector

b) Module of the proposed layer of pixel detector for Delphi

c) Element of pixel detector