Performance studies of the CE-65v2 MAPS prototype structure

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ABSTRACT: With the next upgrade of the ALICE inner tracking system (ITS3) as its primary focus, a set of small MAPS test structures have been developed in the 65 nm TPSCo CMOS process. The CE-65 focuses on the characterisation of the analogue charge collection properties of this technology. The latest iteration, the CE-65v2, was produced in different processes (standard, with a low-dose n-type blanket, and blanket with gap between pixels), pixel pitches (15, 18, 22.5 μ m), and pixel arrangements (square or staggered). The comparatively large pixel array size of 48×24 pixels in CE-65v2 allows the uniformity of the pixel response to be studied, among other benefits.

The CE-65v2 chip was characterised in a test beam at the CERN SPS. A first analysis showed that hit efficiencies of $\geq 99\%$ and spatial resolution better than 5 µm can be achieved for all pitches and process variants. For the standard process, thanks to larger charge sharing, even spatial resolutions below 3 µm are reached, in line with vertex detector requirements for the FCC-ee.

This contribution further investigates the data collected at the SPS test beam. Thanks to the large sensor size and efficient data collection, a large amount of statistics was collected, which allows for detailed in-pixel studies to see the efficiency and spatial resolution as a function of the hit position within the pixels. Again, different pitches and process variants are compared.

KEYWORDS: Particle tracking detectors (Solid-state detectors), instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons)

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1 Introduction

Tracking detectors are a crucial component of particle collider experiments. They detect the passage of charged particles, with the charge and momentum inferred by measuring the curvature of the reconstructed particle trajectory (*track*). The precise measurement of tracks is essential to reconstruct the locations of the particle interactions and decays: the *vertices*.

The ALICE ITS3 [1] project will replace the inner tracker of the ALICE experiment at the Large Hadron Collider (LHC) with three layers of thin, wafer-scale, bent Monolithic Active Pixel Sensors (MAPS). MAPS combine the passive sensor with the active readout chip into one silicon die. They enable a lower material budget, reduced power consumption, and smaller pitches than hybrid sensors. The sensors are manufactured in the 65 nm TPSCo CMOS process, reducing the power consumption compared to the previous generation of MAPS and enabling the construction of larger sensors given the 12-inch wafer diameter. Using the stitching technique, a handful of curved, wafer-scale sensors is sufficient to construct three cylindrical tracking layers.

The Future Circular Collider (FCC [2]) is a proposed successor to the LHC. In its first phase, the FCC-ee would collide electrons and positrons at unprecedented luminosities at centre-of-mass energies between ~90 and 365 GeV. The requirements for FCC-ee vertex detectors (VXDs) are similar to those of ITS3 but demand further development in all areas, as shown in Table 1.

Table 1: Selected design requirements of ALICE ITS3 [1] and the FCC-ee vertex detector [3].

Requirements	ALICE ITS3	FCC-ee vertex
Sensor spatial resolution	5 μm	3 μm
Material budget per layer [% of X_0]	0.07 %	< 0.3 %
Radiation tolerance [1MeVn _{eq} /cm ²]	$\sim 10^{13}$	Several $\sim 10^{13}$ per year
First layer radius	19 mm	$\lesssim 13.7 \text{mm}$
Power density in pixel matrix	40 mW/cm^2	$\lesssim 50 \text{ mW/cm}^2$
Particle hit density	8.5 MHz/cm^2	$O(200 \text{MHz/cm}^2)$

For the FCC-ee VXD, the first layer is envisioned to be at a radius $\lesssim 13.7$ mm and would potentially have to deal with a much larger particle hit rate while keeping the power density comparable. A jump in resolution is also foreseen going to only 3 µm sensor spatial resolution. The requirement on the material budget target in terms of % of radiation length (X_0) per layer is more relaxed, but FCC-ee VXDs would greatly profit from a material budget as low as ITS3 [4].

2 The CE-65v2 MAPS prototype structure

The CE-65 was developed in the context of ITS3 developments. The chip combines an analogue readout with a large pixel matrix. It is used to study the charge collection properties of the 65 nm process and compare three different amplification schemes [5]. The second version of the CE-65 prototype structure, the CE-65v2, was designed by IPHC Strasbourg and aims to go beyond the needs of ITS3. It aims to reach 3 μ m spatial resolution to meet the requirement of FCC-ee VXDs. The sensor features a large pixel matrix of 48 × 24 pixels read out by an analogue rolling shutter readout, where the matrix is read out row-by-row. The in-pixel circuitry consists of AC-coupled

amplifiers, DC-separated from the input stage of the readout electronics. The reverse bias is thus not limited by the power supply for the electronics [6]. The chip comes in 15 different variants, but in the following, the focus is on pixel pitches of 15 and 22.5 µm, both produced in the standard or modified with gap process with a classic, square, pixel arrangement.

In the *standard process* (STD), the depletion layer is balloon-shaped and does not extend to the pixel edges. This makes the charge collection diffusion-dominated with a large amount of charge sharing between neighbouring pixels and thus a good analogue spatial resolution [7]. This process is less radiation tolerant because it is more subject to charge trapping.

In the *modified with gap process* (GAP), the pixel structure was modified to include a deep low-dose n-type blanket below the collection electrode, with a gap at the pixel edges. This increases the lateral electric field, ensuring charge collection by drift rather than diffusion to the pixel edges. This results in faster charge collection even at the edges and better radiation tolerance. The disadvantage is that lower charge sharing leads to an inferior spatial resolution [7].

The previous characterisation campaign focused on the overall efficiency and spatial resolution at a reverse bias of 10 V [8]. In this contribution, reverse biases of 4 V are also investigated, and the performance is evaluated depending on the hit position within the pixel (in-pixel studies).

3 Testbeam setup and analysis

The CE-65v2 chip was characterised in a test beam at the CERN SPS north area facility (H6 beamline [9]). A mixed hadron beam of 120 GeV was shot through the beam telescope holding the CE-65v2 device under test (DUT), six ALPIDE reference planes, and a DPTS chip also produced in 65 nm [10] for triggering. The DUT was kept at a stable temperature of 20 °C using a chiller. The telescope resolution was evaluated using a telescope optimiser² to achieve a resolution of 2.2 μm.

Lab characterisation was performed prior to the test beam using a 55 Fe source to calibrate the sensor response [8]. The test beam data was then analysed using the Corryvreckan framework [11]. In the first step, noisy pixels were masked both on the reference and DUT planes to avoid misalignment. Next, multiple steps of telescope alignment were performed, with one hit required on every reference plane. Lastly, the DUT is aligned with the rest of the telescope. Two methods are used to reconstruct clusters of pixels in the DUT, which are used to determine the cluster position through centre-of-gravity reconstruction: The *cluster method* defines a neighbour threshold equal to the seed threshold, giving a conservative estimate of the sensor resolution. The *window method* sums up all charges around the seed in a 3×3 window (effectively using a neighbour threshold of zero) to fully benefit from charge sharing information. Finally, the telescope resolution is subtracted in quadrature to obtain the final sensor spatial resolution. More details are given in Reference [8].

4 Efficiency and resolution studies

The efficiency and spatial resolution study uses the cluster method to reconstruct the DUT hits. Seed thresholds ranging from 90 to 390 e⁻ are chosen, with the lowest threshold set equal to three times the noise RMS. The achieved global efficiencies are shown in Figs. 1a and 1b. All process,

¹The authors thank the ALICE Collaboration for providing the telescope and the associated DAQ software.

²https://mmager.web.cern.ch/telescope/tracking.html

pitch, and reverse bias combinations yield efficiencies > 99 % given sufficiently low thresholds. As expected, the STD process's efficiency decreases rapidly with increasing seed threshold. In both processes, the sensor performs better at $10\,\mathrm{V}$ reverse bias compared to $4\,\mathrm{V}$, indicating more depletion. For the STD process, the $15\,\mu\mathrm{m}$ pitch performs significantly better than the larger pitch at high thresholds. This comes from the fact that the undepleted region at the pixel boundaries (where diffusion dominates) is wider for larger pitches [8]. This effect is not present in the GAP process, and thus, the $22.5\,\mu\mathrm{m}$ pitch sensors feature a higher efficiency than their lower-pitch counterparts.

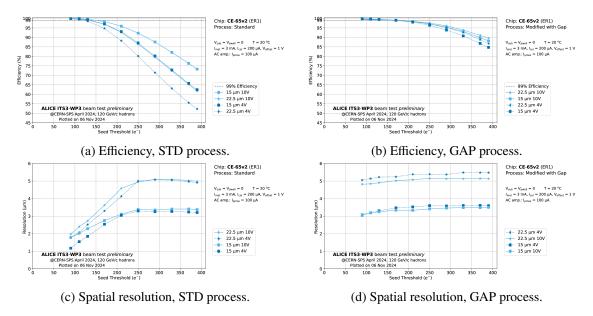


Figure 1: Efficiency (top) and spatial resolution (bottom) for different seed thresholds in the STD (left) and GAP (right) processes with pitches of 15 and 22.5 µm and at reverse biases of 4 and 10 V.

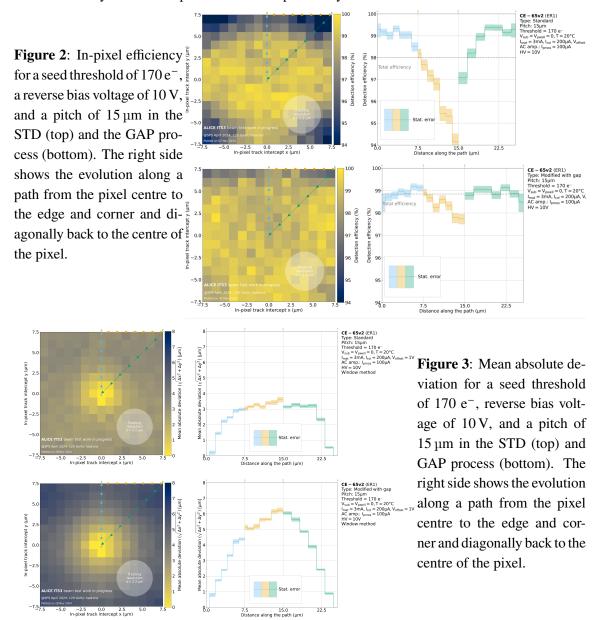
Figs. 1c and 1d show the spatial resolutions. The STD process achieves the target resolution of 3 μ m at a seed threshold of ~150 e⁻, corresponding to efficiencies of ~99% for both pitches. The GAP process does not achieve such a small resolution, but 3.5 μ m (5 μ m) can be safely achieved at reasonable thresholds of 170 e⁻ for a pitch of 15 μ m (22.5 μ m), where efficiencies are > 99 %. Comparing the reverse bias voltages, it can be seen that 4 V provides better resolution in the STD process and worse resolution in the GAP process, indicating a smaller depletion depth. In the STD process, this leads to more charge sharing and, thus, better resolution, while the GAP sensors do not benefit from this since the gap in the low-dose n-type implant inhibits charge sharing.

5 In-pixel efficiency and mean absolute deviation studies

The large pixel matrix of the CE-65 chip, and thus a large number of collected and reconstructed tracks, can be utilised to perform in-pixel studies. The hit information of every pixel (except for the two outermost rows/columns) is superimposed and analysed at a seed threshold of $170 \, e^-$. For both processes, measurements of a $15 \, \mu m$ pitch sensor at a reverse bias voltage of $10 \, V$ are used.

The *cluster* method is deployed to evaluate the in-pixel efficiencies shown in Fig. 2. In the STD process, there is a drop in performance at the edges and corners of the pixel. There, the charge is

shared between multiple pixels and thus often does not overcome the seed threshold. For the GAP process, thanks to depletion up to the pixel edges and stronger lateral fields, one can observe only a minor decrease in efficiency at the corners and an otherwise flat distribution, explaining the overall better efficiency in the GAP process observed previously.



The in-pixel measurement of the mean absolute deviation between the reconstructed telescope and DUT cluster positions $(\sqrt{\Delta x^2 + \Delta y^2})$ uses the window method. Fig. 3 shows the mean absolute deviation depending on the position of the hit inside the pixel. In the STD process, the distribution is more uniform and does not exceed $\approx 3.5 \, \mu m$ anywhere in the pixel. For the GAP sensor, the performance strongly deteriorates at the edges and corners, which leads to the overall worse spatial resolution observed before. Using the window method, the full power of the STD process is showcased: Charge sharing from the seed to the neighbouring pixels strongly helps to reconstruct the hit position and reach resolutions much below pitch/ $\sqrt{12}$.

6 Conclusions and Outlook

This work builds on previous measurements of the CE-65v2 [8] and investigates operation at reverse bias voltages of 4 V and evaluated the performance depending on the in-pixel hit position. Two different paths towards superior spatial resolution in CE-65 structures were explored. Using the STD process, resolutions < 2 μ m (< 3 μ m) are achieved with a pitch of 15 μ m (22.5 μ m), while still operating with over 99 % efficiency. The GAP process, featuring faster charge collection but less charge sharing, enables resolutions of ~3.3 μ m. A further reduction of the pitch could also allow the GAP process to fulfill the FCC-ee VXD spatial resolution requirement.

The challenges of achieving 3 µm resolution in a large digital read-out chip efficient at reasonable noise levels and in a radiation environment differ between the two processes. In STD, an intricate analogue-to-digital conversion scheme is necessary to fully benefit from the charge sharing information while keeping the readout data rate minimal. For the GAP process, the challenge is to integrate all the necessary logic into pixels of small pitch required to achieve 3 µm resolution.

The next steps in characterising the CE-65 are to measure the effect of irradiation and test 18 µm pitch sensors and the Modified without Gap process. Lastly, the impact of a staggered pixel arrangement, mimicking hexagonal pixels, is also still being evaluated.

CE-65 marks a promising step towards MAPS fit for future lepton collider vertex detectors.

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