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A SCALABLE DATA TAKING SYSTEM AT A TEST BEAM FOR LHC

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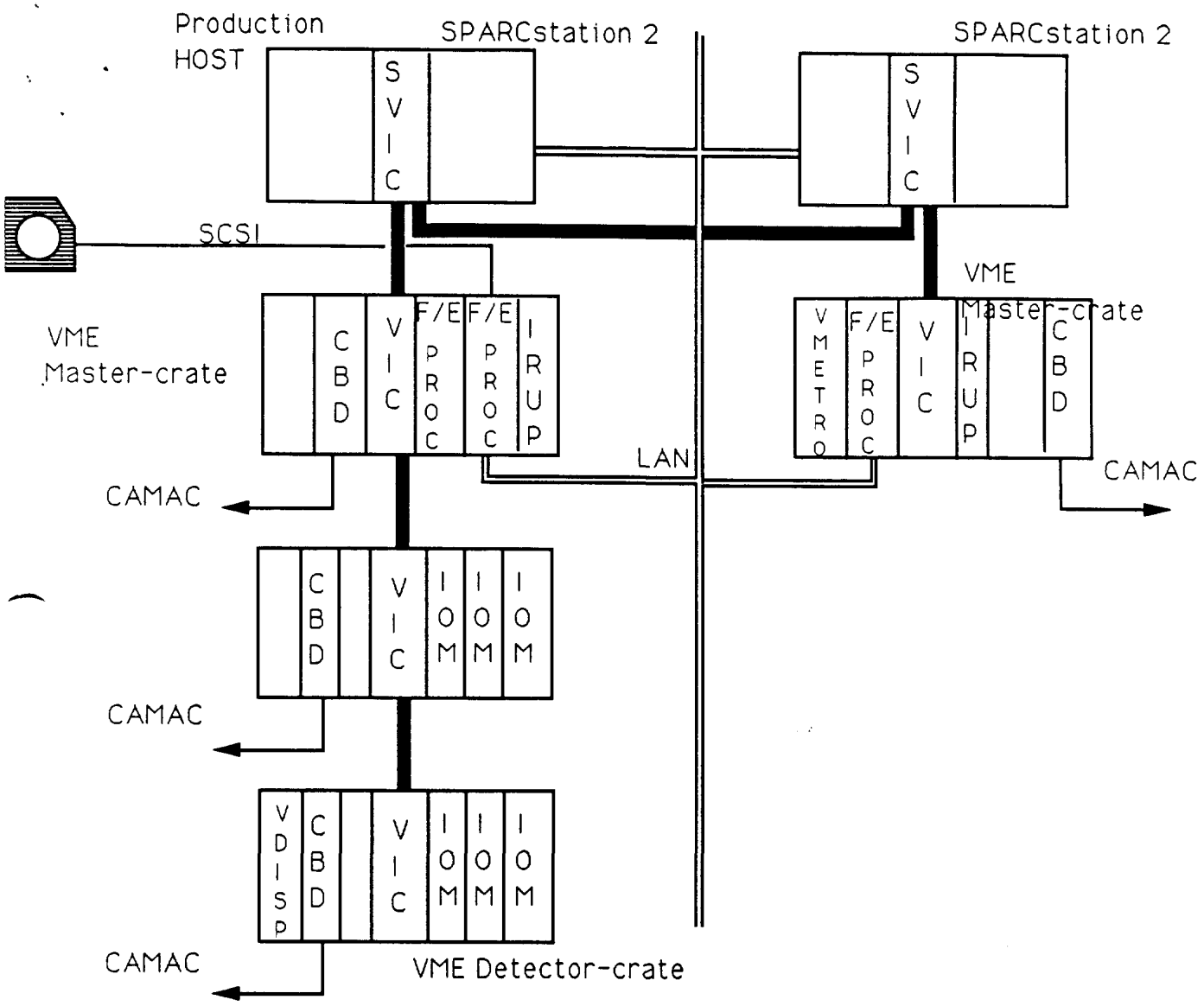
We intend to install a test beam readout facility for the simultaneous test of LHC detectors, trigger and readout electronics, together with the development of the supporting architecture in a multiprocessor environment. The aim of the project is to build a system which incorporates as fully as possible all the functionality of a complete readout chain. A strong emphasis is put on a highly modular design, such that new hardware and software developments can be conveniently introduced for training and evaluation. Exploiting the modularity, the set-up will evolve driven by progress in technologies and new software developments.

One of the main thrusts of the project will be the modelling and system integration of different readout architectures, which is meant to provide a valuable training ground for new techniques. To address these aspects in a realistic manner, we propose to collaborate with detector R+D projects in order to test higher level trigger systems, event building and high rate data transfers, once the techniques involved are sufficiently mature to be tested in data taking conditions.

The figure shows the hardware layout of the initial setup. Although at the beginning two detector R+D's (SPACAL [RD1] and SITP [RD2]) will be integrated, the system will be designed with a strong scalability accent, in the number of data sources, processing power and monitoring and control features. The possibility of driving all the processors (front and back end) with a unique operating system type will be a major issue of study for the initial phase of the project. To this extent a Real Time version of UNIX will be tried in the front end RISC processors.

The complexity expected for the software online system of a LHC experiments imposes the use of non-traditional (within HEP) software development techniques. Therefore, the problems of data acquisition and support software will be addressed by the exploitation of modern software engineering and programming languages tools.

Finally, such a system will be designed with the necessary openness to allow the integration of trigger and DAQ sub-systems, which are or will be the object of independent studies. In particular, studies of event building techniques will be initiated within this project and will be integrated in the system proposed as the first step of system evolution and integration test.



SVIC	VIC/Sbus interface, CES SVIC7213
VIC	VMV Master/slave interface, CES VIC8250/1
F/E PROC	MIPS3000 based processor, CES RAID8235
VDISP	Display module, CES VMDIS 8003A
VMETRO	VMETRO Display/Logic State Analyser Module
CBD	CAMAC branch driver, CES CBD8210
IRUPT	Interrup generator board, ELTEC V-IGEN-A100
IOM	Detector I/O Modules