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Quality Assurance and Quality Control of the 26 m^2 SiPM production for the DarkSide-20k dark matter experiment

The DarkSide-20k Collaboration[a,1]

[1] See back for author list

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Abstract DarkSide-20k is a novel liquid argon dark matter detector currently under construction at the Laboratori Nazionali del Gran Sasso (LNGS) of the Istituto Nazionale di Fisica Nucleare (INFN) that will push the sensitivity for Weakly Interacting Massive Particle (WIMP) detection into the neutrino fog. The core of the apparatus is a dual-phase Time Projection Chamber (TPC), filled with 50 tonnes of low radioactivity underground argon (UAr) acting as the WIMP target. NUV-HD-Cryo Silicon Photomultipliers (SiPM)s designed by Fondazione Bruno Kessler (FBK) (Povo, Trento, Italy) were selected as the photon sensors covering two 10.5 m^2 Optical Planes, one at each end of the TPC, and a total of 5 m^2 photosensitive surface for the liquid argon veto detectors. This paper describes the Quality Assurance and Quality Control (QA/QC) plan and procedures accompanying the production of FBK NUV-HD-Cryo SiPM wafers manufactured by LFoundry s.r.l. (Avezzano, AQ, Italy). SiPM characteristics are measured at 77 K at the wafer level with a custom-designed probe station. As of May 2024, 603 of the 1400 production wafers (43% of the total) for DarkSide-20k were tested, including wafers from all 57 production Lots. The wafer yield is $93.6 \pm 2.5\%$, which exceeds the 80% specification defined in the original DarkSide-20k production plan.

1 Introduction

Silicon Photomultipliers (SiPMs) have emerged as a compelling photosensor solution for detecting single photons in applications ranging from particle physics to medical imaging and beyond [1]. SiPMs consist of an array of tightly packaged Single Photon Avalanche Diodes (SPADs) operated above the breakdown voltage, V_{bd}, so that they generate self sustaining charge avalanches upon absorbing an incident photon [2]. In contrast to the widely used Photo- multiplier Tubes (PMTs), SiPMs are low-voltage powered, insensitive to magnetic field, and have a compact and flat form factor [3]. For these reasons, SiPMs are the adopted solution in the MEG-II and DUNE experiments [4,5]. In addition, SiPMs have very low residual natural radioactivity, making them especially appealing for low-background experiments such as nEXO and DarkSide-20k [6,7].

DarkSide-20k (DS-20k) is a multi-tonne dark matter detector under construction at the Laboratori Nazionali del Gran Sasso (LNGS) of the Istituto Nazionale di Fisica Nucleare (INFN) that will push the sensitivity for Weakly Interacting Massive Particles (WIMP) detection to the level where solar and atmospheric neutrinos become a significant background. The core of the DS-20k apparatus is a dual-phase Time Projection Chamber (TPC), with a vertical electron drift. The TPC is a 348 cm tall octagonal prism with a 350 cm inner diameter containing the liquid argon (LAr) dark matter target: 50 tonnes of underground argon (UAr) (20 t fiducial volume) [8].

Electron extraction in gas is provided by a stainless steel grid made with 200 μm wires, with a pitch of 3 mm. The gas pocket thickness is expected to be 7 mm. The top and bottom lids of the octagon are made in pure acrylic, and their inner planes are coated with a thin conductive layer of PEDOT:PSS (Clevios™) and tetraphenyl butadiene (TPB) to shift LAr scintillation light from 128 nm to visible light [9]. The conductive layers allow biasing the inner planes of the two lids, such that they act as cathode and anode. The barrel pieces of the octagon are machined and coated with Clevios™ to define a geometry of conductive rings (field cage) connected by resistors and biased to define a uniform and stable electric drift field of 200 V/cm.

[a] *corresponding authors: ds-ed@lists.infn.it

The scintillation light emitted in the TPC is detected by two 10.5 m^2 Optical Planes (OP) instrumented with Fondazione Bruno Kessler (FBK) NUV-HD (near-UV sensitive, high-density) SiPMs located at the top and bottom of the octagonal barrel and used to optically readout the argon scintillation (S1) and electroluminescence (S2) signals in the liquid and gas phase, respectively [10, 11].

A stainless steel vessel filled with an additional 36 tonnes of UAr surrounds the TPC. The stainless steel vessel is itself immersed in further 650 tonnes of atmospheric liquid argon (AAr), contained within a DUNE-like membrane cryostat. Both argon volumes are outfitted with SiPMs and will serve as the experiment's Inner Veto (IV) and Outer Veto (OV) detectors [12].

The inner detector employs the TPC and IV detectors to mitigate the most critical background for dark matter searches, which comes from neutron scattering, while the OV is used to detect and tag external neutrons and muons.

The FBK NUV-HD SiPM technology was introduced by FBK in 2016 [13]. The first generation of these devices suffered from a high Dark Count Rate (DCR) and large afterpulsing probability incompatible with the DS-20k specification [7]. A specific process modification was developed by FBK to address the DS-20k requirements [14]. This led to a variant of the FBK NUV-HD technology named FBK NUV-HD LF (Low Field) that features an almost three-orders of magnitude reduction of the SiPM DCR at 80 K when compared to the standard NUV-HD version, comfortably lower than the DS-20k specification.

Further optimization of this technology allowed for a reduced SiPM afterpulsing probability (NUV-HD LF low AP technology) and quenching resistance, thus optimizing the microcell recharge time constant at cryogenic temperature. These two process adjustments led to the development of a new technology called FBK NUV-HD Cryo, presented in Ref. [15], that not only met but exceeded the DS-20k specifications.

In the final DS-20k photodetector design 24 FBK NUV-HD-Cryo SiPMs are aggregated together to form objects known as tiles, with six (three) parallel branches of four (two) SiPMs in series fed into a single transimpedance amplifier (TIA) or a custom designed ASIC amplifier [16, 17], used to instrument the TPC and Veto detectors [18]. The 24 SiPMs are bonded to an Arlon low-radioactive Printed Circuit Board (PCB) [19].

Tiles, in groups of four, are further aggregated in a quadrant: a single analog readout element [20]. Four quadrants are then aggregated into a single object with a total surface area of 400 cm^2. These devices are called Photo Detector Units (PDUs) and constitute the basic element of the DS-20k photoelectronic system. An example is shown in Fig. 1. In total, 680 PDUs are needed to instrument the two TPC optical planes and the IV and OV detectors (528 TPC, 152 IV and OV), which will make DS-20k the largest SiPM-based cryogenic detector, with more than 260,000 SiPMs.

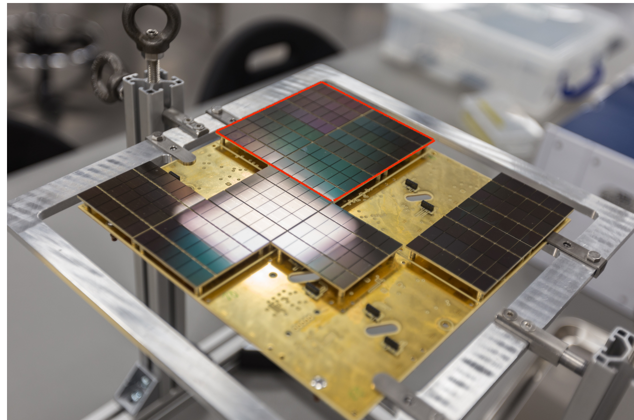

Fig. 1 Tiles prototype partially assembled into a Photo Detector Units (PDU). Each tile consists of 24 FBK NUV-HD-Cryo SiPMs with six (three) parallel branches of four (two) SiPMs in series fed into a single transimpedance amplifier (TIA) or a custom designed ASIC amplifier. Tiles, in groups of four, are further aggregated in quadrants. Only one quadrant, shown in red in the figure, is fully populated. Each quadrant is read out as an individual analog readout channel.

This paper focuses on the Quality Assurance and Quality Control (QA/QC) of the FBK NUV-HD-Cryo SiPM production wafers manufactured by LFoundry s.r.l. (Avezzano, AQ, Italy), an Italian semiconductor company with the infrastructure to produce a large number of devices for DS-20k [21].

Wafers manufactured by LFoundry are stored, tested and diced in the Nuova Officina Assergi (NOA) facility, a new ISO-6 353 m^2 clean room packaging facility constructed at INFN LNGS [22, 23, 24]. NOA houses state-of-the-art production machines for packaging silicon sensors such as the ones used in DS-20k, and it is currently used for the production of the DS-20k PDUs.

Several SiPM characteristics for each wafer dice such as breakdown voltage, quenching resistance, leakage current and correlated avalanche noise, are measured with a custom-designed, cryogenic probe station at the wafer level at 77 K. As of May 2024, 603 of the 1400 production wafers (43% of the SiPM production) were tested, sampling all 57 production Lots. The average wafer yield is $93.6 \pm 2.5\%$, which exceeds the 80% production yield assumed in the original DS-20k production plan.

2 Hardware Setup

Fig. 2 shows an 8-inch FBK NUV-HD Cryo SiPM production wafers manufactured by LFoundry. Each wafer consists of 268 potentially functional dice, highlighted in yellow in the figure, with a dimension of 11.7×7.9 mm^2. The wafer in

the figure is diced and mounted on a grip ring, used in the subsequent steps of the DS-20k silicon packaging process flow. LFoundry produced wafers in 57 batches called Lots.

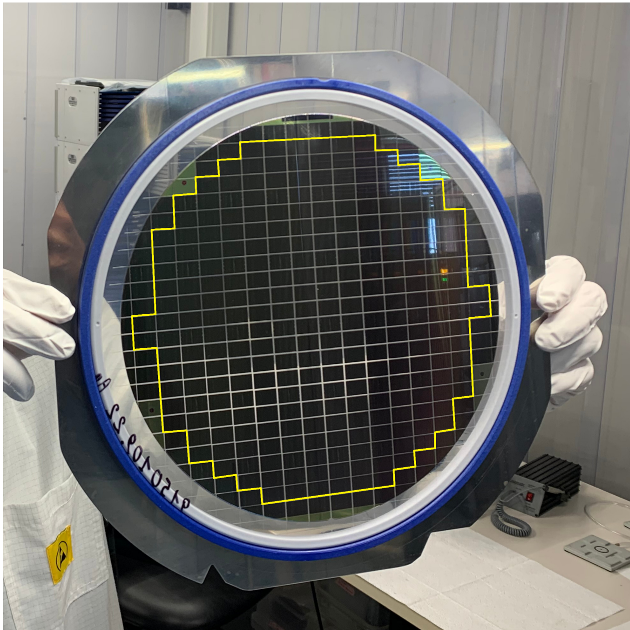

Fig. 2 Production wafer diced and mounted on a grip ring. The 268 SiPM dice are highlighted in yellow. Due to the overlapping geometry of the probe card and the wafer clamping ring, only 264 of the 268 potentially working SiPMs can be probed at 77 K.

Each of the ~ 25 wafers in a Lot travels together through the foundry process steps.

Fig. 3 Wafer cassette containing one production Lot (25 wafers). The wafer's gold backside is visible.

The largest variations in wafer performance are expected when comparing different Lots, while the wafer-to-wafer variations within the same Lot are expected to be a subdominant contribution. This is because wafers in a Lot progress through the manufacturing cycle at the same time (simultaneously or sequentially, depending on whether it's a batch or a single wafer process). For batched processes, the wafer-to-wafer variability is mainly due to each wafer's positioning in the processing equipment (*e.g.* an annealing furnace or a wet etching hood). For single-processes, the variability is due to tool variation over time.[1]

Fig 3 shows one of the production Lots. Each wafer in the Lot has a gold-coated backside that acts as the SiPM cathode. The SiPM anode contact is composed of three short-circuited aluminum pads placed on the top SiPM surface (Fig. 4). One of these three pads is used for cryoprobing (top-right pad in Fig. 4), and the other two are used to wire bond the SiPM to the tile PCB.

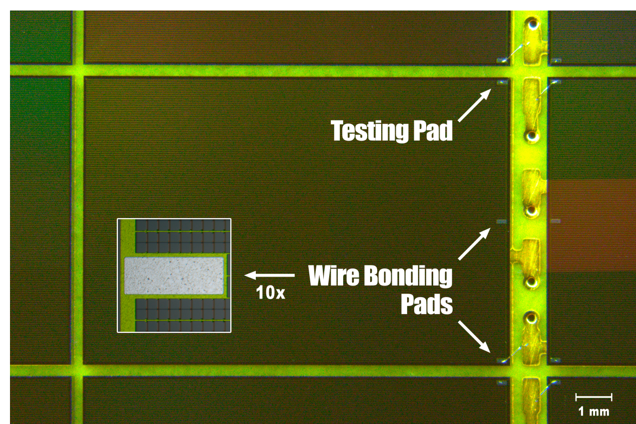

Fig. 4 FBK NUV-HD Cryo SiPM dice bonded to a DS-20k tile. The three aluminum pads are short-circuited together. One of these three pads is used for cryoprobing (top-right), while the other two are used to wire-bond the SiPMs to the corresponding tile PCB. Each dice measures $11.7\times7.9\,\text{mm}^2$.

A new testing setup (Fig. 5) was built to characterize the SiPM response at the wafer level at 77 K. It consists of a high precision, semi-automated cryogenic Cascade Form Factor PAC-200 probe system (cryoprobe) that cools the wafer to 77 K in a high vacuum environment (10^{-7} mbar) [25]. Wafers are tested with a cantilever, needle-based probe card made by htt group (Munich, Germany) [26] (Fig. 6).

For the test, wafers are mounted on a gold-plated copper carrier (Fig. 7). Due to mechanical constraints between the probe card and the wafer clamping ring used to hold the wafer in place on the carrier during measurements, 264 out of potentially functional 268 dice in each wafers can be probed with the cryoprobe[2].

[1] An additional component of wafer variability is within-wafer, or site-to-site, variation. This occurs due to process non-uniformities at the wafer scale.

[2] The 4 SiPMs per wafer not tested with the cryoprobe are not discarded, but instead used to build tiles subsequently tested to ensure compliance with the DS-20k tile specification, presented in a separate work.

Fig. 5 Form Factor PAC-200 probe system + S500 Parametric Keithley tester used to characterize the response of the FBK NUV-HD Cryo SiPMs. The entire system is located in a new ISO-6 353 m^2 clean room packaging facility called the Nuova Officina Assergi (NOA) constructed at the Istituto Nazionale di Fisica Nucleare (INFN) Laboratori Nazionali del Gran Sasso (LNGS).

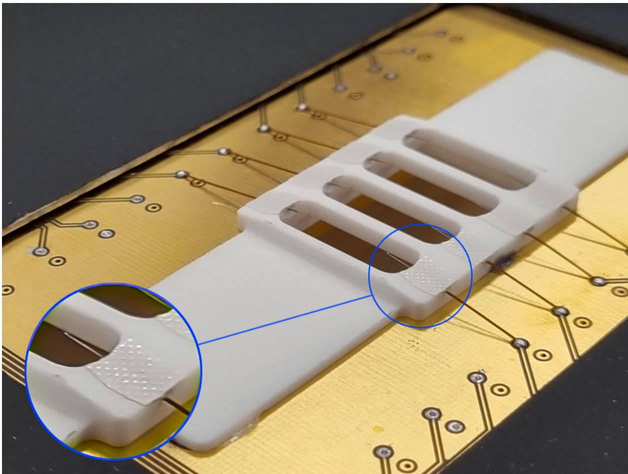

Fig. 6 Htt probe cards designed by Form Factor with 2x4 tungsten needles used for SiPM probing (1 needle per SiPM - shown enlarged in the circle). The white ceramic carrier shown in this photograph connects directly to the needles.

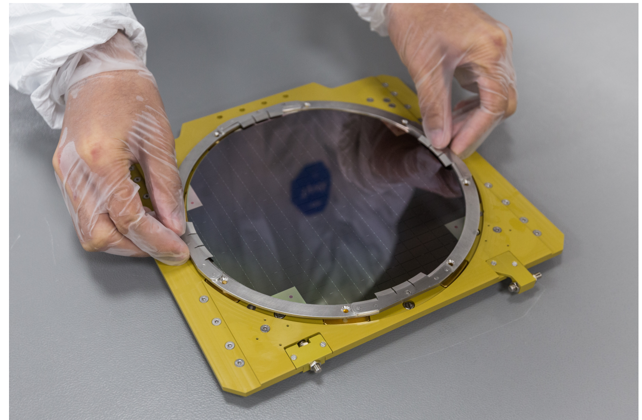

Fig. 7 Production wafer mounted on a gold-plated wafer carrier. The wafer is held in place with a custom-made clamping ring.

The wafer carrier is placed in a semi-automatic loader. The loader is evacuated and transports the wafer into the main chamber via a robot arm. The arm loads the wafer carrier on a gold-plated copper chuck that acts as a common cathode for current-voltage (IV) measurements.

A liquid nitrogen (LN2) cooling coil inside the chuck brings its temperature down to 77 K. The LN2 that flows in the coil is regulated by a needle valve placed on an LN2 transport line that is used to connect the PAC-200 probe station to an external LN2 storage Dewar. Two heater resistors maintain the chuck temperature constant to a precision of better than 0.5 K (1σ) at 77 K.

The wafer carrier makes thermal and electrical contact with the chuck through four indium pads. The probe card needles touch down on the wafer surface, contacting the SiPM aluminum pads (1 needle per SiPM). Two probe cards with 24 and 8 needles, respectively, are used to test the wafers and periodically interchanged as part of regular system maintenance. An S500 Parametric tester equipped with Keithley

2612B Source Meters Units (SMU, 1 SMU channel per needle) is used to bias the SiPMs and read their current [27]. The system noise floor (including cables, SMUs, and probe card) is around 10 pA.

The Keithley Automated Characterization Suite (ACS) software program is used in conjunction with the Form Factor PAC-200 Velox software to control the cryoprobe automatically, move the chuck from dice to dice, and execute the measurement sequence presented in Sec. 3. A MIDAS-based slow control system [28] is used to monitor the entire procedure and protect the system against human errors (*e.g.* wrong needle contact heights). Depending on the probe card configuration (*i.e.* number of needles) and the S500 measurement settings, at least 14 touchdowns are needed to test the accessible wafer surface (264 out of 268 SiPMs). The rate to probe a wafer, including the wafer loading, cooling, measurement, and unloading time, is 0.35 wafers/hour. The cryoprobe is operated 12 hours per day, 7 days per week, with an up-time of 85%, which results in a maximum wafer throughput of 25 wafers per week.

3 Experimental Details

The forward and reverse bias current-voltage (IV) curves of the testable SiPMs on a wafer (264 out of 268 SiPMs) are collected at 77 K. The cryoprobe vacuum chamber is not light-tight: there is a photon-induced rate on the order of a few kHz per SiPM. No external light source is therefore needed to create a measurable current when collecting the reverse bias IV curves. Fig 8 shows IV curves from one production wafer.

To reduce the testing time, SiPMs are measured in parallel. The maximum number of SiPMs that can be measured simultaneously depends on two factors: (i) the probe card configuration (*i.e.* the number of needles on the card) and, (ii) the resistance of the measurement system, which includes the cabling and the cryogenic chuck responsible for inducing a voltage drop and therefore lowering the measured current. This drop is negligible for reverse bias IV curves, but it is relevant for forward bias IV curves due to the large sourced current (order of mA), especially when grouping SiPMs, as shown in Fig. 9[3]. We also observe a growing instability *i.e.* larger fluctuation, in the measured current even for reverse bias IV curves, as the number of SiPMs tested in parallel increases, which is probably due to the common cathode configuration. Overall, we found that grouping 4 (8) SiPMs in parallel for forward (reverse) IV curves represents a good compromise between these effects and the testing throughput.

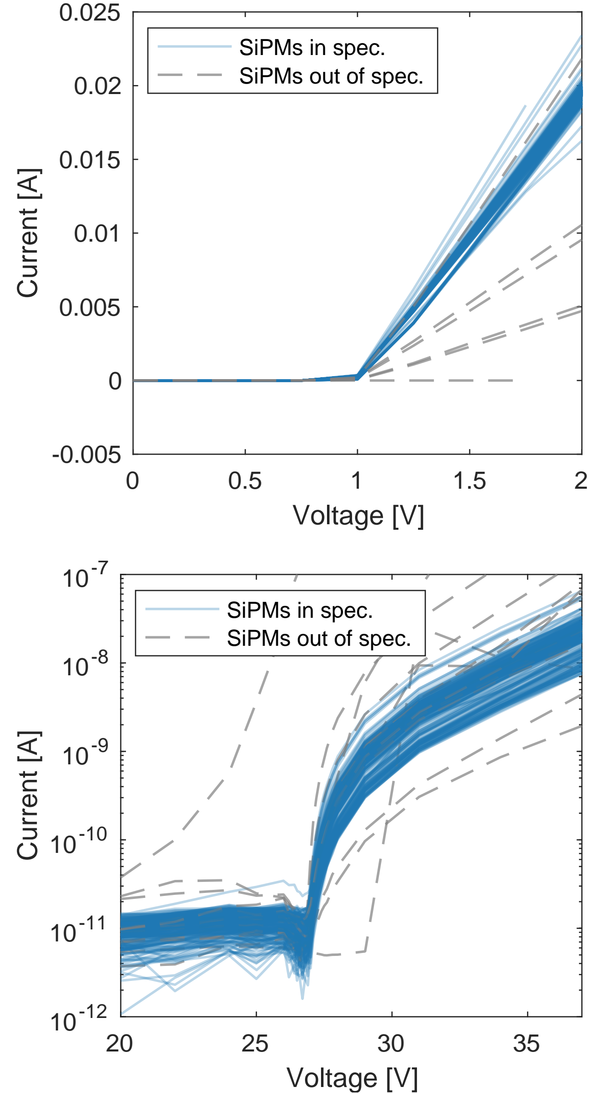

Fig. 8 Forward (top) and reverse (bottom) bias current-voltage (IV) curves for the production Wafer 19 of Lot 9306869. The dashed lines are IV curves that correspond to dice which were discarded based on the selection criteria presented in this work.

IV curves in the forward direction are measured at constant voltage increments of 0.25 V up to 2 V, which corresponds to a forward current of about 20 mA. IV curves in the reverse bias direction are measured starting from 20 V, several volts below the expected breakdown voltage at 77 K (27.2 V), up to 37 V, which corresponds to roughly 10 V of over voltage, larger than the maximum planned SiPM operating over voltage in the DS-20k detector (7 V). The voltage step is adjusted to be smaller in the range [26.4–27.6] V to obtain a more accurate extrapolation of the breakdown volt-

[3] The total system resistance is estimated to be 3.6 Ω, of which 2 Ω is due to the resistance between the chuck top surface and its hermetic bottom surface. This value was estimated by the change in slope of the forward bias IV curves when going from a single channel to a four-channel measurement, as shown in Fig. 9. The extrapolated value was also confirmed with a dedicated measurement done on the cryogenic chuck of the PAC-200 system.

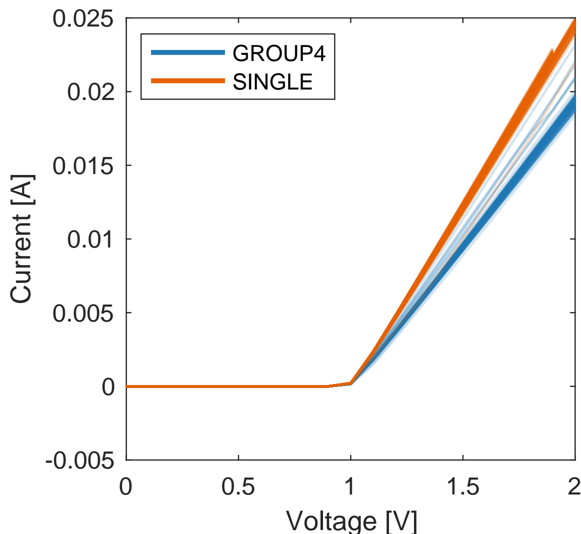

Fig. 9 Forward bias IV curves for one production wafer when simultaneously measuring 4 SiPMs in parallel versus a single SiPM.

age. The step choice is a compromise between accuracy and overall wafer testing time.

A Labview-based application, shown in Fig. 10, was developed to analyze, display, and store the data from the Keithley ACS software (Sec. 2). A PostgreSQL database hosted at INFN-CNAF (Italy) stores the analysis results, tracks the wafers during the entire process flow in NOA, and provides a comprehensive set of criteria for the QA/QC assessment and inventory purposes. The database is also used to keep track of the location and shipping status of wafers, which will be especially important as the detector is assembled.

4 SiPM Acceptance Criteria

The reverse and forward bias IV curves of each SiPM from all the production wafers are analyzed to ensure compliance with the following DS-20k wafer-level requirements: (i) breakdown voltage $V_{\mathrm{bd}} = 27.2 \pm 1.0$ V, (ii) quenching resistor $R_{\mathrm{q}} = 3.35 \pm 1.50$ MΩ, (iii) leakage current before breakdown (at 20 V) $I_L \leq 40$ pA and (iv) Goodness of Fit (GOF) ≤ 20. The first three requirements are set to obtain an acceptable production yield based on the dispersion of the just introduced parameters measured on pre-production FBK wafers.
The goodness of fit parameter is instead based on a χ^2 analysis of the shape of each reverse bias SiPM IV curve and places an upper limit on the SiPM correlated avalanche noise, *i.e.* crosstalk and afterpulse probability (Sec. 4.4.1). V_{bd}, GOF, and I_L are extracted from the reverse bias IV curve, while R_{q} is measured from the forward bias IV curve.

4.1 Breakdown Voltage Distribution

The SiPM breakdown voltage is defined as the voltage at which the first derivative with respect to the voltage of the SiPM current (in log space) is at a maximum [29]. A narrow distribution of this parameter is crucial when grouping SiPMs in tiles (24 SiPMs, Sec. 1) since a large difference in breakdown voltages would result in a gain mismatch when operating tiles at a common bias, reducing the tile single PE resolution [30][4].
Fig. 12 (top) shows the breakdown voltage distribution for all the 171336 tested SiPMs, while Fig. 14 shows the same information grouping SiPMs for their production Lot. At 77 K, the average Production (P) breakdown voltage is measured to be $V_{\mathrm{bd}}^{P} = 27.2 \pm 0.1$ V[5]. The dashed lines in the figure represent the DS-20k requirement (27.2 ± 1.0 V). The tested SiPMs comfortably satisfy this requirement.

The variance of the breakdown voltage distribution $\sigma^2_{V_{\mathrm{bd}}^{P}}$ after exclusion of the out-of-spec data is 0.019 V^2. This quantity can be decomposed into components:

$$\sigma^2_{V_{\mathrm{bd}}^{P}} = \sigma^2_{V_{\mathrm{bd}}^{P}/\mathrm{Lot}} + \sigma^2_{V_{\mathrm{bd}}^{P}/\mathrm{Wafer}} + \sigma^2_{V_{\mathrm{bd}}^{P}/\mathrm{SiPM}}, \tag{1}$$

where $\sigma^2_{V_{\mathrm{bd}}^{P}/\mathrm{Lot}}$ is the Lot-to-Lot variance, $\sigma^2_{V_{\mathrm{bd}}^{P}/\mathrm{Wafer}}$ is the Wafer-to-Wafer variance of a single Lot, and $\sigma^2_{V_{\mathrm{bd}}^{P}/\mathrm{SiPM}}$ is the SiPM-to-SiPM variance of a single wafer. Each variance contribution has been estimated with a Variance Component Analysis (VCA) [31]. The results are summarized in Table 1. 47.5% of the variance is due to the SiPM-SiPM variability within a wafer. The Lot contribution to the variance is 48.2%, and the remaining 4.2% is due to the Wafer to Wafer variability.

Factor	Samples	VC	% of Tot.	Cum. VC	Cum. Fact.
SiPM	169144	9.46	47.5	9.46	SiPM
Wafer	649	0.84	4.2	10.30	W/SiPM
Lot	57	9.59	48.2	19.89	L/W/SiPM
Total		19.89	100		

Table 1 Variance Component Analysis (VCA) of the Breakdown Voltage (V_{bd}) distribution. VC is the Variance Component in V^2 x 1000; % of Tot. is the percentage of each variance component; Cum. VC is the cumulative variance considering the incremental contribution of each component; Cum. Fact. represents the incremental nested factors contributing to the cumulative variance (W and L stand for Wafer and Lot).

Fig. 12 (bottom) shows a visual representation of this analysis using histograms.

[4]Within DS-20k, the single photoelectron resolution is defined as the ratio between half of the Gaussian width of the first Photo-electron Equivalent (PE) peak and its centroid.

[5]In what follows, we will always report summary results using the histogram median and half of its InterQuartile range (IQR/2) so that outliers don't affect the estimators.

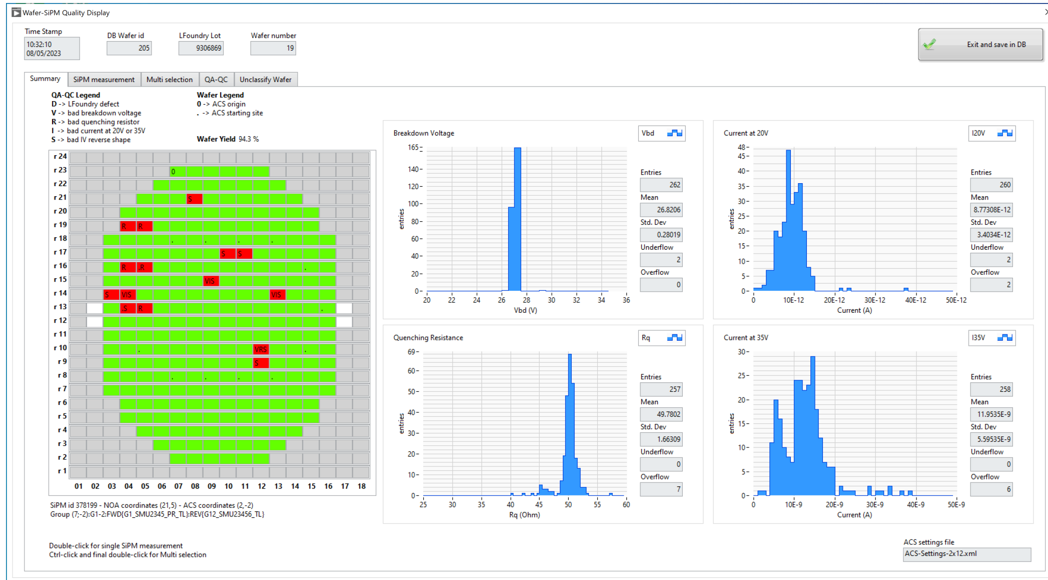

Fig. 10 Main display of the NOA Test Bench SiPM (NOA-TB-SiPM) Labview Application used to analyze the SiPM IV curves measured with the Keithley Automated Characterization Suite (ACS). For each wafer die a reverse and forward bias IV curve is measured at 77 K. Several results are shown to the operator before being stored in the database: (top-left) Breakdown Voltage (V_{bd}), (top-right) leakage current below the breakdown voltage (at 20 V) (I_L), (bottom-left) quenching resistor (R_{q}), and (bottom-right) current at 35 V. Wafer dice coloured in green (red) pass (fail) all (at least one) the wafer-level requirements presented in this work.

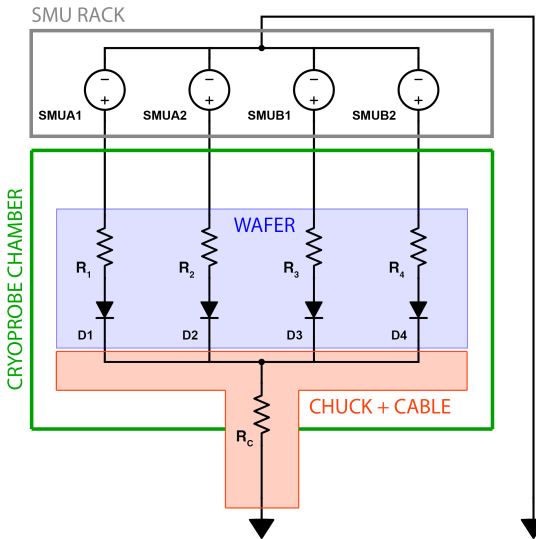

Fig. 11 Schematic of the measurement system for forward bias IV curves. R_C is the series resistance of the cryoprobe+SMUs measurement system, measured to be 3.6 Ω. R_i with $i = 1,2,3,4$ are the resistance of the 4 SiPMs measured in parallel.

We present three histograms: L/W/SiPM, W/SiPM, and SiPM. The L/W/SiPM histogram was obtained by subtracting the median value of the entire distribution from the breakdown voltage of each individual SiPM. Essentially, this represents the whole distribution, shifted to align its median with zero, including all three contributions (Lot, Wafer, SiPM) to the variance. The W/SiPM histogram was created by subtracting the median breakdown voltages within each Lot from the individual SiPM breakdown voltages. This approach removes the Lot-to-Lot contribution to the variance, resulting in each Lot having a median of 0 V. Similarly, the SiPM histogram was produced by subtracting the median breakdown voltages within each Wafer, thus eliminating the Wafer-to-Wafer contribution to the variance. Here the only contribution to the variance is due to the SiPMs themselves.

This representation shows that the breakdown voltage variability drops drastically when the contribution of the Lot is removed. Specifically, moving from L/W/SiPM to W/SiPM, the variance decreases by 9.59×10^{-3} V^2 or 48.2% of the total variance, according to Table 1.

Furthermore, when the Wafer-to-Wafer variability is removed, i.e., comparing W/SiPM with SiPM, the variance reduction is 0.84×10^{-3} V^2 (4.2% of the total), smaller than the previous case, resulting in a residual variance of 9.46×10^{-3} V^2 that accounts for the 47.5% of the total.

4.2 Quenching Resistor Distribution

The SiPM quenching resistor is calculated from the linear part of each forward biased IV curve (Fig. 8) in the regime where the resistance of the SPAD's pn-junction is negligible ($V > 1.25$ V) [32]. The inverse of the IV curve slope, after correcting for the voltage drop of the measurement system (Sec. 2), is the parallel resistance of all the SiPM SPADs' quenching resistors. A narrow distribution of this parameter is desirable when grouping SiPMs in tiles since a mismatch in the SiPM quenching resistor would produce a pulse-to-

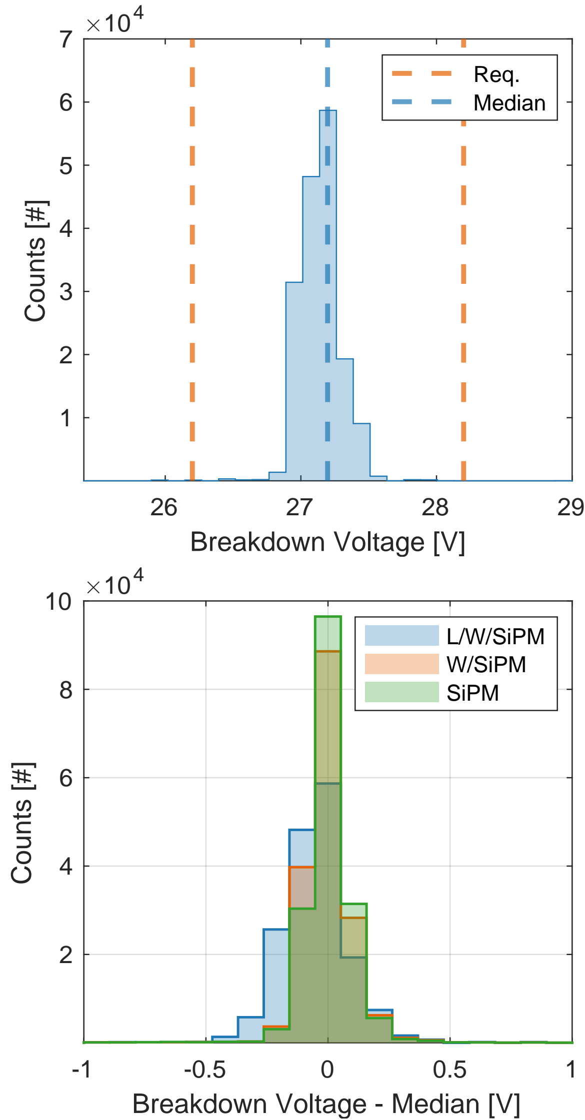

Fig. 12 (Top) Breakdown Voltage distribution of all the 171336 tested SiPMs. The red dashed lines represent the DS-20k requirements (27.2 ± 1.0 V), while the blue line the histogram median. 1311 SiPMs are outside the range of the plot. (Bottom) Breakdown voltage variability within single wafers (SiPM), mixing wafers in the same Lot (W/SiPM) and mixing Lots (L/W/SiPM). W and L stand for Wafer and Lot. See text for more details.

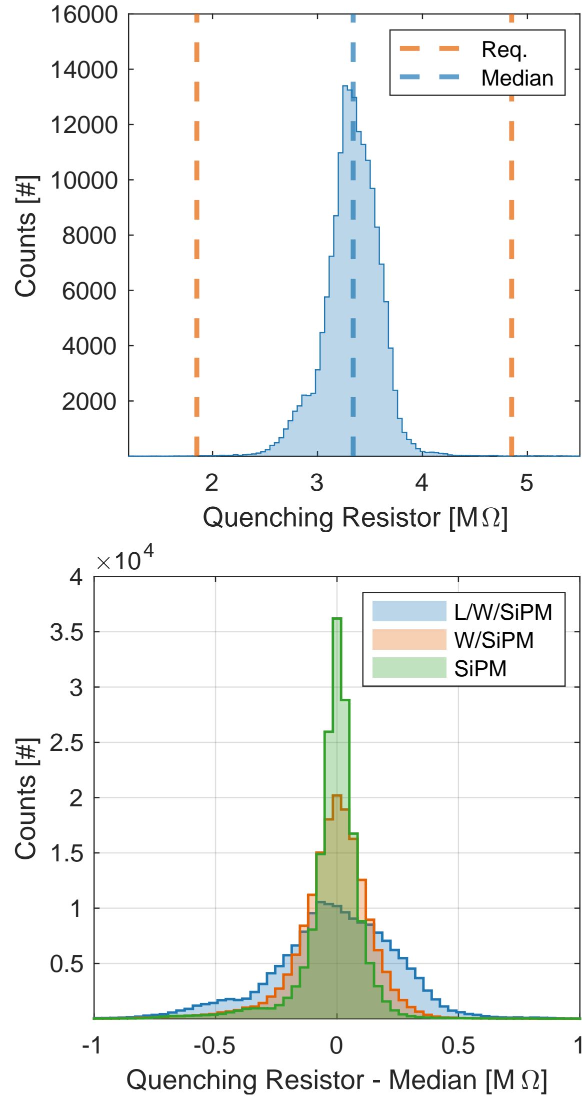

Fig. 13 (Top) Quenching Resistor distribution of all the 171336 tested SiPMs. The red dashed lines represent the DS-20k requirements (3.35 ± 1.50 MΩ), while the blue line the histogram median. 1196 SiPMs are outside the range of this plot. (Bottom) Quenching Resistor variability within single wafers (SiPM), mixing wafers in the same Lot (W/SiPM) and mixing Lots (L/W/SiPM). W and L stand for Wafer and Lot. See text for more details.

pulse variability of the SiPM pulse shape. If R_c is the series resistance of the measurement system ($R_c = 3.6\ \Omega$, Sec. 3), the SiPM SPAD quenching resistor (R_{q}) can be derived as follows

$$R_{\mathrm{q}} = [R^{*} - 4R_{C}] \times N_{\mathrm{cell}} \tag{2}$$

where R^{*} is the resistance measured using a linear fit to the forward bias IV-curve and $N_{\mathrm{cell}} = 94904$ is the number of SPAD cells in each SiPM. The factor 4 in Eq. 2 accounts for the fact that SiPMs are measured in parallel groups of 4, as introduced in Sec. 2 and also shown in Fig. 11.

Fig. 13 (top) shows the quenching resistor distribution for all 171336 SiPMs tested, while Fig. 15 shows the same information grouping SiPMs for their production Lot. At 77 K, the average Production (P) quenching resistor is measured to be $R_{\mathrm{q}}^{P} = 3.34 \pm 0.15$ MΩ. The dashed lines represent the DS-20k requirements (3.35 ± 1.50 MΩ).

Table 2 reports the quenching resistor VCA analysis. The production variance ($\sigma^{2}_{R_{\mathrm{q}}^{P}}$) after removing out-of-spec devices is equal to 0.077 (MΩ^{2}). Fig. 13 (bottom) shows a visual representation of this analysis, similarly to what was done in Sec. 4.1 for the SiPM breakdown voltage. The

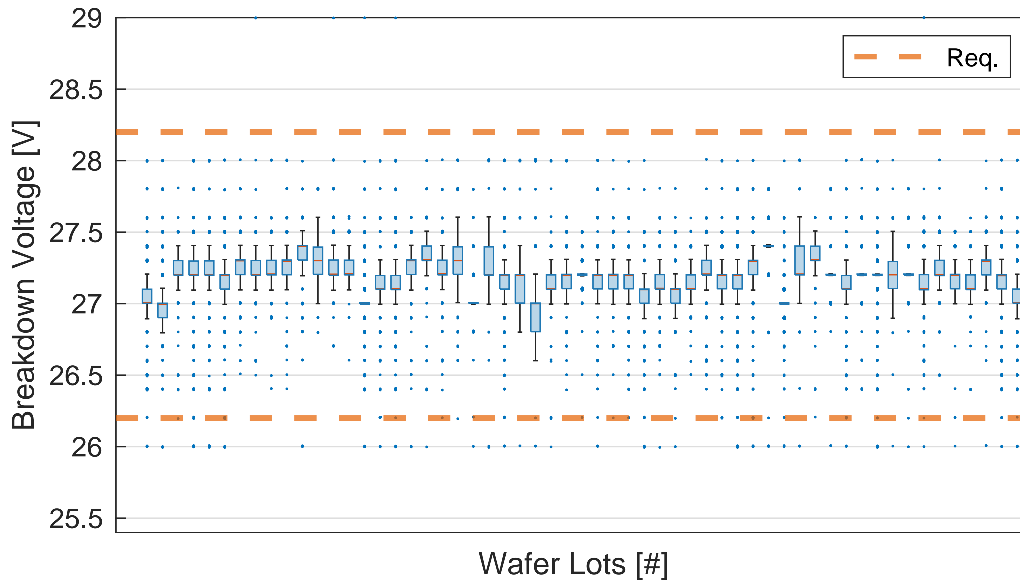

Fig. 14 Box plot of the measured breakdown voltage for all the production Lots. The orange line inside each box represents the sample median, while the top and bottom edges are the upper and lower quartiles. Dots represent outliers more than 1.5 InterQuartile Range (IQR) away from the top or bottom of each box. The dashed lines represent the DS-20k requirements (27.2 ± 1.0 V).

Factor	Samples	VC	% of Tot.	Cum. VC	Cum. Fact.
SiPM	169144	0.022	28.6	0.022	SiPM
Wafer	649	0.009	11.7	0.031	W/SiPM
Lot	57	0.046	59.7	0.077	L/W/SiPM
Total		0.077	100		

Table 2 Variance Component Analysis (VCA) of the Quenching Resistor (R_q) distribution. VC is the Variance Component in $(\mathrm{M\Omega})^2$; % of Tot. is the percentage of each variance component; Cum. VC is the cumulative variance considering the incremental contribution of each component; Cum. Fact. represents the incremental nested factors contributing to the cumulative variance (W and L stand for Wafer and Lot).

variability of the quenching resistor drops drastically when the contribution of the Lot is removed. Specifically, moving from L/W/SiPM to W/SiPM, the variance decreases by $0.046\,(\mathrm{M\Omega})^2$, or 59.7% of the total variance, according to Table 2. Additionally, when the Wafer-to-Wafer variability is removed, *i.e.*, comparing W/SiPM with SiPM, the variance is reduced by $0.009\,(\mathrm{M\Omega})^2$ which is a smaller amount compared to the previous case and corresponding to 11.7% of the total variance. The residual variance (SiPM) is 28.6% of the total.

4.3 Spatial Distribution of the Breakdown Voltage and Quenching Resistor

In the previous sections, we presented the breakdown voltage and quenching resistor variability with histograms and VCA analyses. Fig. 16 illustrates the typical spatial distribution of these two quantities on the surface of one production wafer, which was chosen as representative for the entire production. The results show that both parameters are generally uniform across the wafer, with only a few dice falling out of specification.

Based on the statistical analysis discussed earlier, the current strategy at the tile assembly stage is to freely combine dice from the same wafer and, when necessary, include dice from wafers within the same Lot. Given the consistent performance of SiPMs across a Lot, it is reasonable to consider the Lot as the fundamental grouping element at the tile assembly stage, rather than the individual wafer.

4.4 Correlated and uncorrelated noise

Dark and correlated avalanche noise are critical SiPM parameters that affect the overall DS-20k detector performance by increasing the number and the fluctuations of detected photons. Fluctuations in the number of detected photo-electrons, for example, may decrease the energy resolution of the detector, as shown in Ref. [33].

Dark noise is a spontaneous charge signal generated by an electron-hole pair formed by thermal or field-enhanced processes [34]. Correlated Avalanche (CA) noise is due to at least two processes: the production of secondary photons in the gain amplification stage during primary avalanches and the trapping and subsequent release of charge carriers produced in avalanches (afterpulsing). Several techniques are used to characterize these two sources of noise while oper-

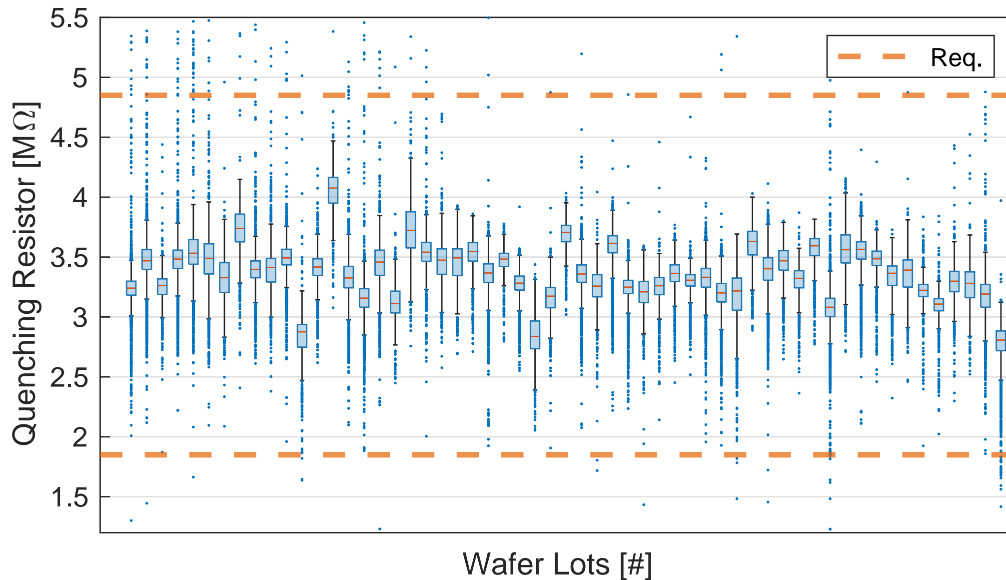

Fig. 15 Box plot of the measured quenching resistor for all production Lots. The line inside each box represents the sample median while the top and bottom edges are the upper and lower quartiles. Dots represent outliers more than 1.5 InterQuartile Range (IQR) away from the top or bottom of each box. The dashed lines represent the DS-20k requirement (3.35 ± 1.50 MΩ).

ating the SiPM in pulse counting mode [30,35,6]. However, estimating these properties directly from the wafer-level reverse bias IV curves is challenging.

In Sec. 4.4.1, we introduce a new technique that, starting from the shape of the reverse bias IV curve and, regardless of the level of SiPM illumination, ensures that all the production-graded SiPMs: (i) have similar CA noise and (ii) don't present an out-of-spec voltage dependence (*e.g.* high DCR). The leakage current before the breakdown voltage is also used as a control parameter to identify out-of-spec SiPMs (*e.g.* shorts). More details are reported in Sec. 4.4.2.

4.4.1 Goodness of fit

To reach the DS-20k design performance, all production-graded SiPMs must have similar correlated noise. The reverse bias SiPM IV curve is sensitive to this quantity. In general, the SiPM current under illumination can be written as [33]

$$I(V,\lambda) = f(V) \times \left[\mathrm{PDE}_\lambda(V) \times \Phi(\lambda) + \mathrm{R}^{\mathrm{DCR}}_{\mathrm{SiPM}}(V)\right] \tag{3}$$

where V is the SiPM reverse bias voltage, PDE_λ is the SiPM Photon Detection Efficiency (PDE), and $\Phi(\lambda)$ is the photon flux. $\mathrm{R}^{\mathrm{DCR}}_{\mathrm{SiPM}}(V)$ is the SiPM DCR. $f(V)$ is a correction factor that can be written as

$$f(V) \sim q_e \times \left(1 + \overline{\Lambda}\right) \times \overline{\mathrm{G}}_{1\ \mathrm{PE}}, \tag{4}$$

where $(\overline{\mathrm{G}}_{1\ \mathrm{PE}})$ is the SiPM gain for 1 Photo-electron Equivalent (PE) charge, $(\overline{\Lambda})$ is the CA noise contribution that artificially increases the total current produced by the SiPM and (q_e) is the electron charge [33][6].

$f(V)$ is a function of the applied bias voltage V but can be considered wavelength-independent because it depends only on the SiPM intrinsic characteristics. This is because the average sensor gain $(\overline{\mathrm{G}}_{1\ \mathrm{PE}})$ depends on the SiPM SPAD capacitance while afterpulses and optical crosstalk that contribute to the sensor CAs depend on impurities and cell geometry.

At 77 K, the DCR of these SiPMs is on the order of $\mathrm{mHz/mm^2}$ [15] and makes a negligible contribution to the total current. If we assume that all the SiPMs have identical characteristics *e.g.* efficiency and correlated noise, and their DCR is negligible compared to the incident photon flux Φ, the ratio point-to-point (*i.e.* at the same bias voltage) of two SiPMs' IV curves as a function of the applied bias voltage V is a voltage-independent quantity, only proportional to the ratio of the photon fluxes seen by the SiPMs, here called k, as follows

$$\frac{I_1(V,\lambda)}{I_2(V,\lambda)} = \frac{\Phi_1(\lambda)}{\Phi_2(\lambda)} \equiv k. \tag{5}$$

In order to ensure compliance of the wafer level IV curves with Eq. 5, we introduce a parameter called goodness of fit defined as follows

$$\mathrm{GOF} = \sum_i \frac{(I_i - k\overline{I}_i)^2}{\overline{\sigma_i^2}}, \tag{6}$$

[6] The SiPM gain $(\overline{\mathrm{G}}_{1\ \mathrm{PE}})$ and the CA noise contribution $(\overline{\Lambda})$ are voltage dependence as shown, for example, in Ref. [30,33]

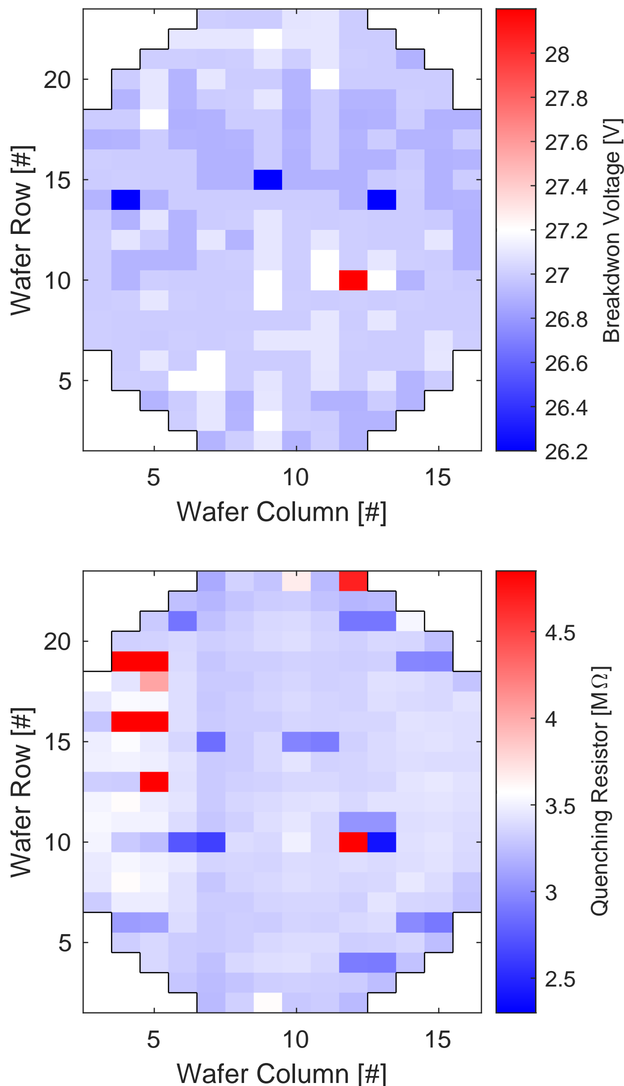

Fig. 16 Spatial distribution of the Breakdown Voltage (top) and Quenching Resistor (bottom) for Wafer 19 of Lot 9306869. This wafer is the same whose IV curves are shown in Fig. 8. To keep the scale readable, we associated to the few dice whose breakdown voltage and quenching resistor is outside the range of the figure a value equal to the closest axis range boundary.

where I_i is the IV curve of any SiPMs in the wafer, and $\overline{I_i}$ is current of a SiPM chosen as to be the reference for the entire DS-20k production, and whose IV curve is named reference-IV. $\overline{\sigma_i}$ is the uncertainty of the reference-IV curve. The sum in Eq. 6 is done over the bias voltage points in the IV curve, starting 0.7 V away from the breakdown voltage of the reference IV-curve ($\overline{I}$) after alignment of the breakdown voltage of the curve I with the one of $\overline{I}$. This was done to avoid the steep IV curve rise, close to the breakdown voltage, where large fluctuations due to baseline noise are present and would affect the GOF computation.
The scaling factor k (Eq. 5) can be calculated analytically by minimizing Eq. 6 as follows

$$k = \frac{\sum_i (\overline{I_i}\, I_i)/\overline{\sigma_i^2}}{\sum_i \overline{I_i^2}/\overline{\sigma_i^2}}. \tag{7}$$

The uncertainty $\overline{\sigma_i}$ is set to be equal to 22% of the reference IV curve, and it was computed accounting for the average point-to-point fluctuation. Fig. 17 shows a histogram of the GOF parameter for all the 171336 tested SiPMs.

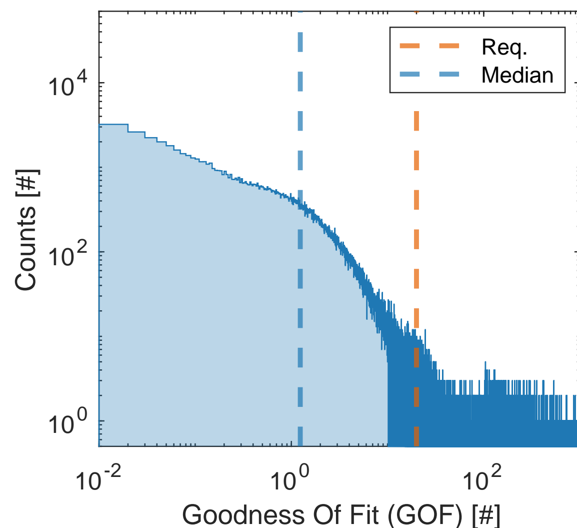

Fig. 17 Goodness of Fit (GOF) distribution of all the 171336 SiPMs tested. The dashed line represents the DS-20k requirements (GOF $\leq$ 20), while the blue line the histogram median. 4313 SiPMs are outside the range of the plot.

The median GOF is 1.2 meaning they are in excellent agreement with the reference IV curve when scaled with a constant scaling factor. There is a tail in the GOF distribution that ends at a GOF value of about 20.

Fig. 18 (top) shows the IV curves of the wafers shown in Fig. 8 categorized according to their GOF parameter. Fig. 18 (bottom) shows instead the same IVs scaled using the k-factor computed as reported in Eq. 7. The fluctuation due to the different light fluxes, after the breakdown voltage, is compensated and most of the SiPM IVs match within the error of the IV curve chosen as reference.

While IV curves with a GOF $>$ 20 are clearly different than the reference IV, there is little practical difference between IV curves with a GOF $\leq$ 20, which is the requirement set for the DS-20k production, as shown in Fig. 17. The upper limit for the GOF parameter (GOF $\leq$ 20) was indeed set at the 3σ level: *i.e.* 99.87% of the data meet the specification in a one-tailed test. A theoretical χ^2 distribution with 5 degrees of freedom contains 99.87% of the data below the value of 20.

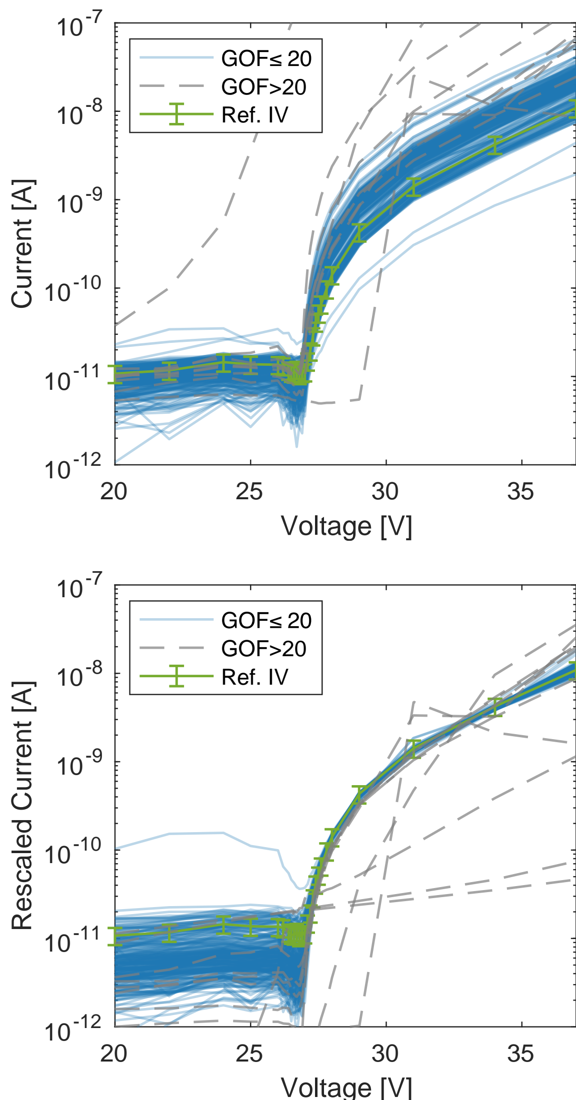

Fig. 18 Reverse bias IV curves for the production Wafer 19 of Lot 9306869 categorized according to their Goodness of Fit (GOF) parameter (Top). The bottom figures shows the same IVs, always categorized according to their GOF and scaled for the corresponding k-factor, computed as per Eq. 7.

4.4.2 SiPM leakage current

The cryoprobe vacuum chamber is not light-tight (Sec. 3), which means the SiPM current above the breakdown voltage can not be used as a measurement of the SiPM DCR. However, the current below breakdown can be used to identify out-of-spec SiPMs.
Below the breakdown voltage, the SiPM current is proportional to the SiPM photon flux. In the absence of gain (Geiger mode multiplication M=1) or under the presence of a proportional gain (M << $\overline{\mathrm{G}}_{1\ \mathrm{PE}}$) the small SPAD capacitance results in a very small current, on the order of a few fA or less, even under kHz of external illumination. This is below the sensitivity of the measurement system.

Fig. 19 shows a histogram of the leakage current measured at 20 V, several volts below the average breakdown voltage (Sec. 4.1).

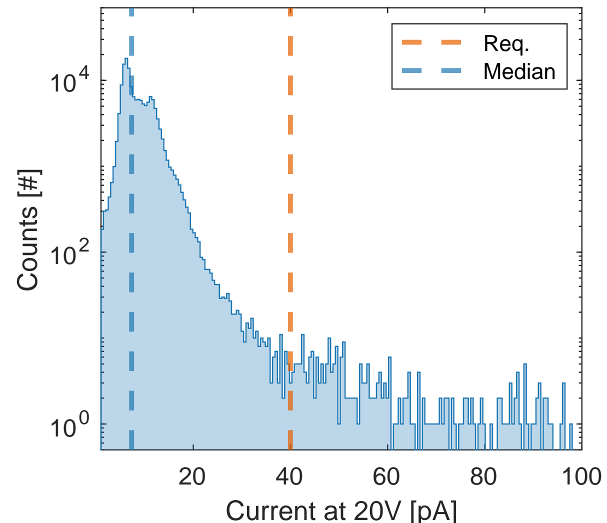

Fig. 19 Leakage Current distribution at 20 V of all the 171336 tested SiPMs. The dashed line represents the DS-20k requirements ($I_L \leq$ 40 pA), while the blue line the histogram median. 1081 SiPMs are outside the range of the plot.

At 77 K, the average Production (P) leakage current is measured to be $I_L^P = 7.2 \pm 2.3$ pA, which represents the measurement system noise floor (Sec. 2). The vertical line represents the DS-20k requirement ($I_L \leq 40$ pA). The upper spec limit for this parameter value was set at the 4σ level: *i.e.* 99.99% of the data meet the specs.

5 Correlation of the 300 K and 77 K Breakdown Voltage and Quenching Resistor data

In Sec. 3, we presented the NOA wafer testing workflow, which has a throughput of 0.35 wafers/hour. If NOA operates 12 hours/day, 7 days per week, with an up-time of 85%, 25 wafers/week can be measured. 26 m^2 of SiPMs will be tested for DS-20k, which will take a bit more than 1 year to complete.

Next-generation noble liquid cryogenic experiments, such as Argo and Darwin [36,37], plan to have SiPM-based photon-sensitive areas in excess of 100 m^2. Cryogenic wafer-level SiPM QA/QC at this scale will be challenging and will likely require several cryoprobing systems.

In this section, we study the correlation of the dice failure rate at 300 K and 77 K, to understand if room-temperature testing is adequate. Room temperature measurements could

likely be performed by the wafer supplier or using measurement systems that are more affordable than the cryogenic prober used in this work.

Fig. 20 shows the correlation between the SiPMs breakdown voltage (top) and the quenching resistor (bottom) measured by LFoundry at 300 K and by the cryoprobe system at 77 K. The cryoprobe (Sec. 2) in its actual configuration cannot in fact perform measurements at 300 K due to the mechanical tolerances of the probe card[7]. Each point in the figure represents a SiPM.

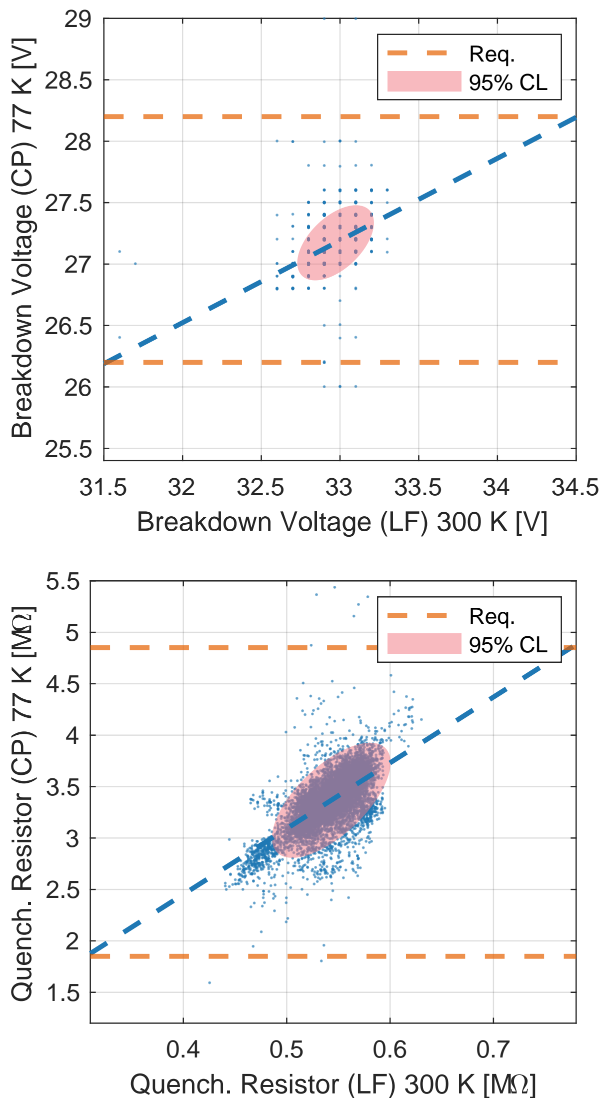

Fig. 20 Correlation of the breakdown voltage (top) and the quenching resistor (bottom) data measured by LFoundry (LF) at 300 K and by the cryoprobe (CP) at 77 K. Each point represents a SiPM. Horizontal orange lines are the SiPMs requirement at 77 K. The red circle represents the 95 % Confidence Level (CL) interval.

[7]The probe card is designed to operate at 77 K. At room temperature, the probe card expands and its needles do not contact the SiPM pads.

For each production wafer, LFoundry tested the breakdown voltage of 10% of the SiPM dice using a technique similar to the one presented in Sec. 4.1. The quenching resistor was instead measured by the foundry on nine lithographic shots per wafer with 8 SiPMs on each shot, using the Van Der Pauw method applied on the wafer dicing street[8]. Overall 19628 and 49436 dice were tested by LFoundry for V_{bd} and R_{q}, respectively.

The horizontal orange lines in Fig. 20 represent the 77 K dice requirements (Sec. 3) and the dashed blue lines are fit to the data. In the same figures, we also reported the 95 % Confidence Level (CL) interval. Table 3 reports the intersection between the 77 K requirements and the data fit line that shows a correlation between the 300 K and the 77 K dataset.

Quantity	77 [K]	300 [K]
V_{bd}[V]	27.2 ± 1.0	33 ± 1.5
R_{q}[MΩ]	3.35 ± 1.50	0.55 ± 0.25

Table 3 Breakdown voltage and quenching resistor requirements at 77 K and the extrapolated requirements at 300 K.

Other than being correlated, the two data sets have similar distributions. This can be seen by comparing the Z-Scored data of the two quantities at both temperatures using QQ-Plots [39], as shown in Fig. 21. Given a variable $X = V_{\mathrm{bd}}, R_{\mathrm{q}}$, the corresponding Z-scored quantity is defined as

$$Z = \frac{X - \overline{X}}{\sigma_X} \tag{8}$$

where $\overline{X}$ and σ_X are the mean and sigma of the corresponding distribution.

Both curves (300 K and 77 K) produce approximately a straight line and almost perfectly overlap, apart from the very edges, confirming they follow the same probability distribution.

The results presented in this section show that based on the measured data more than 99% of the dice that comply at room temperature are also compliant at cryogenic temperature. The low statistics of failing dice however do not allow us to conclude that the room temperature screening is sufficient to identify failing dice at cryogenic temperature. This is a consequence of the high wafer yield and low statistics of failing dice of the LFoundry production. New measurements, with a newly designed probe card that can operate at 300 K, are now being planned to further expand the results presented in this section. These also include the possibility

[8]The LFoundry measurements were performed before the deposition of the gold back-metallization (Fig. 3). The large backside resistance at this step of the manufacturing process prevents the usage of the forward bias IV curve, as was shown in Sec. 4.2. The two techniques yield comparable results, as shown in Ref. [38].

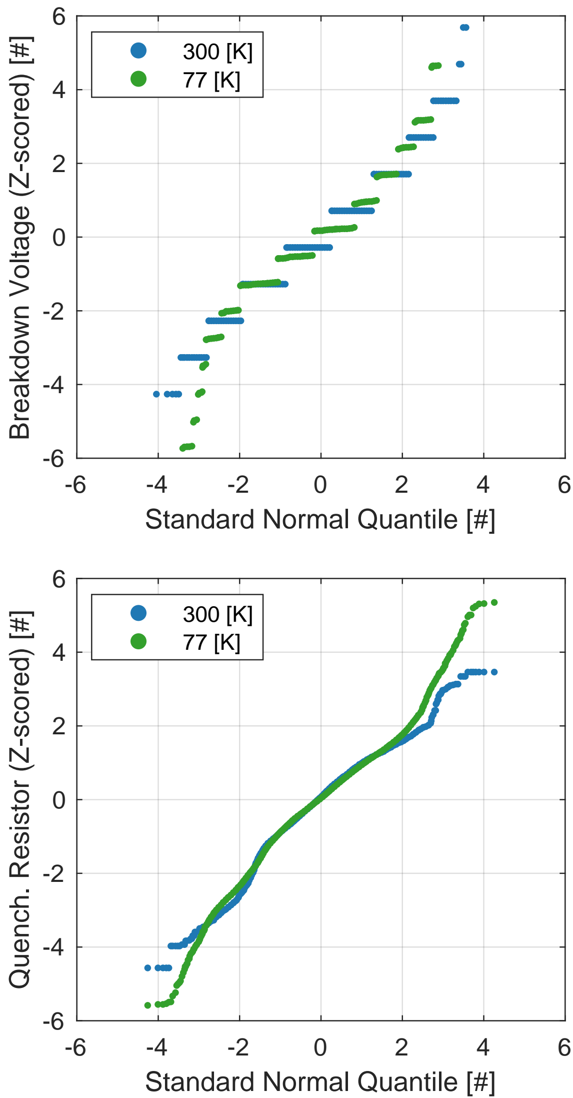

Fig. 21 QQ-Plots of the Z scored Breakdown Voltage (top) and Quenching Resistor (bottom) distributions for the 300 K and 77 K data. Both curves (300 K and 77 K) produce approximately a straight line and almost perfectly overlap, apart from the edges, confirming that the two datasets follow the same probability distribution .

of building a correlation not only based on the SiPMs breakdown voltage and quenching resistor, but also based on the GOF and leakage current parameters that could not be tested using the data presented in this work since LFoundry only performed measurements close to the dice breakdown voltage.

6 Wafer Production Yield

Fig. 22 shows a histogram of the wafer yield for all tested wafers. The yield has been computed based on the 264 testable dice per wafer. The dashed orange line represents the assumed production yield (80%), computed from pre-production

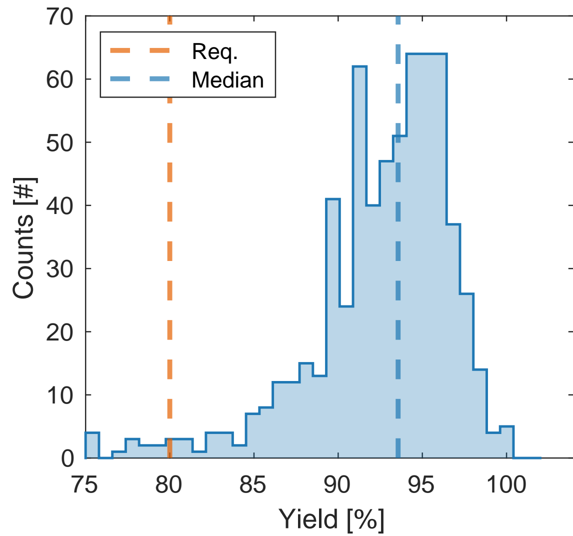

Fig. 22 Histogram of the wafer production yield after applying the screening presented in this work. The two dashed lines represent the histogram median (blue) and the expected production yield (red, 80%), which is based on the yields of pre-production from FBK.

wafers from FBK. The tested wafers not only meet but significantly exceed this requirement, with an overall yield of $93.6 \pm 2.5\%$. The Lot-to-Lot yield variation is also mostly negligible, apart for few Lots, as shown in Fig. 24.

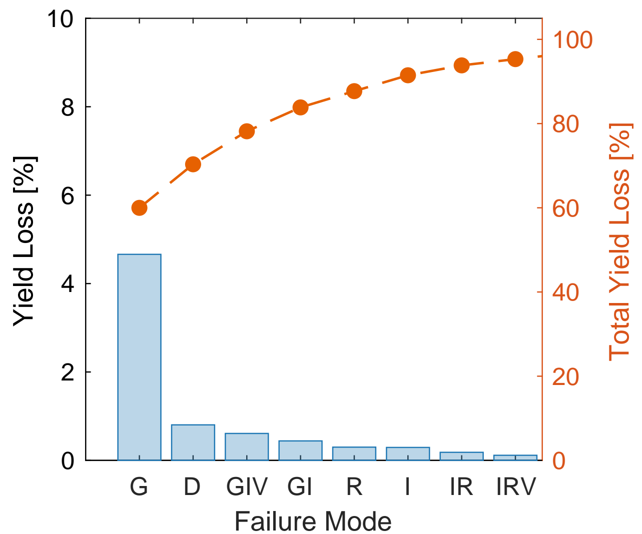

Fig. 23 Pareto plot that shows the source of the wafer yield loss differentiating SiPMs according to their failure loss mechanism: (i) Goodness of fit (G), (ii) leakage current below breakdown (I), (iii) defective pads (D), (iv) quenching resistor (R), (v) breakdown voltage (V) and their combination. To keep the figure readable only the largest source of yield loss are considered, since they overall constitute 95% of screened SiPMs.

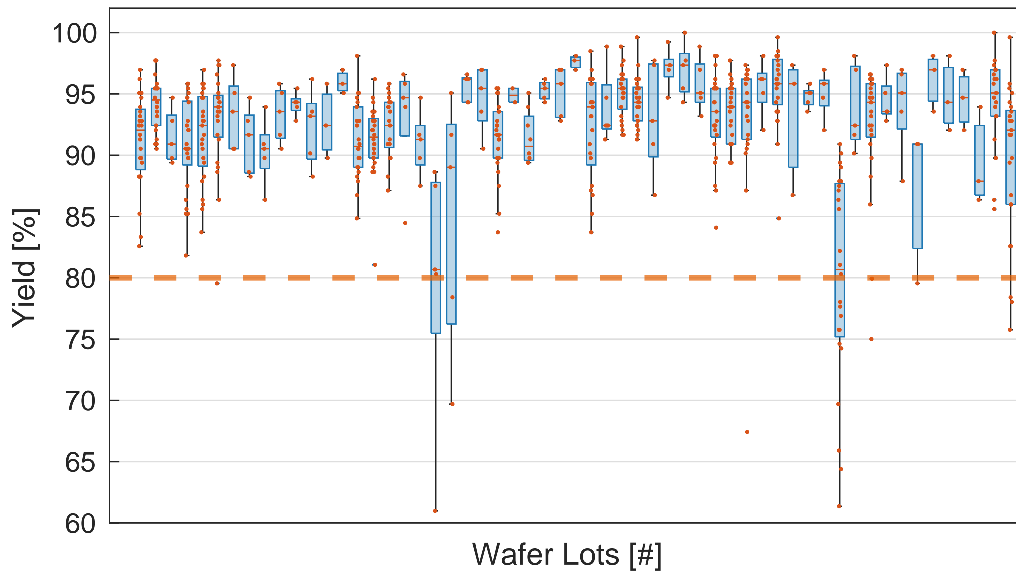

Fig. 24 Box plot of the yield for all production Lots. The line inside each box represents the sample median while the top and bottom edges are the upper and lower quartiles. Dots represents wafers in each Lot. The dashed lines represent the DS-20k requirement.

This represents a significant improvement if compared with the assumed pre-production results. Manufacturing facilities, such as LFoundry, invest heavily in optimizing their production processes and use equipment and technologies specifically designed for mass production, with infrastructures that contribute to stability and uniformity in the production process. Research institutes like FBK may have good equipment, but they might not always have the latest technology optimized for high-volume production. Their emphasis is more on prototyping and innovation rather than large-scale production, justifying the lower yield, on average.

Fig. 23 shows with a Pareto plot the sources of yield loss differentiating SiPMs according to their failure mechanism obtained by singularly applying the previously introduced requirement or by combining them. The largest source of yield loss is the Goodness of fit (G) cut, responsible for screening 4 % of the tested SiPMs. The subsequent source of yield loss not yet presented in the previous section of this work, is labelled D in Fig. 23 and it is due to dice classified as out-of-spec at LFoundry's outgoing optical inspection because they have one or more aluminum pads etched in an uncontrolled way during processing. An example of a defective failure is shown in Fig. 25. Note that these dice do not necessarily fail the characterization tests reported in previous sections of this work. Still, they may be problematic for other steps in the photosensor process flow (*e.g.* wire bonding). Rather than risk failures of entire tiles due to unforeseen issues with this defect, these dice are discarded, contributing a yield loss on the order of 1% in the overall wafer production.

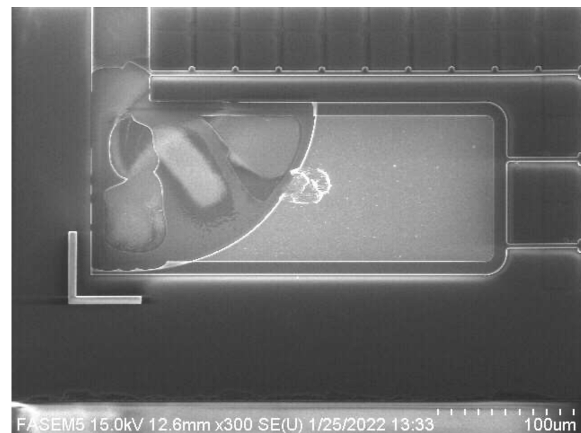

Fig. 25 Scanning Electron Microscope (SEM) image made by LFoundry of one SiPM pad that was marked as defective. The aluminum pad was etched in an uncontrolled way showing the layers at the bottom of the pad.

Fig. 23 also shows other sources of yield losses ordered by their progressively lower efficiency in screening SiPMs. Note that the SiPMs discarded only due to their breakdown voltage or quenching resistor represent a negligible fraction.

Fig. 26 shows again with a Pareto plot the same data of Fig. 23, but each of the failure mechanisms is treated as an independent quantity showing for each of the selection criteria the cumulative yield loss due to each requirement *i.e.* SiPMs can fail for one or more requirements at the same time.

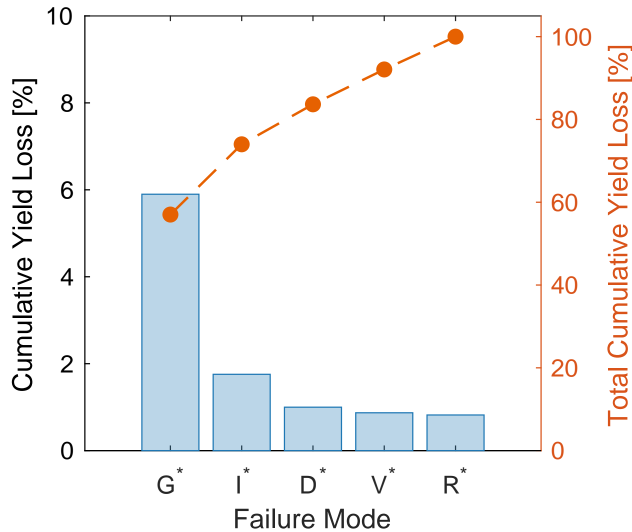

Fig. 26 Pareto plot that shows the cumulative source of the wafer yield loss. Each failure mechanism is treated as an independent quantity. The following yield loss mechanisms have been considered: (i) Goodness of fit (G*), (ii) leakage current below breakdown (I*), (iii) defective pads (D*), (iv) quenching resistor (R*), and (v) breakdown voltage (V*).

7 Wafer Campaign Control Plans

The DS-20k wafer testing campaign follows rigorous handling, storage and testing procedures. Wafer Lots are stored for their entire life in the NOA ISO-6 clean room (Sec. 1) sealed under vacuum anti-static bags. Storage parameters, such as humidity (HM), temperature (T), and radon contamination (RC), are monitored to ensure compliance with the DS-20k exposure specification ($\mathrm{HM} < 50\%, \mathrm{T} < 25\,\mathrm{C}^{\circ}, \mathrm{RC} < 50\,\mathrm{Bq/m^3}$).

During wafer handling, only certified tools, such as SPS vacuum pencils, are used to touch the gold back surface of the wafers (Fig. 3), while the wafer front surface is touched only with specifically designed tools *e.g.* the frame mounter for dicing operation (Fig. 2). The results of the wafer testing campaign are constantly monitored by using Statistical Process Control (SPC) Charts to detect trends or correlations with equipment parts (*e.g.* probe card needles degradation) and therefore to ensure the reliability of the cryo-probing operation over time. Moreover, process capability indices are used to measure the ability of the cryoprobe process to produce SiPMs within the specification limits.

More generally we monitor, on a weekly basis, three process Capability (Cp) indexes linked to the specifications presented in the previous sections of this work: CpL, CpU and Cpk. CpL(U) is a measurement of the cryoprobing process based on its Lower (Upper) Specification Limit LSL(USL). CpL and CpU are defined in Eq. 9 and Eq. 10 as the ratio of two values: (i) the distance between the mean of the measured quantity X and the lower (upper) specification limit LSL (USL), and (ii) the standard deviation of the process ($3\sigma_X$ variation)

$$\mathrm{CpL} = \frac{\overline{X} - \mathrm{LSL}}{3\sigma_X} \tag{9}$$

$$\mathrm{CpU} = \frac{\mathrm{USL} - \overline{X}}{3\sigma_X} \tag{10}$$

Fig. 27 shows the weekly-based CpU of the SiPM leakage current. The horizontal line at 1.33 is the conventional requirement used in the industry standard [40], which defines a $4\sigma_X$ difference between the mean of the measured quantity and its upper specification limit[9]. Fig. 27 also shows the number of wafers tested weekly. This number is not constant due to periodic maintenance of the cryoprobing system, which reduces the weekly wafer throughput.

Overall the leakage current below breakdown is within specification throughout the entire wafer testing campaign.

When upper and lower specifications are both needed to determine the process compliance, as is the case for breakdown voltage and quenching resistor specifications (Sec. 3), the CpL(U) index is substituted by the Cpk, which is defined as the ratio between: (i) the difference between the mean of the measured quantity X and the closest specification limit (USL or LSL), and (ii) the standard deviation of the process ($3\sigma_X$ variation):

$$\mathrm{Cpk} = \min\left[\frac{\mathrm{USL} - \overline{X}}{3\sigma_X}, \frac{\overline{X} - \mathrm{LSL}}{3\sigma_X}\right] \tag{11}$$

Figs. 28 and 29 show the Cpk of the quenching resistor and breakdown voltage. Similarly to the CpU leakage current discussion, the Cpks of both quantities are above the 1.33 specification for almost the entire production testing time. Their Cpks also show an artificial variability when compared to the leakage current CpU due to the overall wafer testing plan of the first production weeks. Only about 20% of the 25 wafers in each Lot were in fact tested during the first few weeks of operations before moving to the subsequent Lot. This was done to efficiently sample the entire LFoundry wafer production and establish an overview of the Lot-to-Lot variability of the production, which was expected to be the biggest component of the wafer variability (Sec. 3). Fig. 29 and Fig. 15 show therefore a correlation with the Lot-to-Lot quenching resistor variation. Figs. 28 and 29 also show a remarkably large Cpk (> 5) for a few weeks. This is again linked to the testing procedure, where only 1 wafer was tested in week 6 or 21, for example. Single wafers or

[9] Note as the CpU is computed using the weekly median and standard deviation, where the standard deviation is measured after removing the outliers defined as dice with more than 1.5 IQR above the upper quartile, as also shown in Sec. 4.1.

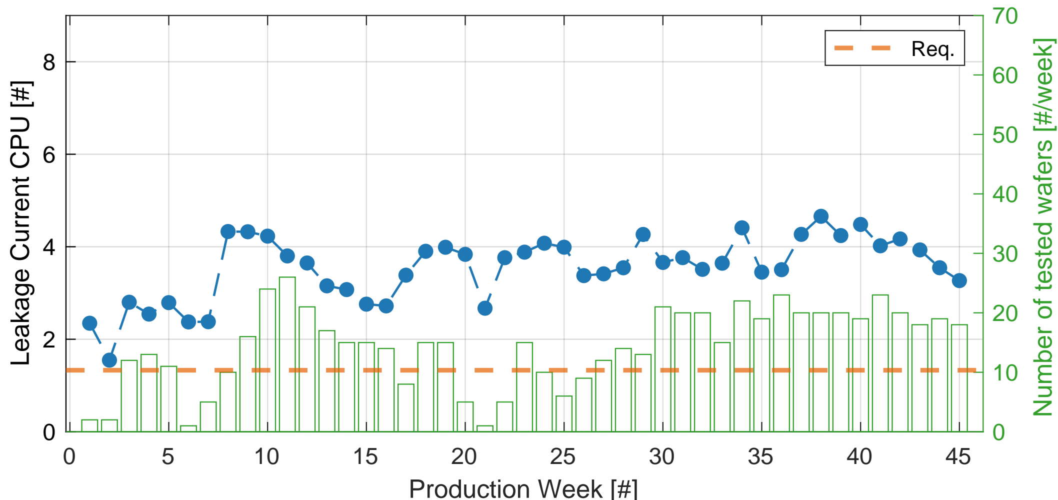

Fig. 27 Weekly upper specification limit (CpU) of the SiPM leakage current at 20 V (blue dots). The dashed orange line represents the industry standard of 1.33. The green bars are the number of wafers tested in each production week.

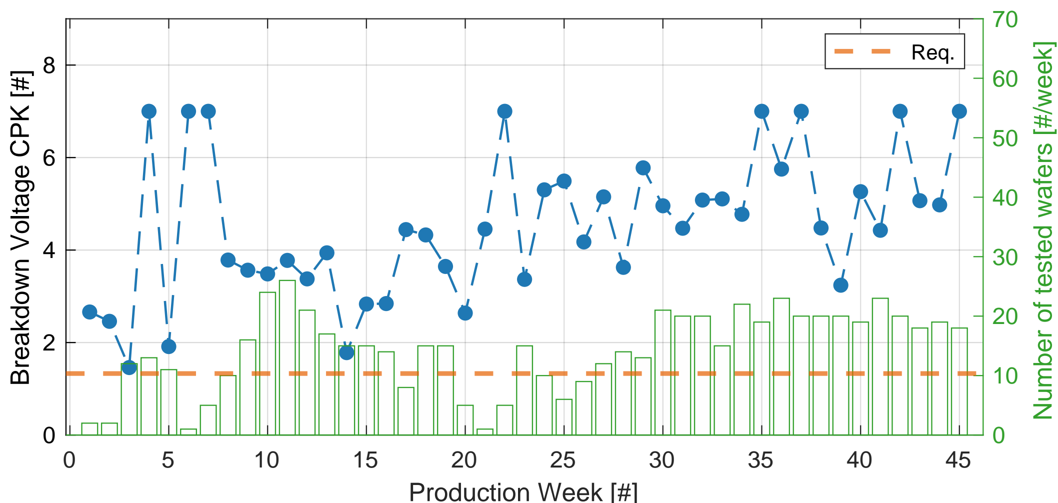

Fig. 28 Weekly based Cpk of the SiPM breakdown voltage (blue dots). The dashed orange line represents the industry standard of 1.33. The green bars are the number of wafers tested in each production week.

single Lots have in fact much tighter breakdown voltage and quenching resistor distributions when compared to the average weekly ones measured when mixing Lots, as shown in Sec. 4.1 and Sec. 4.2. Overall, the process capability indices show a fairly stable testing campaign, demonstrating the capability of the cryoprobing process to produce SiPMs within the specification limits.

8 Conclusions

This paper describes measurements performed in support of the DarkSide-20k experiment to characterize the properties of 1400 wafers of Fondazione Bruno Kessler (FBK) NUV-HD (near-UV sensitive, high-density) SiPMs produced by LFoundry. These wafers will be used to instruments the two 10.5 m^2 DS-20k TPC optical planes and the inner and outer veto detectors. This work focused on the quality control and quality assurance of 603 production wafers, representing 43% of the overall production. The data presented here sample all the 57 production Lots from LFoundry, capturing the Lot-to-Lot variation, the largest contributor to the production variability. We measure an average breakdown voltage at 77 K of $V^P_{\text{bd}} = 27.2 \pm 0.1$ V, where the central value represents the distribution median and the error half of its InterQuartile Range, that is comfortably within the DS-20k specification (27.2 ± 1 V). We measure an average quenching resistor value, the leakage current below breakdown, and a Goodness of Fit (GOF) parameter, all at 77 K, of $R^P_{\text{q}} = 3.34 \pm 0.15$ MΩ, $I^P_L = 7.2 \pm 2.3$ pA, and $\text{GOF}^P = 1.2 \pm 1.5$.

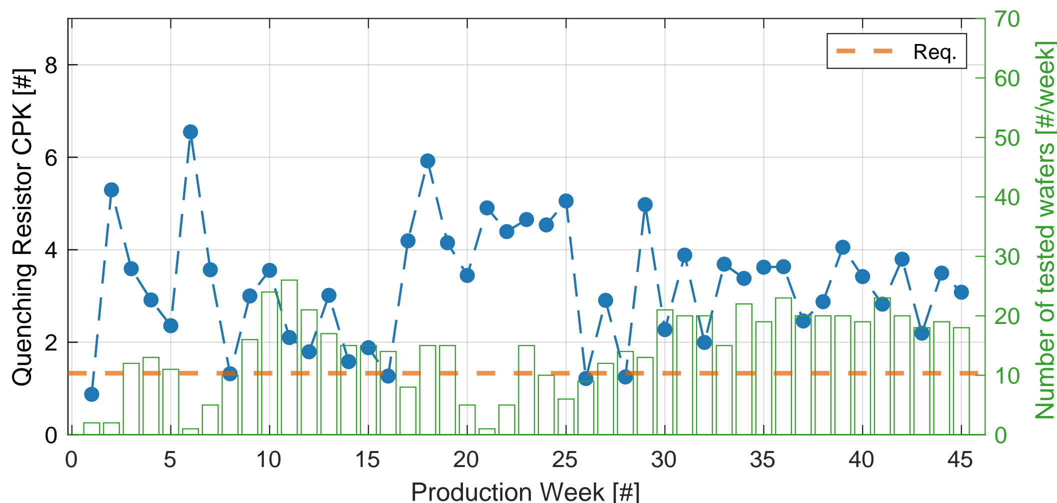

Fig. 29 Weekly Cpk of the SiPM quenching resistor (blue dots). The dashed orange line represents the industry standard of 1.33. The green bars are the number of wafers tested in each production week.

These values are consistent with the DS-20k specifications ($I_L \leq 40$ pA, $R_q = 3.35 \pm 1.50$ MΩ, GOF ≤ 20). In this work, we also show a correlation between the breakdown voltages and the quenching resistor values at room temperature and 77 K. More than 99% of the dice that are within specification at room temperature are also compliant at cryogenic temperature. The low statistics of failing dice however do not allow us to conclude that the room temperature screening is sufficient to identify failing dice at cryogenic temperature. This is a consequence of the high wafer yield and low statistics of failing dice of the LFoundry production. Finally, we presented process capability indices that monitor the stability of the cryoprobing operation over time for all the tested wafer-level parameters. The average production wafer yield is 93.6 ± 2.5%, which exceeds the 80% specification defined in the DarkSide-20k production plan. The wafer testing campaign is expected to conclude in 2025 if it continues at the current pace. Given the observed low variability between wafers within each Lot and the comprehensive testing of a representative sample from every Lot, we do not anticipate significant changes in the overall SiPM yield from the results presented in this work. Following the wafer-level testing, tile assembly and PDU assembly are progressing at NOA and in the UK, respectively. At this stage, a dedicated QA/QC and characterization program is in place, with the final step being a complete cryogenic test of fully assembled units. These tests are conducted across various collaboration institutions: for the TPC PDUs in Naples, and for the veto PDUs in Liverpool, Edinburgh, Lancaster, and Warsaw.

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The DarkSide-20k Collaboration

F. Acerbi[1], P. Adhikari[2], P. Agnes[3,4], I. Ahmad[5], S. Albergo[6,7], I. F. Albuquerque[8], T. Alexander[9], A. K. Alton[10], P. Amaudruz[11], M. Angiolilli[3,4], E. Aprile[12], M. Atzori Corona[13,14], D. J. Auty[15], M. Ave[8], I. C. Avetisov[16], O. Azzolini[17], H. O. Back[18], Z. Balmforth[75], A. Barrado Olmedo[20], P. Barrillon[21], G. Batignani[22,23], P. Bhowmick[24,87], M. Bloem[87], S. Blua[25,26], V. Bocci[27], W. Bonivento[13], B. Bottino[28,29], M. G. Boulay[2], A. Buchowicz[32], S. Bussino[33], J. Busto[21], M. Cadeddu[13], M. Cadoni[13,14], R. Calabrese[50,34], V. Camillo[35], A. Caminata[29], N. Canci[34], A. Capra[11], M. Caravati[3,4], M. Cardenas-Montes[20], N. Cargioli[13,14], M. Carlini[4], P. Castello[13,36], P. Cavalcante[4], S. Cebrian[37], J. Cela Ruiz[20], S. Chashin[38], A. Chepurnov[38], L. Cifarelli[40,39], D. Cintas[37], B. Cleveland[41,42], Y. Coadou[21], V. Cocco[13], D. Colaiuda[4,43], E. Conde Vilda[20], L. Consiglio[4], B. S. Costa[8], M. Czubak[44], S. D'Auria[46,31], M. D. Da Rocha Rolo[25], G. Darbo[29], S. Davini[29], R. de Asmundis[34], S. De Cecco[47,27], G. Dellacasa[25], A. V. Derbin[49], F. Di Capua[50,34], L. Di Noto[29], P. Di Stefano[51], L. K. Dias[8], C. Dionisi[47,27], G. Dolganov[53], F. Dordei[13], V. Dronik[54], A. Elersich[55], E. Ellingwood[51], T. Erjavec[55], N. Fearon[24], M. Fernandez Diaz[20], A. Ficorella[1], G. Fiorillo[50,34], P. Franchini[19,56], D. Franco[57], H. Frandini Gatti[58], E. Frolov[59], F. Gabriele[13], D. Gahan[13,14], C. Galbiati[52], G. Galiski[32], G. Gallina[52], G. Gallus[13,36], M. Garbini[60,39], P. Garcia Abia[20], A. Gawdzik[61], A. Gendotti[62], G. K. Giovanetti[63], V. Goicoechea Casanueva[64], A. Gola[1], L. Grandi[65], G. Grauso[34], G. Grilli di Cortona[47], A. Grobov[53], M. Gromov[38], M. Gulino[66,88], C. Guo[67], B. R. Hackett[9], A. Hallin[15], A. Hamer[68], M. Haranczyk[44], T. Hessel[57], S. Horikawa[4,43], J. Hu[15], F. Hubaut[21], J. Hucker[51], T. Hugues[51,5], E. V. Hungerford[69], A. Ianni[52], G. Ippoliti[4], V. Ippolito[27], A. Jamil[52], C. Jillings[41,42], R. Keloth[35], N. Kemmerich[8], A. Kemp[87], Carlos E. Kester[8], M. Kimura[5], K. Kondo[4,43], G. Korga[19], L. Kotsiopoulou[68], S. Koulosousas[19], A. Kubankin[54], P. Kunze[3,4], M. Kuss[22], M. Kuźniak[5], M. Kuzwa[5], M. La Commara[70,34], M. Lai[71], E. Le Guirriec[21], E. Leason[24], A. Leoni[4,43], L. Lidey[9], M. Lissia[13], L. Luzzi[20], O. Lychagina[72], O. Macfadyen[19], I. N. Machulin[53,73], S. Manecki[41,42,51], I. Manthos[75], A. Marasciulli[4], G. Margutti[76], S. M. Mari[33], C. Mariani[35], J. Maricic[64], M. Martinez[37], C. J. Martoff[9,77], G. Matteucci[50,34], K. Mavrokoridis[58], E. Mazza[4], A. B. McDonald[51], S. Merzi[1], A. Messina[47,27], R. Milincic[64], S. Minutoli[29], A. Mitra[78], J. Monroe[24], E. Moretti[1], M. Morrocchi[23,22], T. Mroz[44], V. N. Muratova[49], M. Murphy[35], M. Murra[12], C. Muscas[13,36], P. Musico[29], R. Nania[39], M. Nessi[79], G. Nieradka[5], K. Nikolopoulos[74,75], E. Nikoloudaki[57], J. Nowak[56], K. Olchanski[11], A. Oleinik[54], V. Oleynikov[59], P. Organtini[4,52], A. Ortiz de Solrzano[37], M. Pallavicini[28,29], L. Pandola[66], E. Pantic[55], E. Paoloni[23,22], D. Papi[15], G. Pastuszak[32], G. Paternoster[1], P. A. Pegoraro[13,36], K. Pelczar[44], R. Perez[8], V. Pesudo[20], S. Piacentini[3,4], N. Pino[7,6], G. Plante[12], A. Pocar[80], M. Poehlmann[55], S. Pordes[35], P. Pralavorio[21], E. Preosti[52], D. Price[61], S. Puglia[6,7], M. Queiroga Bazetto[58], F. Ragusa[46,31], Y. Ramachers[78], A. Ramirez[69], S. Ravinthiran[58], M. Razeti[13], A. L. Renshaw[69], M. Rescigno[27], S. Resconi[31], F. Retiere[11], L. P. Rignanese[39], A. Rivetti[25], A. Roberts[58], C. Roberts[61], G. Rogers[74], L. Romero[20], M. Rossi[29], A. Rubbia[62], D. Rudik[50,34,73], M. Sabia[47,27], P. Salomone[47,27], O. Samoylov[72], S. Sanfilippo[66], D. Santone[24], R. Santorelli[20], E. Moura Santos[8], C. Savarese[89], E. Scapparone[39], F. G. Schuckman II[51], G. Scioli[40,39], D. A. Semenov[49], A. Sheshukov[72], M. Simeone[81,34], P. Skensved[51], M. D. Skorokhvatov[53,73], O. Smirnov[72], T. Smirnova[53], B. Smith[11], A. Sotnikov[72], F. Spadoni[9], M. Spangenberg[78], R. Stefanizzi[13], A. Steri[13,82], V. Stornelli[4,43], S. Stracka[22], S. Sulis[13,36], A. Sung[52], C. Sunny[5], Y. Suvorov[50,34,53], A. M. Szelc[68], O. Taborda [3,4], R. Tartaglia[4], A. Taylor[58], J. Taylor[58], G. Testera[29], K. Thieme[64], A. Thompson[19], S. Torres-Lara[69], A. Tricomi[6,7], E. V. Unzhakov[49], M. Van Uffelen[21], T. Viant[62], S. Viel[2], A. Vishneva[72], R. B. Vogelaar[35], J. Vossebeld[58], B. Vyas[2], M. Wada[5], M. Walczak[3,4], Y. Wang[67,83], H. Wang[84], S. Westerdale[71], L. Williams[85], R. Wojaczyski[5], M. M. Wojcik[44], M. Wojcik[86], T. Wright[35], Y. Xie[67,83], C. Yang[67,83], J. Yin[67,83], A. Zabihi[5], P. Zakhary[5], A. Zani[31], Y. Zhang[67], T. Zhu[55], A. Zichichi[40,39], G. Zuzel[44], M. P. Zykova[16]

1. Fondazione Bruno Kessler, Povo 38123, Italy
2. Department of Physics, Carleton University, Ottawa, ON K1S 5B6, Canada
3. Gran Sasso Science Institute, L'Aquila 67100, Italy
4. INFN Laboratori Nazionali del Gran Sasso, Assergi (AQ) 67100, Italy
5. AstroCeNT, Nicolaus Copernicus Astronomical Center of the Polish Academy of Sciences, 00-614 Warsaw, Poland
6. INFN Catania, Catania 95121, Italy
7. Università of Catania, Catania 95124, Italy
8. Instituto de Física, Universidade de São Paulo, São Paulo 05508-090, Brazil
9. Pacific Northwest National Laboratory, Richland, WA 99352, USA
10. Physics Department, Augustana University, Sioux Falls, SD 57197, USA
11. TRIUMF, 4004 Wesbrook Mall, Vancouver, BC V6T 2A3, Canada
12. Physics Department, Columbia University, New York, NY 10027, USA
13. INFN Cagliari, Cagliari 09042, Italy
14. Physics Department, Università degli Studi di Cagliari, Cagliari 09042, Italy
15. Department of Physics, University of Alberta, Edmonton, AB T6G 2R3, Canada
16. Mendeleev University of Chemical Technology, Moscow 125047, Russia
17. INFN Laboratori Nazionali di Legnaro, Legnaro (Padova) 35020, Italy
18. Savannah River National Laboratory, Jackson, SC 29831, United States
19. Department of Physics, Royal Holloway University of London, Egham TW20 0EX, UK
20. CIEMAT, Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas, Madrid 28040, Spain
21. Centre de Physique des Particules de Marseille, Aix Marseille Univ, CNRS/IN2P3, CPPM, Marseille, France
22. INFN Pisa, Pisa 56127, Italy
23. Physics Department, Università degli Studi di Pisa, Pisa 56127, Italy
24. University of Oxford, Oxford OX1 2JD, United Kingdom
25. INFN Torino, Torino 10125, Italy
26. Department of Electronics and Telecommunications, Politecnico di Torino, Torino 10129, Italy
27. INFN Sezione di Roma, Roma 00185, Italy
28. Physics Department, Università degli Studi di Genova, Genova 16146, Italy
29. INFN Genova, Genova 16146, Italy
30. Civil and Environmental Engineering Department, Politecnico di Milano, Milano 20133, Italy
31. INFN Milano, Milano 20133, Italy
32. Institute of Radioelectronics and Multimedia Technology, Warsaw University of Technology, 00-661 Warsaw, Poland
33. INFN Roma Tre, Roma 00146, Italy

34. INFN Napoli, Napoli 80126, Italy
35. Virginia Tech, Blacksburg, VA 24061, USA
36. Department of Electrical and Electronic Engineering, Università degli Studi di Cagliari, Cagliari 09123, Italy
37. Centro de Astropartículas y Física de Altas Energías, Universidad de Zaragoza, Zaragoza 50009, Spain
38. Skobeltsyn Institute of Nuclear Physics, Lomonosov Moscow State University, Moscow 119234, Russia
39. INFN Bologna, Bologna 40126, Italy
40. Department of Physics and Astronomy, Università degli Studi di Bologna, Bologna 40126, Italy
41. Department of Physics and Astronomy, Laurentian University, Sudbury, ON P3E 2C6, Canada
42. SNOLAB, Lively, ON P3Y 1N2, Canada
43. Università degli Studi dell'Aquila, L'Aquila 67100, Italy
44. M. Smoluchowski Institute of Physics, Jagiellonian University, 30-348 Krakow, Poland
45. Department of Structures for Engineering and Architecture, Università degli Studi "Federico II" di Napoli, Napoli 80126, Italy
46. Physics Department, Università degli Studi di Milano, Milano 20133, Italy
47. Physics Department, Sapienza Università di Roma, Roma 00185, Italy
48. Chemistry, Materials and Chemical Engineering Department "G. Natta", Politecnico di Milano, Milano 20133, Italy
49. Saint Petersburg Nuclear Physics Institute, Gatchina 188350, Russia
50. Physics Department, Università degli Studi "Federico II" di Napoli, Napoli 80126, Italy
51. Department of Physics, Engineering Physics and Astronomy, Queen's University, Kingston, ON K7L 3N6, Canada
52. Physics Department, Princeton University, Princeton, NJ 08544, USA
53. National Research Centre Kurchatov Institute, Moscow 123182, Russia
54. Radiation Physics Laboratory, Belgorod National Research University, Belgorod 308007, Russia
55. Department of Physics, University of California, Davis, CA 95616, USA
56. Physics Department, Lancaster University, Lancaster LA1 4YB, UK
57. APC, Université de Paris Cité, CNRS, Astroparticule et Cosmologie, Paris F-75013, France
58. Department of Physics, University of Liverpool, The Oliver Lodge Laboratory, Liverpool L69 7ZE, UK
59. Budker Institute of Nuclear Physics, Novosibirsk 630090, Russia
60. Museo Storico della Fisica e Centro Studi e Ricerche Enrico Fermi, Roma 00184, Italy
61. Department of Physics and Astronomy, The University of Manchester, Manchester M13 9PL, UK
62. Institute for Particle Physics, ETH Zürich, Zürich 8093, Switzerland
63. Williams College, Physics Department, Williamstown, MA 01267 USA
64. Department of Physics and Astronomy, University of Hawai'i, Honolulu, HI 96822, USA
65. Department of Physics and Kavli Institute for Cosmological Physics, University of Chicago, Chicago, IL 60637, USA
66. INFN Laboratori Nazionali del Sud, Catania 95123, Italy
67. Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China
68. School of Physics and Astronomy, University of Edinburgh, Edinburgh EH9 3FD, UK
69. Department of Physics, University of Houston, Houston, TX 77204, USA
70. Pharmacy Department, Università degli Studi "Federico II" di Napoli, Napoli 80131, Italy
71. Department of Physics and Astronomy, University of California, Riverside, CA 92507, USA
72. Joint Institute for Nuclear Research, Dubna 141980, Russia
73. National Research Nuclear University MEPhI, Moscow 115409, Russia
74. School of Physics and Astronomy, University of Birmingham, Edgbaston, B15 2TT, Birmingham, UK
75. Institute of Experimental Physics, University of Hamburg, Luruper Chaussee 149, 22761, Hamburg, Germany
76. LFoundry S.r.l, Via Antonio Pacinotti 7, Avezzano AQ 67051, IT
77. Physics Department, Temple University, Philadelphia, PA 19122, USA
78. University of Warwick, Department of Physics, Coventry CV47AL, UK
79. Istituto Nazionale di Fisica Nucleare, Roma 00186, Italia
80. Amherst Center for Fundamental Interactions and Physics Department, University of Massachusetts, Amherst, MA 01003, USA
81. Chemical, Materials, and Industrial Production Engineering Department, Università degli Studi "Federico II" di Napoli, Napoli 80126, Italy
82. Department of Mechanical, Chemical, and Materials Engineering, Università degli Studi, Cagliari 09042, Italy
83. University of Chinese Academy of Sciences, Beijing 100049, China
84. Physics and Astronomy Department, University of California, Los Angeles, CA 90095, USA
85. Department of Physics and Engineering, Fort Lewis College, Durango, CO 81301, USA
86. Institute of Applied Radiation Chemistry, Lodz University of Technology, 93-590 Lodz, Poland
87. Science & Technology Facilities Council (STFC), Rutherford Appleton Laboratory, Technology, Harwell Oxford, Didcot OX11 0QX, UK
88. Engineering and Architecture Faculty, Università di Enna Kore, Enna 94100, Italy
89. Center for Experimental Nuclear Physics and Astrophysics, and Department of Physics, University of Washington, Seattle, WA 98195, USA