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Irradiation test for BETSEE at CSNS for ATLAS ITk strip upgrade

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Abstract: ITk strip module is the basic unit in ITk strip upgrade, to perform an irradiation test on a strip module using a beam size that is not too large, the collaboration develop a smaller board called Board for Evaluation of Triple chip Single Event Effect (BETSEE). This paper will introduce the result for the BETSEE test with all latest version of ASICs using proton beam at China Spallation Neutron Source. The TID effect were monitored because of the high flux in CSNS.

Keywords: HL-LHC, CSNS, BETSEE, Irradiation, ASIC

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1 Introduction

The ATLAS inner detector will have a phase II upgrade to the new ATLAS inner tracker (ITk) to reach the requirements for the High Luminosity Large Hadron Collider (HL-LHC) [1, 2], which will be an all-silicon detector and including the pixel tracker on the inner side [3] and the strip tracker on the outer side [4].

For the ITk strip, the minimum unit for data acquisition (DAQ) is called strip module, if it is a barrel short strip module, which is composed of a silicon sensor, two hybrid and a powerboard. Barrel long strip modules only have one hybrid and the endcap modules have complex layouts. Hybrid is the direct part for data collection, which include 10 ATLAS Binary Chip (ABC), and 1 Hybrid Controller Chip (HCC). Powerboard is a big board for power supply of the whole module, where the central chip to control the powerboard is called Autonomous Monitoring and Control Chip (AMAC) [5]. These three kinds of ASIC chips are the main components of DAQ electrics, and are also the main object to be protected under a high irradiation environment. When irradiation beam pass through chips, the high energy particles will cause different effects on the electrics, including Single Event Effects (SEEs), which is caused by single particle, and Total Ionising Dose effect (TID), this is due to the cumulative total irradiation dose to which the chip has been exposed. SEE mainly manifested as storage bit flips inside the chips and TID could be observed by current increase from the chip. These effects could disrupt the normal procedure of chips and should be seriously considered.

In this case, all these kinds of chips have been radiation-hardened designed for several iterations. For the final version, Triple Modular Redundancy (TMR) is highly used on digital circuit to protect against SEEs [6]. To test ASIC's irradiation performance, in addition to performing single chip tests on all of them [5, 7, 8], it's also necessary to test them in a working module to check their communications and the system performance. Since a real module is too large for the irradiation beam to cover completely, the collaboration has developed a smaller Board for Evaluation of Triple chip Single Event Effect (BETSEE) board specifically for this testing purpose [9].

Our test was using 80 MeV proton beam at China Spallation Neutron Source (CSNS). One feature for CSNS was the quite high beam flux to be 6.60×10^9p/cm^2/s, which was never been used in BETSEE test before. The test lasted 19 hours, during which communication issues with the powerboard were identified in the first 9 hours while using this high flux, we reduced the beam energy to 70 MeV for the remaining 10 hours, which lowered the flux to 1.30×10^9p/cm^2/s. A notable result was that the powerboard fully lost all communications and would even stop supplying power at high flux. This shows powerboard still have a bad behavior under high flux irradiation. For hybrid, we can see that TMR has done a good protection for ABC and HCC chips against SEEs. However, TID current is still too huge and causes the system running unstable under such a big flux.

Testing details and results from proton irradiation will be presented and discussed in section 2 and 3, respectively. Conclusions will be provided in section 4.

2 CSNS irradiation

In September 2023, we performed irradiation test about BETSEE at the Associated Proton Experimental Platform at CSNS [10] in China, since BETSEE is basically a small module, all hardware requirement and their connections are same as a module test. The control PC connect to Field-Programmable Gate Array (FPGA) board with a network cable for data transmission and a USB cable for FPGA programming [11]. Then FPGA connect together with FPGA Mezzanine Card (FMC-DP) board [12]. FMC-DP board has 6 groups of interface to connect with modules. Additionally, PC is connected to the low voltage power supply for control and monitoring purposes.

During beam tests, we construct a lead brick enclosure and place the FPGA and FMC-DP board inside to shield the devices from irradiation that could potentially impact our results, additionally, the control PC is positioned 10 meters away to ensure a more stable environment. Only the BETSEE is exposed to the proton irradiation environment as Figure 1.

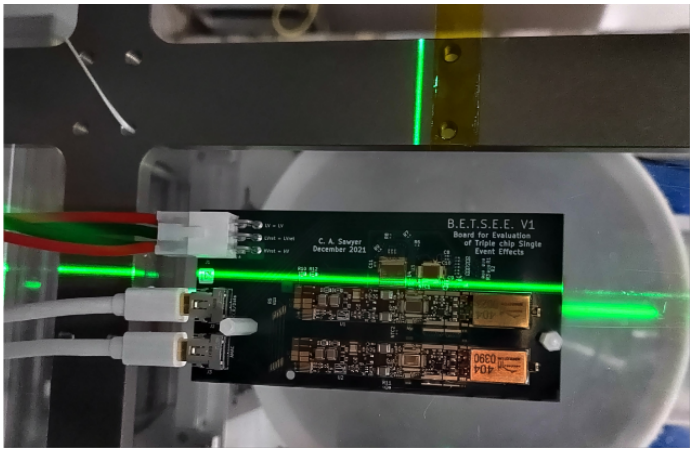

Figure 1. BETSEE board mounted to platform during proton beam running. The green lines shows the rough location of the beam spot with the AMAC, ABC, and HCC inside.

The red and black cables, which are power lines, connect to an 11V low voltage supply. Two mini-DP lines link to the previously mentioned FMC-DP board. The beam is 3cm × 3cm square and its center is marked by the intersection of laser points. The primary powerboard above has

its AMAC directly under the beam, while the secondary one is used to ensure that the irradiated AMAC does not inadvertently cause the adjacent powerboard to shut down.

Testing involves running two distinct DAQ software programs simultaneously. The primary function is to continuously cycle through and read chip data under the irradiation beam. The software package named powertools is utilized for the powerboard, which monitors all power outputs and collects data from the AMAC's registers. Additionally, ITk Strips DAQ (ITSDAQ) is employed for the hybrid, gathering all register data from the HCC and ABC chips, as well as physical packet data. With the comprehensive results obtained, we can ascertain both the location and the extent of the SEEs on the system.

3 Results

Since the DAQ software varies, the results for the powerboard and hybrid are distinct. This section will review all the results and attempt to find their underlying relationships.

3.1 System results

First of all, the total current is recorded to check the TID effect. The result is shown as Figure 2.

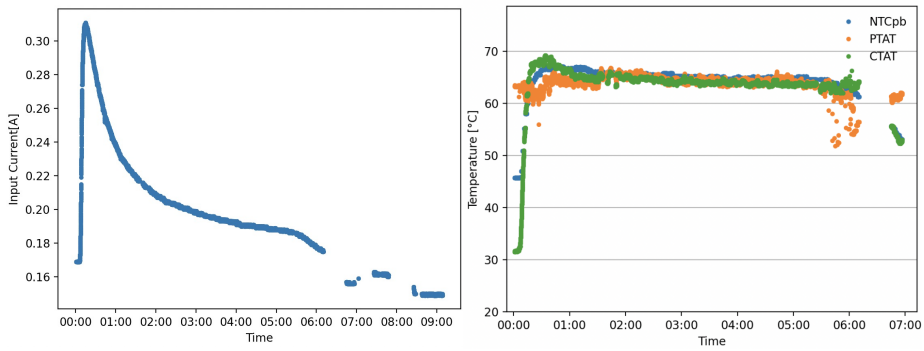

Figure 2. Current and temperature measured on two powerboards showing TID peak and stability during running.

The normal current should be 0.17A, but we observed that it peaks at 0.31A after several minutes, corresponding to approximately 0.35 Mrad. This indicates that our beam flux is excessively high. An optimal flux would allow the TID current to peak over several hours instead. The flux can also influence the magnitude of the TID peak. A current of 0.31A is nearly twice the normal level, which could also cause significant heating effects. This is evident from the temperature plot shown as Figure 2, where the temperature increases substantially due to the rising current.

3.2 AMAC results

The communication protocol used with AMAC, known as Endeavour, began to fail after about 6 hours. By examining data from AMAC, we observed a significant voltage drop in the powerboard output just before this occurred. This is illustrated in Figure 3 and could indicate that some component was being damaged.

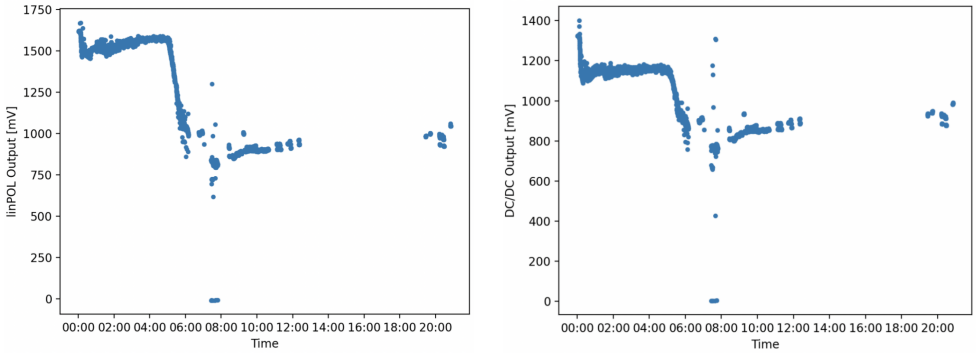

Figure 3. The output voltage of the Linear Point of Load regulator (linPOL) when the input is 12 V, which is a linear regulator used on the powerboard to power AMAC independent of the DC-DC converter.

The failing protocol began to show as increasing transformation errors, which initially could be rectified by power cycling and reconfiguring the ASICs. As more radiation dose accumulated, it resulted in complete failure, losing all communications whenever the beam was activated. After 20 hours, we had to proceed with the test without monitoring the AMAC, focusing solely on the hybrid.

On the other hand, the power function ceased functioning after irradiation reached 20.9 Mrad. Notably, the power output would automatically restore when the flux was reduced, suggesting that there exists a critical dose rate at which the power function fails. This issue occurred just 30 minutes after we ceased monitoring the AMAC. Consequently, we had to reduce the beam energy from 80 MeV to 70 MeV, which also decreased the dose rate from 2.60 Mrad/h to 0.57 Mrad/h. This adjustment is reflected more clearly in the hybrid's results.

Regarding the SEE effect, there was only one SEE on register 104, bit 20 (flipping from 1 $\rightarrow$ 0), which appeared to have no impact on the system. This incident underscores the effectiveness of TMR in protecting the AMAC against SEE, which is consistent with the results in TRIUMF [9].

3.3 Hybrid results

Both the ABC and HCC chips withstood the entire test. Nonetheless, during the TID peak, the system operated unstable. We observed various types of packet errors, along with numerous signal errors termed LCB errors.

Regarding the SEE effect, only one SEE occurred in both the ABC and HCC chips. In the HCC, it happened at register 48, bit 0, and in the ABC at register 3, bit 8 (both affecting the ADC), with changes from 0 $\rightarrow$ 1. Additionally, we were able to observe the frequency of SEE corrections by TMR in these two chips. This demonstrates that TMR provides effective protection for hybrid ASICs as well, which is consistent with the results before [7, 8].

Since ABC, HCC, and AMAC each had only one actual SEE during the irradiation test, and the total fluence was 2.52×10^{14}p/cm^2, the cross section of each of these three chips is 3.97×10^{-15}cm^2/p, we can calculate the rate of SEE, Rate$_{\mathrm{SEE}}$ is given by:

$$
\begin{aligned}
\mathrm{Rate}_{\mathrm{SEE}} &= \Phi_{\mathrm{hadrons}} \cdot \frac{\sigma_{\mathrm{SEE}}}{\mathrm{chip}} \cdot \frac{10^7\mathrm{s}}{\mathrm{year}} \\
&= O(10^7)\frac{\mathrm{hadrons}}{\mathrm{cm}^2 \cdot \mathrm{s}} \cdot \frac{\sigma_{\mathrm{SEE}}}{\mathrm{chip}} \cdot \frac{10^7\mathrm{s}}{\mathrm{year}} \\
&= O(10^7)\frac{\mathrm{hadrons}}{\mathrm{cm}^2 \cdot \mathrm{s}} \cdot O(10^{-15})\frac{\mathrm{cm}^2}{\mathrm{hadrons}} \cdot \frac{10^7\mathrm{s}}{\mathrm{year}} \\
&= O(0.1)\mathrm{SEEs/year/chip}.
\end{aligned}
\tag{3.1}
$$

As shown in [7], the expected hadron flux in HL-LHC is estimated to be $O(10^7)$ hadrons/cm^2/s, with the ATLAS detector estimated to operation for a duration of four months every year.

4 Conclusion

We have performed a system-level SEEs test on three ASICs developed for the ATLAS ITk Strip detector, which is slated for the Phase 2 upgrade in anticipation of the HL-LHC. The BETSEE test exposed all three chips to beams of protons in a setup mimicking detector conditions to enhance the assessment of possible SEEs that could affect detector functionality. BETSEE is notably sensitive to any issues stemming from chip interactions, unlike the single chip tests which do not account for these effects. The use of both real-time monitoring and post-test data analysis enabled quick responses and detailed examination, helping us detect a few SEEs. It is expected that the BETSEE will function effectively in the HL-LHC conditions, with each chip likely to encounter around $O(0.1)$ SEEs per year. The completion of these tests confirmed that SEEs would have minimal impact on detector functionality.

Acknowledgments

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