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Development of the ATLAS Liquid Argon Calorimeter Off-detector Readout Electronics for the HL-LHC

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Abstract: The High-Luminosity LHC will start operations for physics in 2030. The expansion of the dataset will be achieved by increasing the instantaneous luminosity of the LHC to 5-7.5 times its design value. For the ATLAS Liquid Argon calorimeter system, this poses new technical and operational challenges due to the higher radiation doses for the front-end electronics and increased pile-up caused by coincident and consecutive collisions. Additionally, the trigger rate of the first-level hardware trigger is projected to be increased to close to ten times its current value. At the same time, two new trigger subsystems must be provided with reconstructed energy data up to cell-level granularity in real time.

To keep up with these conditions and requirements while not sacrificing data quality, the Liquid Argon calorimeter readout needs to undergo a fundamental upgrade. The new off-detector electronics will be realized on custom ATCA-compliant boards based on FPGAs. A total of 278 new signal processing boards will receive the digitized data from 182 468 calorimeter cells at 40 MHz. They provide enough resources to facilitate the use of new online energy reconstruction algorithms and transmit the results to trigger and DAQ systems. A new timing system consisting of 30 additional ATCA blades will complement the new on-detector electronics by providing timing, monitoring and control functionality.

This article gives a summary on the planned off-detector electronics upgrades and the recent progress in firmware and hardware development.

Keywords: Calorimeters, Electronic detector readout concepts (gas, liquid)

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1 Introduction

As part of the ATLAS experiment [1], the Liquid Argon Calorimeters [2] are a system of sampling calorimeters encompassing a total of 182 468 cells in multiple layers. The calorimeters — divided into the electromagnetic barrel (EMB), electromagnetic endcaps (EMEC), the forward calorimeters (FCal) and hadronic endcaps (HEC) as shown in Figure 1 — use Liquid Argon (LAr) as active medium and lead, copper or tungsten as absorber material. Within the calorimeters, the incoming particles give rise to electromagnetic showers which deposit their energy inside the cells and leave an ionization trace in the liquid argon. This allows for the measurement of the position, energy and timing of the incoming photons, electrons, τ leptons and hadronic jets.

In the setup of the current run, the readout of the LAr calorimeters consists of two distinct readout paths. On the digital trigger path, energy values are sent to the trigger systems every bunch crossing (25 ns) at a reduced granularity of 34k supercells. This part of the detector readout electronics has been upgraded recently and was commissioned during the most recent long shutdown [3]. The data readout path is activated upon a trigger accept signal. Typically four digitized samples of the signal pulse are transmitted from the on-detector to the off-detector electronics at full granularity for energy and timing reconstruction on DSPs using an Optimal Filter approach [4], allowing for a sustained trigger rate of 110 kHz.

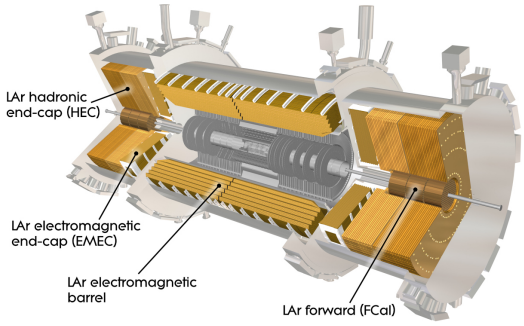

Figure 1. Overall structure of the ATLAS Liquid Argon Calorimeter system [5]

With the High-Luminosity LHC (HL-LHC), which is expected to start operation in 2030, the luminosity of the LHC will increase to up to 5-7.5 times its nominal value of $1 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The mean number of proton-proton interactions per bunch crossing will thus reach values of $\langle\mu\rangle \sim 140 - 200$. At the same time, the LAr calorimeters will likewise undergo an upgrade of the on-detector and off-detector electronics [6]. Beside the inherent need to replace the on-detector components due to the increased radiation levels in the detector area, a complementing upgrade of the off-detector components will allow for a better handling of the increased pile-up. The use of more sophisticated algorithms for energy reconstruction aims to maintain or improve the current energy reconstruction performance (Figure 2). The upgraded hardware should support a first-level trigger rate of 1 MHz and enables trigger decisions based on data at cell-level granularity.

In the following section, the current status, recent achievements and future plans for the new components of the LAr Phase-II upgrade (Figure 3) — in particular the new Liquid Argon Signal Processor (LASP) and its complementing Smart Rear Transition Module (SRTM), as well as the new Liquid Argon Timing System (LATS) — are presented in more detail.

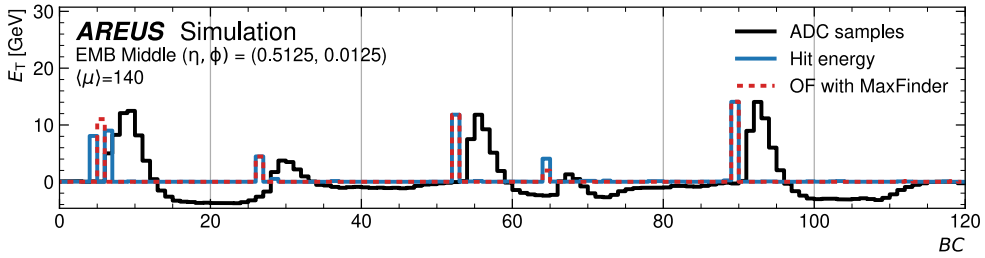

Figure 2. Performance of the currently used Optimal Filtering approach for energy reconstruction under HL-LHC conditions. For energy depositions in short succession, hit energies can be underestimated or attributed to the wrong bunch crossing. Adapted from [7]

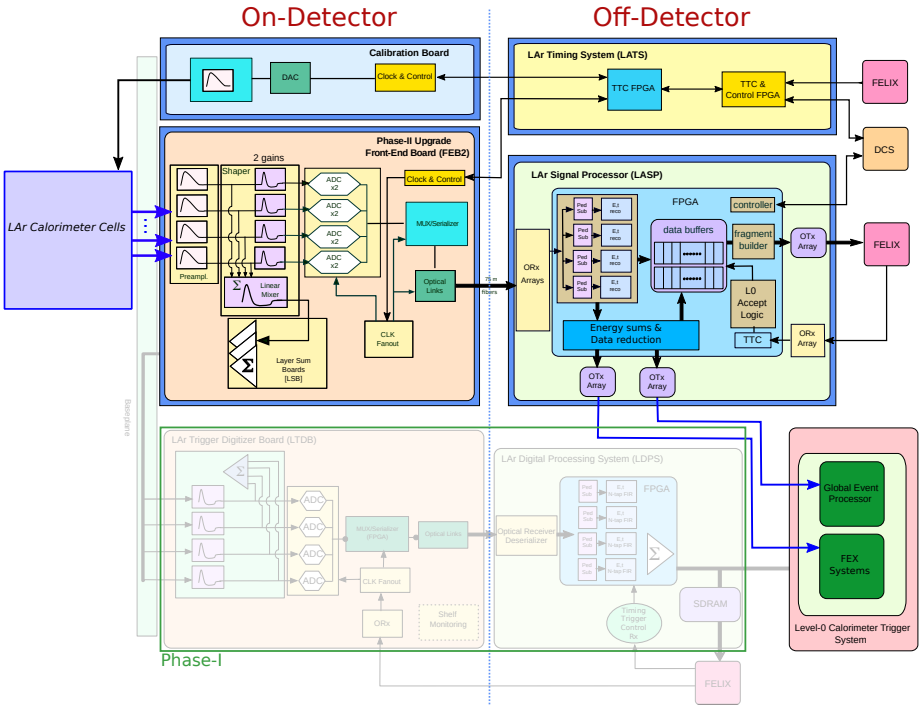

Figure 3. Plan of the LAr calorimeter on-detector and off-detector electronics for the HL-LHC. The systems shown on the upper half of the figure are going to be installed during the next long shutdown, while the shaded once are already operational. Adapted from [6]

2 Liquid Argon Signal Processor

The purpose of the Liquid Argon Signal Processor (LASP) is the calculation of energy and timing values as well as quality indicators for each energy deposition. The energy values are transmitted to two new parts of the ATLAS trigger system: the forward Feature EXtractor (fFEX) and the Global Event Processor (GEP). While waiting for a trigger decision, the data are buffered within the LASP and further transmitted to the data acquisition (DAQ) systems upon a trigger accept.

Hardware. The LASP system comprises a total of 278 Advanced Telecommunications Computing Architecture (ATCA) blades equipped with two Intel® Agilex™ 7 FPGAs each. One LASP blade receives data from up to 6 front-end boards, corresponding to up to 768 calorimeter cells, via Samtec

Firefly™ modules. The 66 unidirectional optical links have a data rate of 10 Gbps each. For the links to the fFEX and GEP trigger systems, with a data rate of 25 Gbps per link, Firefly™ modules are used as well. For the data path to the DAQ systems, three pairs of copper traces per FPGA towards an ATCA rear transititon module with link speeds of 10 Gbps are provided. Additional Ethernet connections allow for configuration, control and monitoring. Multiple testboards (Figure 4) with Intel® Stratix® 10 FPGAs have been manufactured and tested. Currently, the design of the next version of boards is being finalized and production is expected for the beginning of 2025. Besides moving from the Stratix® 10 to an Agilex™ 7 FPGA with more resources and higher achievable operating frequency for data processing, an improved clock distribution and JTAG scheme has been introduced. The preparation of a hardware testbench for verifying the power supply and for low-level tests of the high-speed interfaces of the blades is ongoing.

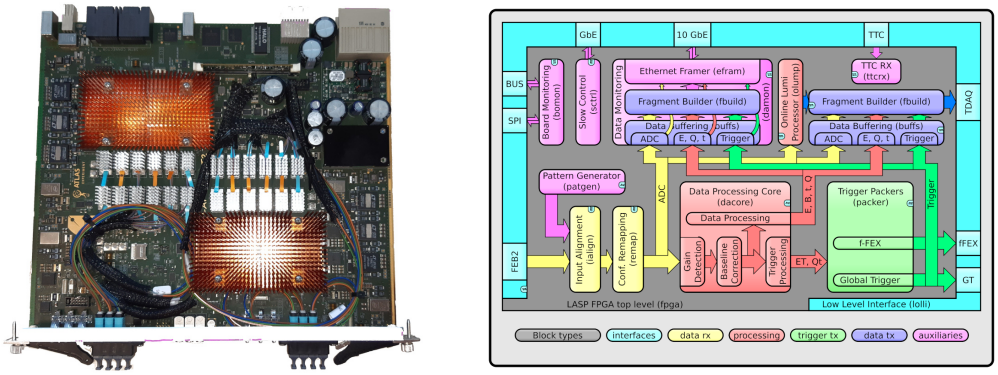

Figure 4. Left: LASP testboard. The ATCA blade prominently hosts two Intel® Stratix® 10 FPGAs and several Samtec FireFly™ modules for data reception from the new frond-end boards and for transmission to the hardware trigger systems. On the final boards, Intel® Agilex™ 7 FPGAs will be installed. Right: Schematic overview of the LASP firmware. The LASP provides output to the DAQ system as well as the trigger systems fFEX and GEP.

Firmware. On the FPGAs, multiple tasks are accomplished (Figure 4). First, the incoming data from the new front-end boards are received and decoded. They consist of 16-bit ADC values at two gains for each calorimeter cell, which are sent at every bunch crossing. The payload also includes an embedded bunch crossing identifier and comes encoded with the lpGBT protocol developed at CERN [8]. The data are then aligned in time to account for different delays on the individual fibers. Subsequently, the energy and timing values are calculated in the main processing stage which also includes the correction of a bunch crossing-dependent baseline and the selection of the optimal gain. Currently, different novel energy reconstruction reconstruction techniques based on Machine Learning are under investigation to replace the Optimal Filter [4] approach of the current readout. Under tight latency constraints of 150 ns, these methods show promising results in mitigating the increased pile-up noise under HL-LHC conditions [9, 10]. For transmission to the GEP a selection of the most energetic cells is performed while the cell-level granularity is kept. Furthermore, the energies of cells in the forward regions are prepared for transmission to the fFEX by a summation step. Eventually, the trigger data are formatted, encoded with the core1990/Interlaken protocol [11] and sent to the respective trigger systems. In order to compensate for the trigger latency of 10 µs,

the raw ADC values, the computed energy and timing values and the trigger data are buffered. Upon a trigger accept, they are finally sent to the DAQ systems. Control and monitoring of the boards is implemented via a memory-mapped interface based on the IPbus protocol [12].

3 Smart Rear Transition Module for LASP

For the main purpose of extending the IO capabilities of the LASP, the presented ATCA blades come with 278 complementing ATCA rear transition modules (SRTM) based on Xilinx® Zynq™ UltraScale+™ MPSoCs. The SRTM is responsible for receiving the TTC (timing, trigger and control) signal from the FELIX system and forward it to both LASP FPGAs. Similarly, the three data streams on the DAQ path coming from each LASP FPGA are merged into a single Interlaken/core1990 stream. For the reception and transmission of the aforementioned data, FireFly™ modules are used. The processor within the Zynq™ will run an OPC Unified Architecture (OPC UA) server to provide detailed board monitoring to the detector control system.

At the beginning of this year, the most recent version of the SRTM board (Figure 5) was successfully tested. On the firmware side, efforts currently concentrate on the integration and testing of the Local Trigger Interface (LTI) protocol and the DAQ stream merging.

4 Liquid Argon Timing System

The Liquid Argon Timing System (LATS) is responsible for the distribution of the TTC clock to the new front-end electronics boards. Additionally, it provides the 1524 new front-end boards with a bunch-counter reset (BCR) signal and delivers the calibration pulses to the 122 calibration boards. The LATS also acts as a bridge for the configuration and monitoring of the aforementioned boards.

The hardware of the LATS consists of 30 boards in ATCA format, called LATOURNETT, to be installed in shared racks with the LASP boards. Each board features 13 Intel® Cyclone® 10 GX FPGAs among which one *central* FPGA is connected to the upstream systems, and 12 *matrix* FPGAs provide connections to the on-detector boards. On the LATS-side, these links are based on Samtec FireFly™ modules. Two testboards have been produced and tested successfully (Figure 5). In the next iteration, the board will be supplemented with an additional passive ATCA RTM and an improved clock distribution and JTAG scheme. Having passed the preliminary design review, a production of four updated boards is planned for 2025.

A functional firmware is available for the LATOURNETT testboards, as well as for the Cyclone® 10 GX devkit for small-scale integration testing in the lab. For configuring and monitoring the on-detector boards, the capabilities of the lpGBT's internal/external control channels are harvested. The integration of the LTI protocol into the firmware is ongoing.

5 Integration

Recently, the first successful readout of a fully populated new front-end board via the LASP has been demonstrated. Besides, for the core1990/Interlaken link from the LASP towards the fFEX a test setup based on an Intel® Agilex™ 7 devkit and a Xilinx® Virtex™ UltraScale+™ devkit has been set up. Furthermore, on the software side, an OPC UA server is being developed to facilitate

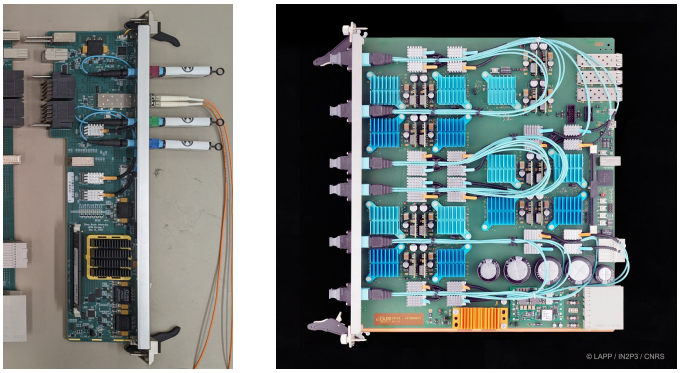

Figure 5. Left: SRTM v2.0 prototype. It connects to the LASP via the ATCA Zone 3 connectors. Right: Testboard for the LATS, called LATOURNETTv1. As the design is mainly limited by the number of high-speed transceivers, but not by FPGA resources, a solution with multiple low-range FPGAs was adopted. The next version of this board will be complemented by a passive ATCA RTM to ease routing and maintainability of the rear SFP+ and GbE connections.

controlling and monitoring of the LATS and through this the new front-end electronics. Similarly, the development of configuration, monitoring and debugging tools for the LASP is progressing.

The next integration milestone will be a test setup based on half of a Liquid Argon *front-end crate* — comprising a total of 14 new front-end boards, or 3584 ADC channels — attached to a Liquid Argon calorimeter mockup. The raw data will be aligned and buffered on the LASP board. Upon an accept signal, several hundred consecutive samples should be sent to an attached FELIX [13] machine. This test will be crucial to demonstrate that the entirety of analog and digital front-end board electronics, the clock distribution, configuration processes, the LASP boards and essential LASP firmware components work successfully. Equally, it helps to measure important properties of the analog side such as coherent noise, crosstalk, gain, and linearity.

6 Conclusion

The on-detector and off-detector electronics of the ATLAS Liquid Argon calorimeter system need to be upgraded before the start of the HL-LHC in 2030 to cope with the higher radiation doses, increased pile-up and to support a higher first-level trigger rate. In particular, the second phase of the off-detector electronics upgrade will provide the capacity for better real-time reconstruction algorithms and a more fine-granular readout on the trigger path. It also adds timing, monitoring and control for the new on-detector electronics boards. Testboards for all systems have been produced and evaluated, with new prototype boards being in the making. Recently, a first successful readout of a fully populated new front-end board prototype was demonstrated. Currently, the hardware and firmware is scaled up aiming at a readout of half of a front-end crate with 14 new front-end boards using the new off-detector electronics. Overall, the project is on track for the HL-LHC.

Acknowledgments

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