Prepared for submission to JINST

25th International Workshop on Radiation Imaging Detectors
30 June 2024 to 4 July 2024
Lisbon, Portugal

ATLAS Pixel Detector Overview

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Abstract: In the high-luminosity era of the Large Hadron Collider, the instantaneous luminosity is expected to reach unprecedented values, resulting in up to 200 proton-proton interactions in a typical bunch crossing. To cope with the resulting increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of the ITk will consist of a pixel detector, with an active area of about 13 m^2. To deal with the changing requirements in terms of radiation hardness, power dissipation and production yield, several silicon sensor technologies will be employed in the barrel and endcap layers. The ITk project is currently in the pre-production stage; sensors, modules, mechanical structures and services are being fabricated. The pixel modules assembled with ITkPix readout chips have been built to evaluate their performance and production rate. Irradiation campaigns were done to determine their thermal and electrical performance before and after irradiation. A new powering scheme – serial – will be employed in the ITk pixel detector, helping to reduce the material budget of the detector as well as power dissipation.

This contribution presents the status of the ITk-pixel project focusing on the lessons learned and the biggest challenges towards production. It will summarize the latest results on module assembly and testing. It will also present results from test beam campaigns.

Keywords: Detector physics: concepts, processes, methods, modelling and simulations, Detector readout concepts, electronics, trigger and data acquisition methods

Contents

1 Introduction

The High-Luminosity Large Hadron Collider (HL-LHC), which should be operational from the beginning of 2029, will allow physicists to study New Physics in greater detail. This will be achieved by upgrading the Collider systems to reach an instantaneous luminosity of $5-7\times10^{34}\,\mathrm{cm}^{-2}$, which is five times the LHC's design value and provide up to 200 interactions per bunch crossing (25 ns), extending the dataset from about $300\,\mathrm{fb}^{-1}$ by the end of LHC run to about $4000\,\mathrm{fb}^{-1}$. The ATLAS detector will be upgraded in order to face the challenges of radiation hardness, track multiplicity and increased data rates posed by the HL-LHC. The Inner Detector (ID), which is the closest to the interaction point, will be replaced by an all-silicon Inner Tracker (ITk) with silicon strips and hybrid pixel detectors.

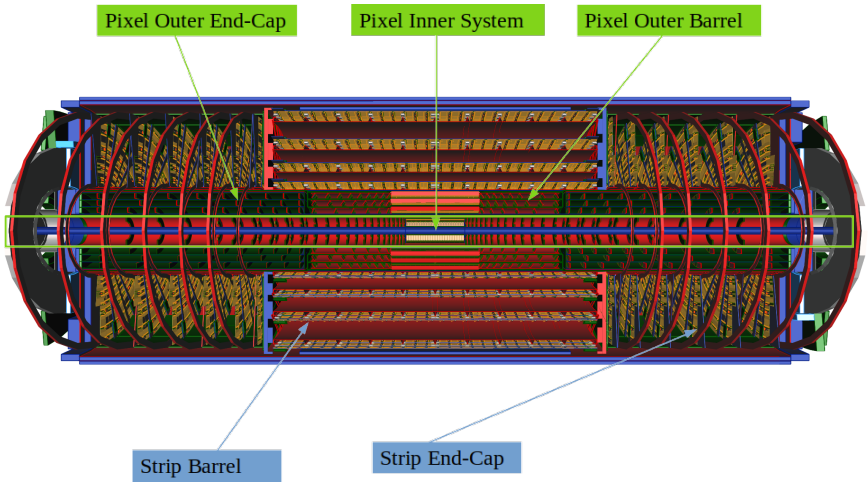


Figure 1: Rendering of the ATLAS ITk Pixel Detector is shown inside the green box, surrounded by the Strip Detector. The Pixel Detector consists of the Inner System, the Outer Barrels and the End Caps Rings [1].

2 ITk Pixel Detector Layout

Figure 1 shows the ITk Detector comprising of the Strip layers and the Inner System of the Pixel Detector which is the focus of this work. It consists of five silicon tracking layers split into three regions: the Inner System (IS), Outer Rings (OR) and Outer Barrel (OB), covering pseudo-rapidities up to $\eta = 4$. The Inner System consists of the Barrel with flat staves (L0, L1) and Ring layers (R0, R0.5, R1) which are replaceable owing to the harsh radiation environment. About 9600 modules are required to cover an area of 13 m^2. Figure 2 depicts a quadrant of active detector elements and their pseudo-rapidity coverage.

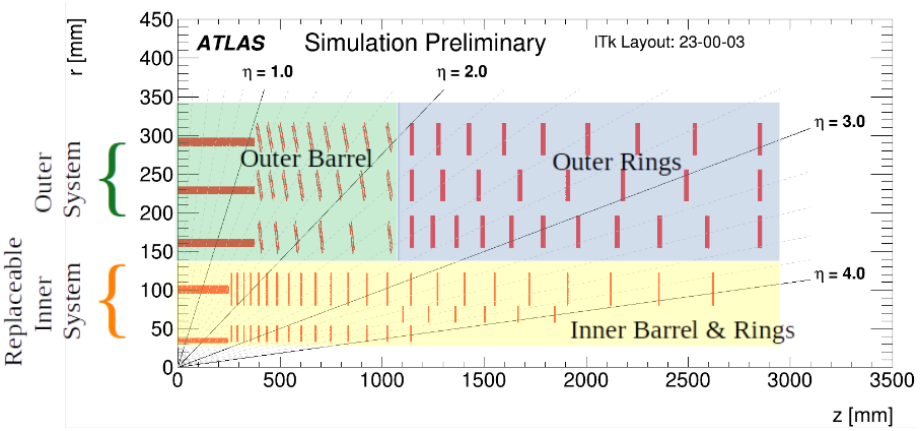


Figure 2: ITk Detector Layout. Enclosed in the yellow box is the Inner Barrel & Rings, the green box shows the Outer Barrel and in the blue box are the Outer Rings [2].

3 Pixel Module: Sensors and Readout Chip

The fundamental building blocks of the ITk Pixel Detector are the pixel modules. The core of all modules are the hybrids, which consist of pixelated sensors bump-bonded to one ore more readout chips, see figure 3. Each ASIC is composed of a pixel matrix of 400 rows and 384 columns where the signal of the corresponding sensor pixel is processed. The hybrid detectors are referred to as bare modules which are glued onto a flexible printed circuit board which, after wire-bonding, provides all the electrical connections needed to operate the device.

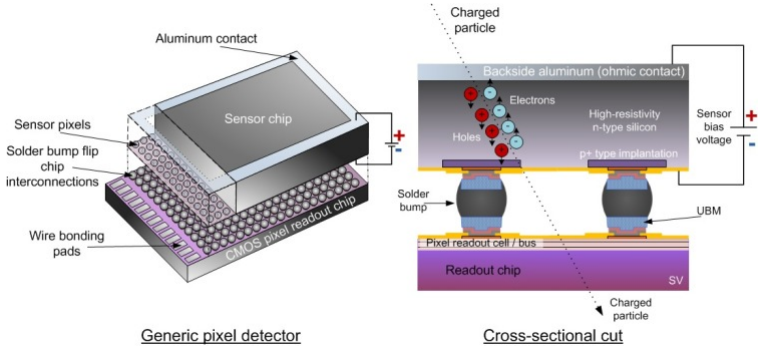
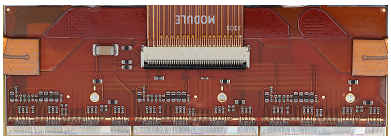


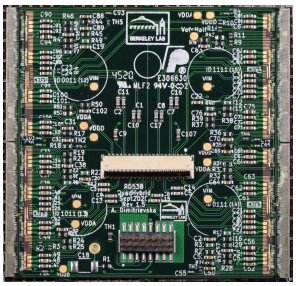
Figure 3: Exploded view of a generic pixel detector is shown on the left. The cross-sectional cut of a hybrid pixel detector is shown on the right [3].

ITk will use different configurations of pixel modules in the three regions of the detector. Figure 4 shows the three configurations.

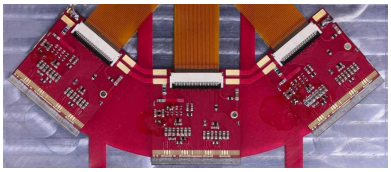
- Quad modules in the outer system (OS), composed by a planar n-on-p silicon sensor bump-bonded to 4 readout chips.
- Quad modules in the second innermost barrel layer (L1) and rings (R1).
- Linear triplets in the innermost barrel layer (L0), composed by $3 \times (50 \times 50\ \mu m^2$ pitch) 3D silicon sensors.
- Ring triplets in the innermost ring layers (R0, R0.5), composed by $3 \times (25 \times 100\ \mu m^2$ pitch) 3D silicon sensors.



(a) L0 Linear Triplet module – 3 readout chips



(b) Quad module

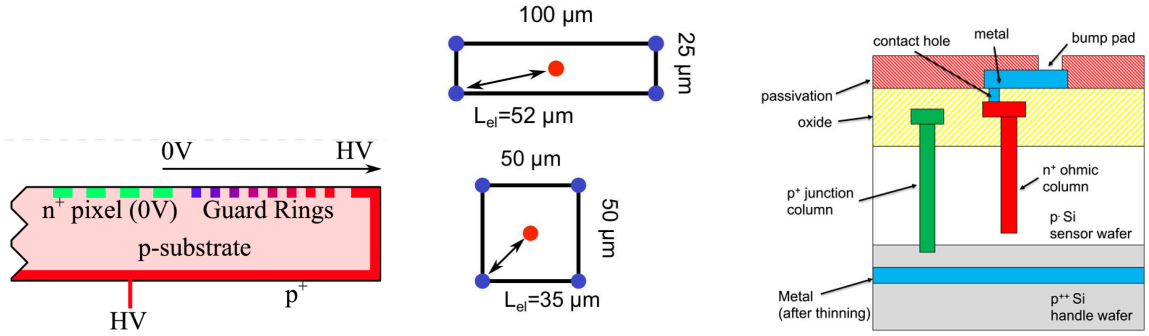


(c) R0 Ring Triplet module – 3 readout chips

Figure 4: From the left to right, figure shows assembled Linear triplet, Quad and Ring triplet (R0) modules.

3.1 Sensors

Extensive R&D has been conducted to design silicon sensors capable of withstanding the intense radiation levels of the HL-LHC. Two silicon pixel sensor technologies will be used: *Planar* and *3D*. Figure 5a depicts the schematic of a planar sensor with n-in-p silicon technology with a pixel pitch of 50×50 μm^2 which has been shown to be radiation hard up to 5×10^{15} n_{eq}/cm^2 [2]. Quad Modules with 100 μm thickness (active) sensors will be used in the IS layer L1 and Quad Modules with 150 μm thick sensors for the OS. The planar sensors will be manufactured by HPK, Micron and FBK.



(a) Schematic of planar sensor.

(b) Two geometries of 3D sensors.

(c) Schematic of 3D sensor.

Figure 5: Pixel sensor schematics and geometry [4].

The 3D sensors for ITk are designed to withstand fluences of up to about 2×10^{16} n_{eq}/cm^2 and have an active thickness of 150 μm. Two different configuration of 3D sensors will be used: 50×50 μm^2 pitch for the Rings and 25×100 μm^2 for the Barrel L0 (see figure 5b). SINTEF and FBK have been selected as the vendors for the 3D sensors.

3.2 ITkPix Readout Chip

The readout chip designed by the RD53 Collaboration is produced in the 65 *nm* CMOS technology and has a pixel pitch of 50×50 μm^2 with a pixel core of 8×8 pixels. This core design is stepped and repeated to make a pixel matrix of 400×384 pixels. The chip-bottom area contains all the global chip functionalities with a complete system-on-chip including power management and sophisticated digital communication (sensing as well as monitoring). The chip features a differential front end which provides 4-bit charge measurement per pixel (ToT) and can operate at a minimum threshold of 600 e^-. It also provides four data links per chip at 1.28 Gb/s. The ITkPixV1 and V1.1 were the first full size prototypes used for the pre-production stage. The ITkPixV2.0 is the final version of the chip that has been developed with improvements for production.

3.3 Serial Powering Scheme

To reduce the material budget, a serial powering scheme will be employed. ITkPix chips, equipped with Shunt-LDO regulators, can maintain stable voltages with a constant current. Modules will be powered in series with a constant current, while the chips on each module will be powered in

parallel. This setup enhances reliability, ensuring continued operation even if individual chips fail. The powering technique guarantees smooth performance regardless of load variations or voltage drops. By shortening power cabling and reducing material, the mass of services and auxiliary electronics is minimized, meeting the stringent physical constraints within the service channels. Figure 6 presents a system test conducted to evaluate serial powering along with a schematic illustrating the setup. Up to eight Quad Modules were powered in series with constant current. Mild transient effects were observed in the serial power chain but no substantial issues were found.

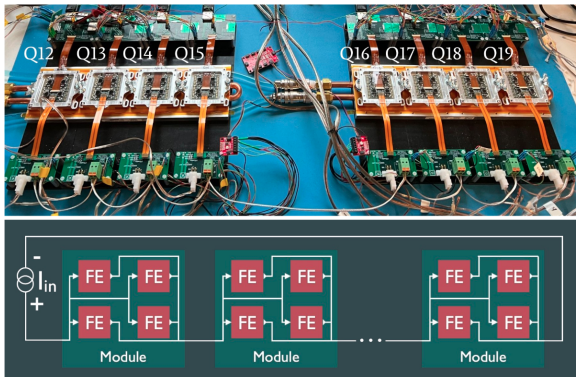
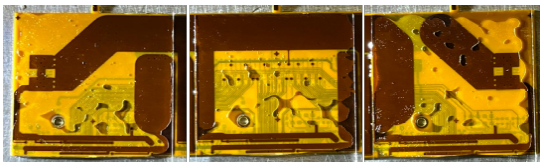


Figure 6: The bottom image illustrates the schematic of the Serial Powering setup, while the top image depicts a System Test conducted using Quad Modules [5].

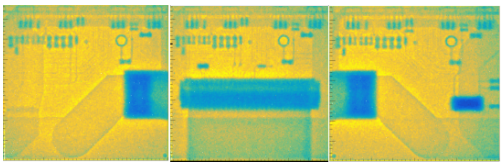
4 Module Assembly and Testing

A module is constructed using so called bare modules, composed of a sensor bump-bonded to a readout chip. These bare modules are then attached to flexible PCBs with adhesive, followed by wire bonding to create the required electrical connections. In the case of a Quad module, a single large sensor is bump-bonded to four readout chips and mounted onto the flexible PCB.

For the assembly of triplets, three individual Bare Modules (each consisting of a sensor and a single readout chip) need to be assembled and wire-bonded. Given the stringent constraints on triplet width and geometry, each component undergoes rigorous metrology, visual inspection, and quality control prior to assembly. During the assembly process, precise alignment (within a $\sim 50\ \mu$m tolerance) and accurate glue application are crucial. Figure 7a illustrates studies performed on glue distribution and deposition using glass dummies to meet strict specifications. After assembly, additional metrology is conducted to ensure the triplet meets the required specifications. After the modules are wire-bonded, consistent electrical quality control tests are performed both at room temperature (20°C) and cold temperature (−25°C). These tests include scans to evaluate the digital and analog functionalities of the front-end chip, equalization of the pixel threshold, dedicated scans and using radiation sources to detect bump disconnections between the sensor and the readout chip. Figure 7b shows the pixel occupancy map obtained during a source scan. Yellow indicates the highest hit rates, while blue represent lower hit rates particularly around the SMD components and electrical connectors. Thermal cycles were also conducted to stress the bumps and to determine if the modules can withstand the repeated temperature fluctuations and mechanical stresses expected during their operational lifetime.



(a) Image from glue deposition studies with glass dummies.

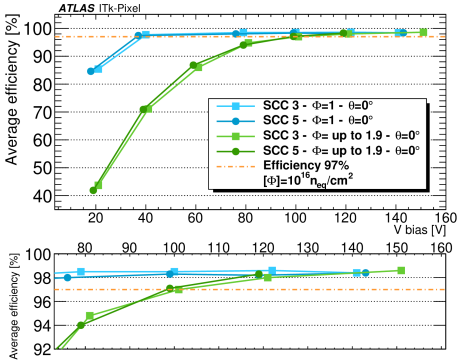


(b) Pixel occupancy map of the triplet obtained from Source Scan performed with ^{90}Sr source.

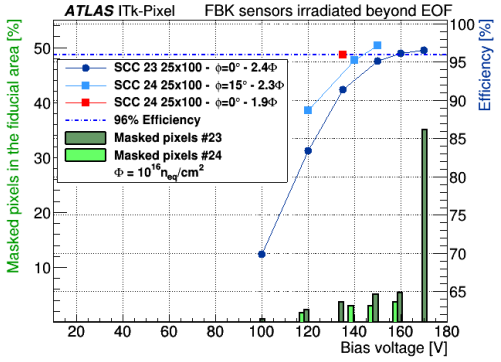
Figure 7: Glue deposition tests and Source Scan of a triplet module

5 Test Beam Results

Multiple test-beam campaigns were carried out to assess module performance and evaluate the track reconstruction capabilities of the different module designs before and after irradiation. The results of the FBK 3D sensors with 50×50 μm^2 and 25×100 μm^2 geometries are presented in figure 8. The maximum hit efficiency requirement for irradiated sensors is 97 %. The results (figure 8a) demonstrate that this requirement is met at 40 V for sensors irradiated up to 1.0×10^{16} n_{eq}/cm^2 and at 100 V for sensors irradiated up to 1.9×10^{16} n_{eq}/cm^2. Figure 8b indicates that 25×100 μm^2 3D sensors meet the requirement at 130 V for a fluence of 1.9×10^{16} n_{eq}/cm^2 and at 160 V for a fluence of 2.4×10^{16} n_{eq}/cm^2. It also shows that the percentage of masked (noisy) pixels remains below 3 % at voltages up to 150 V.



(a) Module efficiency at different fluences versus bias voltages for the 50×50 μm^2 3D sensors. [6]



(b) Module efficiency at different fluences versus bias voltages for the 25×100 μm^2 3D sensors. [7]

Figure 8: Module efficiency plots obtained during tests with particle beams at CERN/DESY

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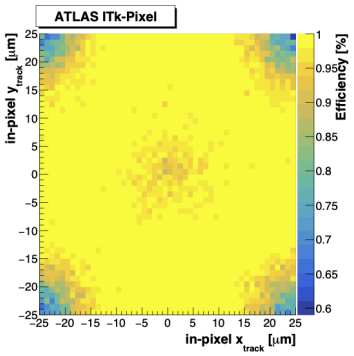
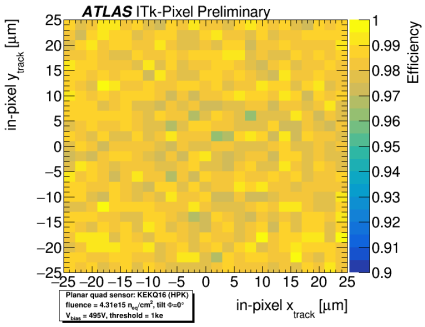
Pixel cell efficiency maps for the 3D and planar sensors are also presented. The SINTEF 50×50 μm^2 3D sensor irradiated up to 1.0×10^{16} n_{eq}/cm^2 reaches 97 % hit efficiency at 40 V. Figure 9a indicates that hit efficiency is reduced in the pixel-cell corners and center due to the presence of the readout electrode columns. These results are obtained with perpendicular particle tracks which is the worst-case scenario. In the actual detector, most tracks will strike at an angle, thereby improving efficiency in the electrode regions. Figure 9b shows the hit efficiency of a HPK 150 μm thick planar sensor which was irradiated up to 4.31×10^{15} n_{eq}/cm^2 reaches the requirement of 97 % at 400 V with uniform efficiency over the pixel surface.



(a) Pixel cell efficiency of SINTEF 3D sensor. [8]



(b) Pixel cell efficiency of HPK planar sensor. [9]

Figure 9: Pixel cell efficiency maps obtained during tests with particle beams at CERN/DESY

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6 Conclusion and Outlook

The ATLAS ITk is an all-silicon detector set to replace the current inner detector. It is designed to handle the increased luminosity anticipated with the HL-LHC Phase II upgrade. Sensor pre-production has been completed and sensor production is underway. Module pre-production is in the final stages and production is expected to start by end of 2024. System tests and demonstrators for all sub-systems have been prepared using prototype modules. The delivery of the final production version of the ITkPixV2 readout chip has already commenced. Services, loading, and integration procedures are being finalized. All member institutes of the ATLAS ITk-Pixel collaboration are transitioning from pre-production to production, with the goal of having the upgraded ITk installed and operational by 2029.

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