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EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN DRDC/93-54
RD19 Status Report
1 January 1994

RD19: Status report on 1993
Development of hybrid and monolithic silicon micropattern detectors

Spokesman: Erik H.M. Heijne

CERN[1], Collège de France[2], CPPM Marseille[3], EPFLausanne[4], ETH Zurich[5], IMEC Leuven[6], INFN and University of Bari[7], Genova[8], Milano[9], Modena[10], Padova[11], Pisa[12], Roma[13], Trieste[14], University GHS Wuppertal[15], Technical University Athens[16], Group Praha[17], Univ. of Glasgow[18], Canberra Semiconductor NV[19]¶, GEC-Marconi (Caswell)[20]¶ and Smart Silicon Systems SA[21]¶

F. Anghinolfi[1], F. Antinori[1], H. Beker[13], D. Barberis[8], K. Bass[20]¶, G. Batignani[12], W. Beusch[1], V. Bonvicini[9], V. Bonzom[3], L. Bosisio[12,14], C. Boutonnet[2], P. Burger[19]¶, M. Campbell[1], P. Cantoni[10], M.G. Catanesi[7], E. Chesi[1], C. Claeys[6], J.C. Clemens[3], M. Cohen Solal[3], G. Darbo[9], J.C. Da Silva[3], C. Da Via[1], I. Debusschere[6], P. Delpierre[2,3], D. Di Bari[7], S. Di Liberto[13], B. Dierickx[6], D. Elia[7], C.C. Enz[4], E. Focardi[12], F. Forti[12], Y. Gally[3], M. Glaser[1], T. Gys[1], M.-C. Habrard[3], G. Hallewell[3], E.H.M. Heijne[1], L. Hermans[6], J. Heuser[15], P. Inzani[9], A. Jacholkowski[7], J.J. Jæger[2], J. Jakubek[17], P. Jarron[1], P. Jirousek[17], S. Kersten[15], F. Krummenacher[21]*¶, R. Leitner[17], F. Lemeilleur[1], V. Lenti[7], M. Letheren[1], M. Lokajicek[17], L. Lopez[1], D. Loukas[16], M. LoVetere[9], M. Macdermott[5], G. Maggi[7], V. Manzari[7], P. Martinengo[1], G. Meddeler[1], F. Meddi[13], A. Mekkaoui[3], P. Middelkamp[1,15], M. Morando[11], A. Munns[20]¶, P. Musico[8], P. Nava[10], F. Navach[7], M. Pallavicini[9], F. Pellegrini[11], F. Pengg[1]†, M. Pindo[9], S. Pospisil[17], R. Potheau[3], E. Quercigh[1], N. Redaelli[9], J. Ridky[17], L. Rossi[8], K. Safarik[1], D. Sauvage[3], G. Segato[11], F. Severi[9], S. Simone[7], K. Smith[18], B. Sopko[17], G. Stefanini[1], P. Tempesta[7], G. Tonelli[12], G. Vegni[9], H. Verweij[1], G.M. Viertel[5], V. Vrba[17] and J. Waisbard[2]

* Also with EPF Lausanne, Switzerland,
† Fellowship Austria
¶ The companies Canberra, GEC-Marconi and SSS are not formally member of the collaboration

Summary

In 1993 we have demonstrated in a collaboration with the Omega WA97 experiment the first 29 cm^2 hybrid pixel array with 72576 contiguous sensor elements, each coupled to an electronics cell with binary output. This array uses an improved version of the CMOS readout chip (Omega2) with 1024 cells of 75 μm x 500 μm. The tracking precision was 20 μm and the noise hits $<<10^{-6}$, with 2% dead area on the first array. We also operated in another beam test 150 μm thick detectors at 98% efficiency which is possible because of the very low noise level of pixel detectors. The absolute value of the Equivalent Noise Charge ENC has been determined to be 170 e^- r.m.s. ± 30 e^- using a ^{109}Cd radioactive source. This isotope emits photons at 22 and 25 keV which could be well separated in a differential threshold scan for single pixels. The same readout chip has been bonded to a special matrix detector with thin, transparent window in order to study the sensitivity of this silicon matrix to low energy electrons and light for scintillating fiber detector readout.

For the Delphi Very Forward Tracker the development work focussed on large bump bonding, on a sparse readout scheme and on bus structures integrated onto the high-resistivity silicon detector.

In the Silicon-On-Insulator (SOI) monolithic technology the design of a new mask set including an array of detector diodes with associated electronics has been completed in August. Production of SIMOX and BESOI wafers is expected to be ready in June 1994.

Comparative studies of various readout architecture schemes for the LHC p-p experiments have been started. Submicron technologies are being evaluated for use in this next phase.

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1. INTRODUCTION

The micropattern particle detector is a semiconductor pixel device that consists of a matrix of contiguous particle sensing elements with dimensions between ~10 µm and ~500 µm which have an individual signal pulse amplifier, comparator, memory, etc. with similar cell size connected to each sensor element. The matrix ultimately will have an intelligent readout architecture that provides the user with a pattern (true 2-dimensional coordinate information) of the hits at every chosen timeframe. RD19 aims at development, demonstration and possibly implementation of micropattern pixel detectors in one or several LHC experiments. Discussions on the application of the micropattern detectors in the inner vertex and tracking detectors of ATLAS, CMS and the heavy-ion collaboration ALICE are conducted in parallel with continued generic technical development. The goals of the R&D are still more determined by general technological considerations than by differences in requirements between these potential users. They all can benefit from a common effort, keeping in mind that making devices of the projected sophistication is straining resources, in particular concerning personnel beyond those available presently in the particle physics community.

We have to show that an active pixel detector matrix can be made at all, that it can be made large in size, that it can be made thin, that it can be made with MHz detection frequency at low power and then that all this can be made radiation hard as well. The acceptable cost will be a function of the proven benefits of this detector and of the importance of tracking requirements in the overall experiment philosophy. A significant fraction of the overall cost is already in the development itself which stretches over many years and necessarily involves in each phase the production of sizeable quantities of devices, in order to evaluate reliability and yield factors. Therefore, it is useful to ally each development step to an application in a running experiment, if this proves possible.

2. 1ST PHASE, DEVELOPMENT OF A DETECTOR FOR FIXED TARGET

We started working in 1987 on the design of both a monolithic and a hybrid version. In the latter the detector elements and the readout circuits are implemented on different substrates, coupled via microscopic bump bonds. The hybrid devices mostly incorporate available technology and this approach proves to be faster than the technological development needed for the monolithic detectors. After initial tests of the first hybrid silicon pixel detector in the heavy-ion experiment WA94 at the end of 1991 we have improved the readout chip in order to make it compatible with an array of many chips. This array was designed and fabricated in collaboration with experiment WA97. Two arrays together cover hermetically an area of 53 mm x 55 mm. The operation of the first arrays is described in an article "72k element array" in the appendix. We now have shown that devices can be made and that they can be made in large arrays.

3. OTHER USES OF THE 'OMEGA' READOUT CHIPS

Besides the operation of the first array other major achievements in 1993 are the measurement of the absolute value of the noise of the pixel electronics: 170 e^- r.m.s. ± 30 e^- using a ^{109}Cd radioactive source (fig. 1, Wuppertal), the test of thin detectors of only 150 μm (fig. 2 and fig. 22 in the "72k article", Wuppertal and Prague) and the study of the sensitivity of the pixel detectors to electrons in vacuum (Gys) and visible light (fig. 3, DaVia and Stefanini). These measurements also used the Omega readout chips. A complete list of all publications, technical notes, etc. in the framework of RD19 can be found in the appendix.

4. SILICON-ON-INSULATOR MONOLITHIC DETECTORS

After the preliminary positive results obtained with SOI devices, published at the end of 1993, there was discovered a significant problem of cross talk between the logic and the amplifier inputs. The choice of a different SOI process using bond-and-etchback (BESOI) wafers and extensive simulations of technology have led to an improved process flow which offers design options that were not available previously. An implanted shielding layer can be produced in the high resistivity silicon before the SOI insulating layer is created, as shown in fig. 4. Improved SPICE parameters were extracted from the transistors made in the last run. These enabled more precise design and the implementation of checking logic in the CADENCE simulator has reduced the risk of errors in the designs that are now in the processing cycle. A matrix of 16 x 32 cells has been designed with pixel size 100 μm x 500 μm resulting in a senstive area of 3.2 x 8.0 mm^2. An extensive set of test structures should enable understanding of possible problems that may be found once the wafers are available, in Summer 1994.

5. DELPHI PIXEL DETECTOR FOR THE VERY FORWARD TRACKER

A Delphi group is developing for the Very Forward Tracker pixel detector a sparse readout scheme, bus lines on the detector substrate and large bump bonds. A drawing of the Delphi pixel detector module with integrated bus lines is shown in fig. 5 and a first prototype has been tested in November in a test beam. A part of this prototype was adapted to the CDF_Sparse4 readout chip and another part featured a number of test structures for evaluation of the bonding with large bumps. The 2 different, final readout chips will be new versions of the CDF_Sparse4. There is some concern about the radiation resistance of these chips which are still made in the SACMOS3 technology, originally chosen for its exceptional density and well-known analog characteristics. Alternatives are being studied. The Delphi development work is now organizationally and financially independent of RD19 but exchange of information is taking place.

6. ANALOG PIXEL DETECTOR DEVELOPMENT (ANAPIX)

The linear array of 8 analog pixel cells has been connected by wirebonding to a silicon microstrip detector with 10 mm long strips at 50 μm pitch. Without external capacitance an equivalent noise charge ENC of 105 e^- rms has been measured and with the detector connected this is 200 e^- rms. An improved noise performance can be expected if the circuit will be bump-bonded to the detector matrix. This will be possible once a full readout chip has been implemented. It is planned to design this new chip during 1994 in the SACMOS1 technology.

7. OTHER STUDIES

Several other studies have been undertaken in the framework of RD19 itself or in association. A study was made of the ZMR-SOI optimization. Silicon detector processing has been studied in Modena. Pixel detector capacitance calculations and measurements were done in Athens and Pisa (partly at LBL). The light detection studies have been mentioned already in sect. 3. as well as the vacuum studies. A few assembled silicon detectors were tested after heating in vacuum to 350 C and they still performed well even though the solder bumps have been some time above the melting point (183 C). Finally, in a collaboration with Glasgow they have started preparation of bump bonding and design work on a GaAs pixel detector that is compatible with the existing readout chips.

8. THE PHASES IN DETECTOR DEVELOPMENT FOR LHC

Although the pixel detector development at CERN has been going on already for ~7 years it has seen some 'stop-and-go' in the beginning. Some important steps have been made but many questions remain to be solved. There may be ~5 years until final commitments have to be made for installation in the initial setup for an LHC experiment and these years have to be used to reach satisfactory technical performance and economical production methods.

In a previous status report we distinguished several phases in the development:

1. Multi-chip array operational in fixed target experiment (now practically done).
2. Improvements in architecture and timing compatible with collider operation at 'low' frequency, e.g. at LEP or HERA, using submicron technology for first time. The detector arrays made in this phase might already prove to be suitable for a LHC heavy ion collider experiment.
3. Implementation of final specifications in a prototype for p-p operation at high luminosity in LHC.
4. Radiation-hard prototype with performance as in phase 3.

These phases are not necessarily sequential in time. E.g. some radhard studies are already going on but the technology performance needed in the radhard process can only be defined once the functions of the readout electronics are fully understood. On the other hand, an early understanding of the radhard processes available may help in finding realistic solutions for the desired functions. In this respect a certain number of iterations have to be allowed.

Phase 2 can be expected to need 2 iterations in design and chip production as well as some preliminary test circuit runs. The first useful detector arrays can be available realistically in the course of 1995 or early 1996. Devices produced in this phase 2 probably should be used also in prototype studies that are being prepared for the p-p experiments, e.g. the Barrel Sector Prototype (BSP) for the inner detector of ATLAS.

It is difficult to define with precision already now the planning of phase 3 and phase 4. This will depend on the progress in phase 2 and on the technology development in industry. It is likely that phase 3 will use 0.5 μm CMOS which is announced for 1995.

Readout architecture studies

In table 1 several distinct approaches to the readout architecture are compared.

TABLE 1 Comparison of some Pixel Readout Architectures

	architecture	fast clocks in pixels?	data driven?	broadcast lines in active matrix	systematic inefficiencies	critical items
	1	2	3	4	5	6
A	event/time stamp ("LBL")	NO	YES	1 out, 3 in	if >7 events p col	output fast OR
B	pulse delay/width (Darbo)	NO	YES	-	contiguous cells/events	delay => BCO
C	strobed (Ω-Campbell)	NO	YES	trigger/strobe	may pick up other BCO	precision on delays in pixel
D	sparse scan (Delphi-Jaeger)	NO	YES	col + row	ghosts from out-of time BCO	fast broadcast lines
E	synchr hit addr shift (CPPM)	YES	NO	continuous clock	loss~0.064%	clock noise

Of the architectures mentioned 2 have been already implemented in existing chips: C is used in the Omega2 array and is discussed in detail in the appendix, while D is used in the CDF_SPARSE4 chip for the Delphi VFT. Test chips for study of the architecture E have been designed and are in processing. Critical parts of architectures A and B will probably be implemented and studied in the SACMOS1 technology during 1994. All architectures have to be evaluated and improved where possible in alternative Phase 2 chips, in order that a choice can be made for the Phase 3 design.

Engineering studies for cost reduction in processing and testing

In collaboration with GEC-Marconi Materials Ltd (Caswell) we have prepared a study of the application of automatic equipment in the bump bonding processing. Apart from technical problems we also have to solve procedural aspects. The projected number of devices for LHC and the expenditure involved are relatively small in view of usual investment cost of semiconductor processing equipment.

Another study is in preparation for possibly cheaper alternatives for the high-resistivity detector substrates.

As the yield of acceptable devices will be the main factor in the production cost it is important to study test procedures and testability at an early stage. Industrial standards have to be respected and contacts organized with commercial test houses. In order to have realistic evaluations it will be needed to use fairly sizeable batches, even in the R&D stage. The devices thus produced could be put to good use in an experiment.

9. MILESTONES

The milestones which we had set for 1993 have been amply met. Due to constraints of money and manpower it was not possible to do any significant work within RD19 on the additional milestone concerning a radhard pixel circuit. However, some design work has been done at CPPM on a pixel front-end circuit in radhard technology and results may be know later. In RD9 some of us have worked on implementation of amplifier and memory circuits but as long as the details of simulation are not yet fully understood there is little point in making circuits of the pixel type which usually go through lengthy optimization.

Objectives of the R&D plan for 1994

We foresee implementation of a readout chip and a "bus"/readout chip in the 1 µm SACMOS technology. These chips will have to be compatible with a Multi-Chip-Module detector substrate and different readout architectures will be considered as discussed above. The radiation hardness of SAC1 will be evaluated. First indications suggest hardness up to several 100 krad which may in fact be sufficient for heavy-ion experiments in LHC.

Improvement in bump bonding technology and smaller bump size (20 µm) will be studied.

Detector development will focus on thin detectors, integrated bus lines and solutions for cross talk problems.

A new SOI run will be finished and the resulting devices can be studied.

The collaboration with WA97 will continue and several arrays will be installed in the heavy ion experiment. This will allow statistical data on performance and production.

The Delphi pixel collaboration under responsibility of P. Delpierre will pursue similar goals in parallel and plans are to have the full detector array ready early in 1995.

10. CONCLUSION

After the first operation of a realistic, multi-chip array the applied physicists and engineers can confirm the feasibility of the silicon micropattern detectors and the particle physicists can begin to evaluate the benefits in using such devices in experiments. The low noise performance allows very clean tracking even in the busy environment of heavy ion experiments. The true 2-dimensional nature of the data will provide space points without ambiguities and therefore pattern recognition will be quick and very efficient in computing power. The binary readout reduces the amount of data and the processing time in comparison with analog systems while a precision of $<15\ \mu m$ will be achieved with the pitch of $50\ \mu m$. In the recent tests with detectors of $75\ \mu m$ pitch a precision of $20\ \mu m$ has been measured for single hits and $< 10\ \mu m$ for double hits. Noise hits occurred at a rate $<<10^{-6}$ of the hits from reconstructed beam tracks and some part of these spurious hits can be attributed to real ionizing events.

Early assesment of strong points of these detectors is important in order to use them optimally in the overall experiment strategy in LHC. The weak points also should be discovered in time to allow changes to be made to the readout chips, the detector modules or the manufacturing procedure before the phase of the final prototype, well before major commitments are made for production. One should be aware that each iteration in chip and detector development and evaluation takes between 1 and 2 years. With one phase completed of the 4 mentioned in sect. 6 each following phase has to coincide practically with only a single iteration.

In spite of a potential 'diversion' it has been shown to be beneficial to link intermediate phases in the long-term detector development with short-term applications in running experiments. This provides a stimulus for a realistic approach and feedback to the design process. It provides additional financing which supports the study of feasibility and improvement of yield in the industrial manufacturing and testing of a larger number of devices than would be possible in a pure development project.

Acknowledgments

It is a pleasure to acknowledge the effective work of our industrial partners.

11. ACCOUNTS AND BUDGET

The 1993 expenditures on micropattern detector development in RD19 have been covered by partcipating institutes, CERN and the Omega WA97 experiment. The planned budget for RD19 in 1994 amounts to 750 kSf of which 250 kSf is requested from CERN. An additional amount of money is requested separately for the acquisition by CERN of a semi-automatic flip-chip alignment and bonding machine which will have to be operated in collaboration with industry. Omega will assume the production cost of items directly related to the arrays which it will use.

REFERENCES

A list of RD19 publications and other papers related to pixel detector development can be found in the appendix.

Figure Captions

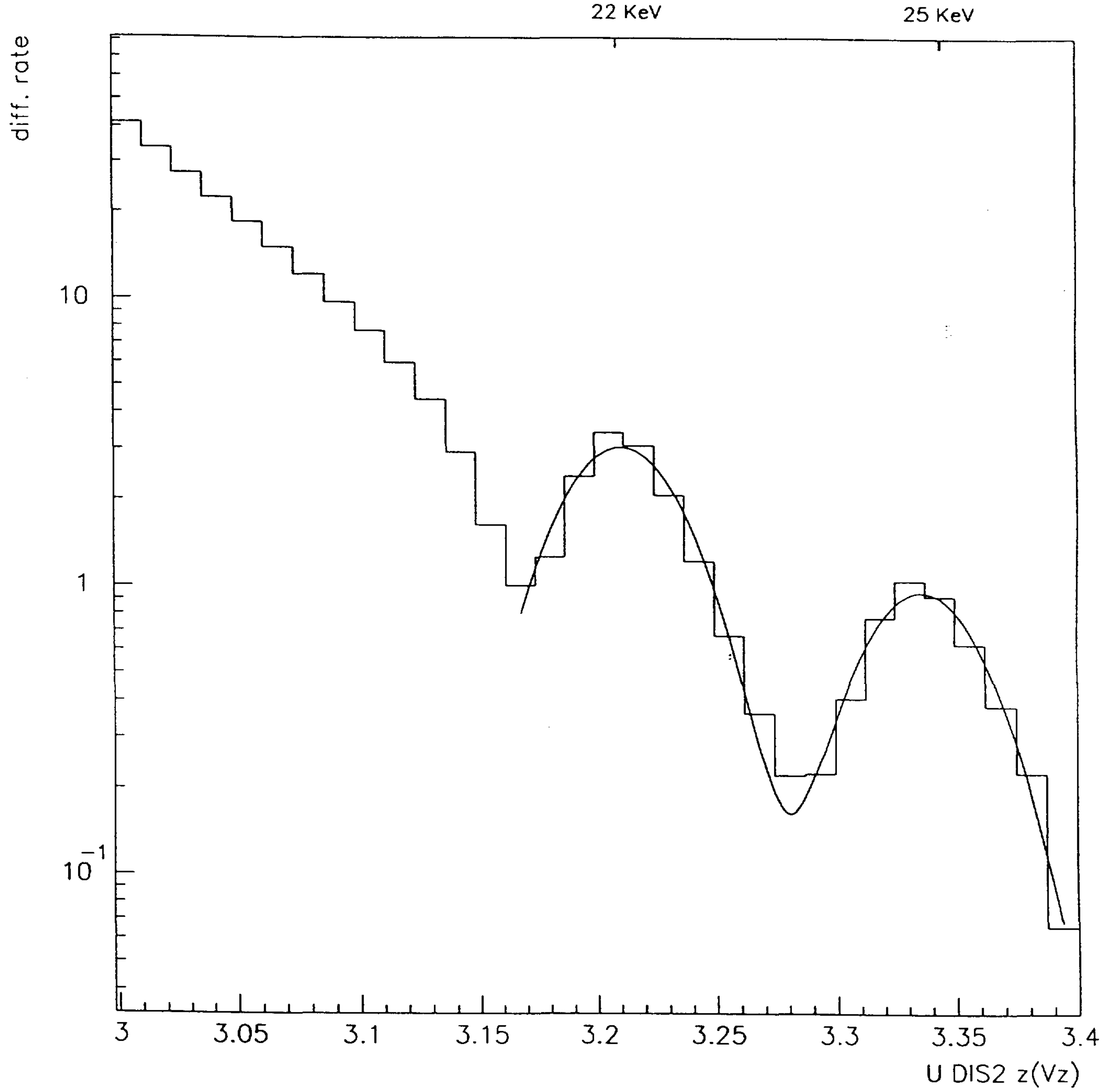
Fig. 1 Differential number of counts in a threshold scan for a single pixel irradiated by a ^{109}Cd radioactive source. The 22 keV and 25 keV lines are clearly separated, and this indicates a noise of 170 e^- r.m.s. or 1.4 keV FWHM.

Fig. 2 Histogram of beam particles detected in the 150 μm thick pixel detector matrix. The pixel dimensions are 75 μm x 500 μm. The beam is defined by the coincidence of several small scintillators. The spot measures only ~1 mm x 2 mm and its profile is measured at a threshold of ~4000 e^-.

Fig. 3 A pixel matrix with thin, modified back contact is irradiated through a fiber with light pulses of different wavelengths. The threshold curve for green (565 nm) light as a function of the LED bias voltage is shown at the bottom.

Fig. 4 Schematic representation of a wafer bonding process with preprocessed high resistive "handle wafer"

Fig. 5 Drawing of the basic module ("plaquette") of the DELPHI VFT pixel array.



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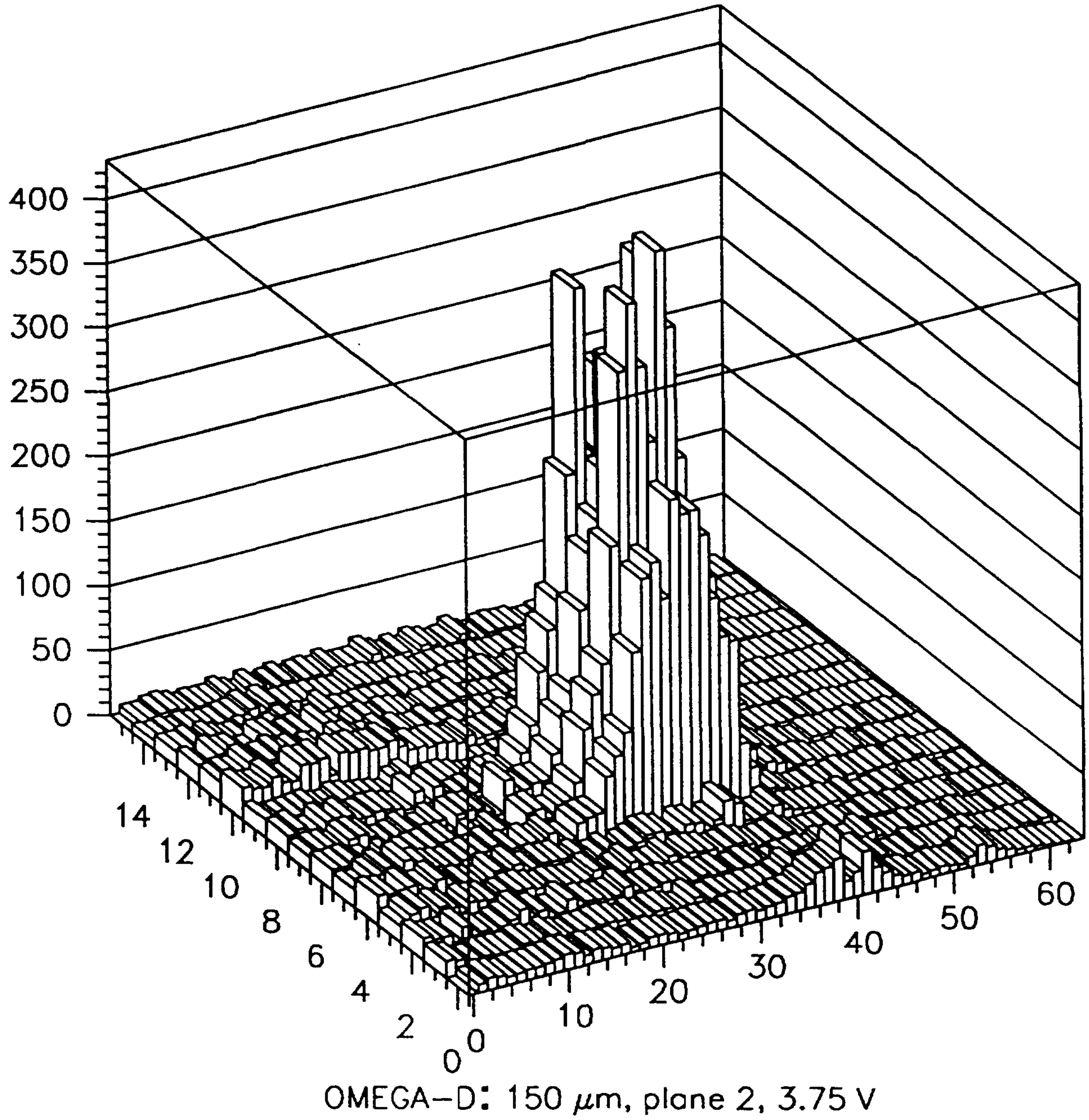

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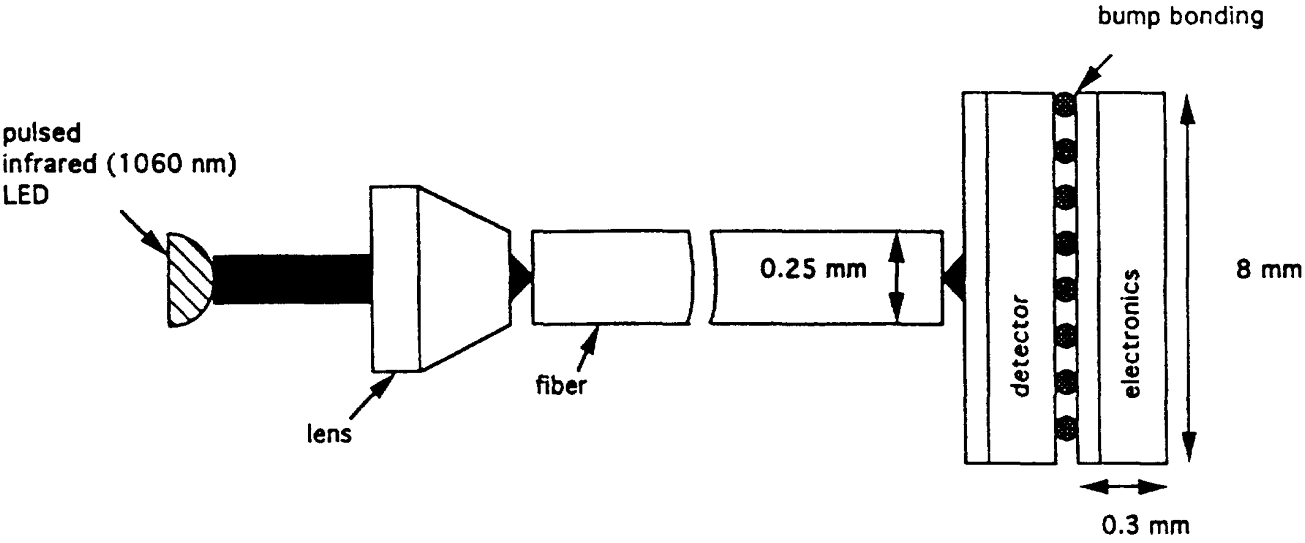

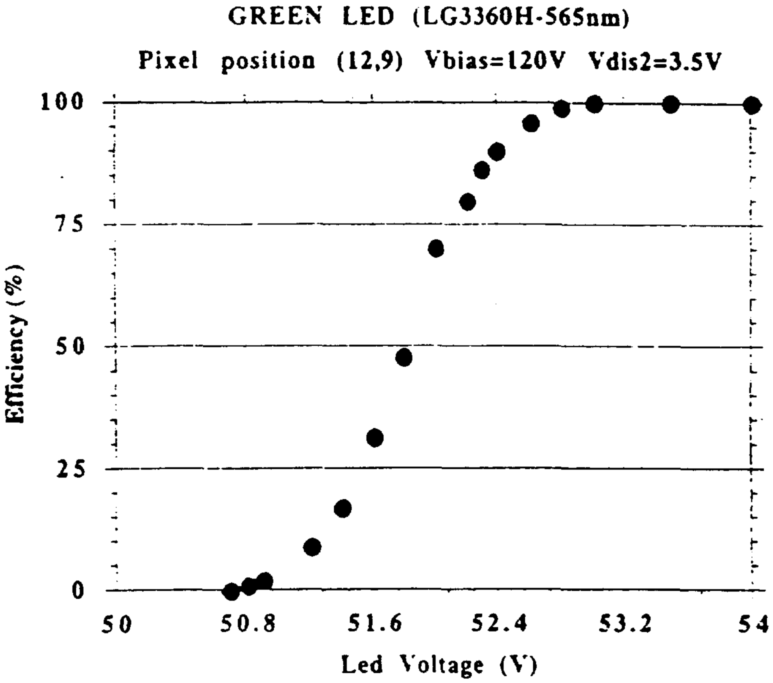

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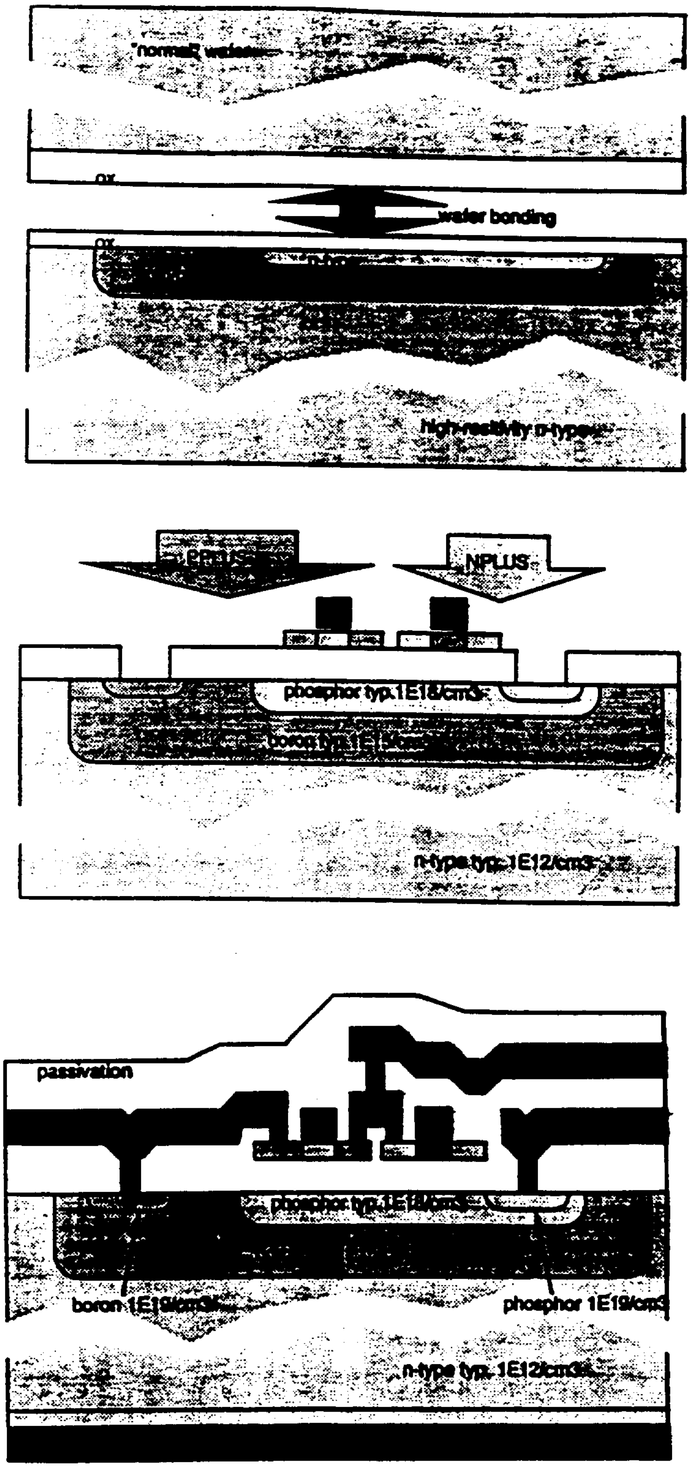

Fig. 4 Schematic representation of a wafer bonding process with preprocessed high resistive "handle wafer"

DELPHI PIXEL DETECTOR MODULE

16 electronic chips bump-bonded on
1 large detector plaquette (9 cm^2)

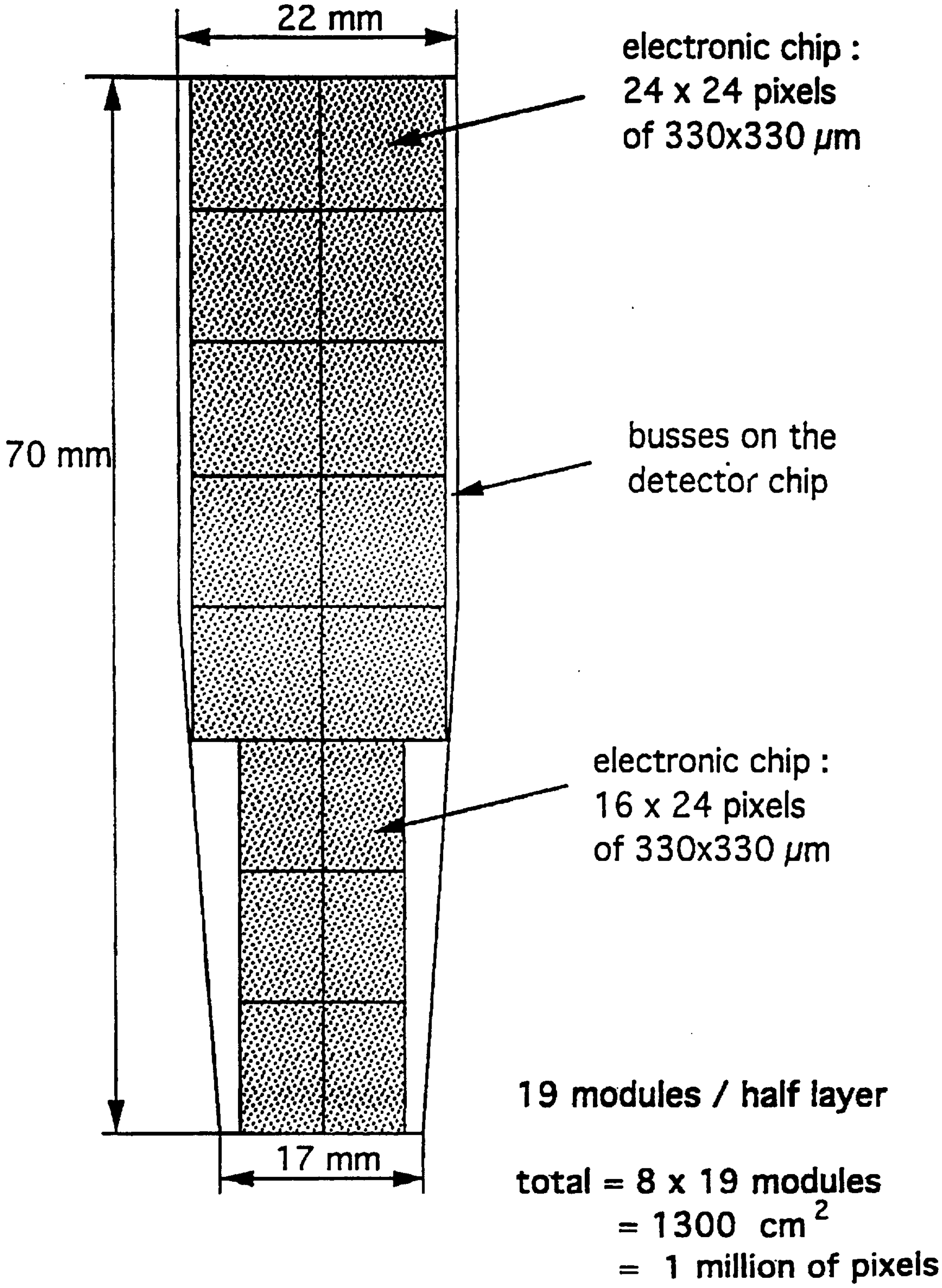

Fig. 5 Drawing of the basic module ("plaquette") of the DELPHI VFT pixel array.

APPENDIX

CERN/ECP/MIC-TF
5 January 1994

list of RD19 documents Erik Heijne/CERN

1. General documents

Erik H.M. Heijne, W. Beusch, M. Campbell, E. Chesi, M. Glaser, P. Jarron, F. Lemeilleur, E. Quercigh, C. Boutonnet, P. Delpierre, J.J. Jæger, A. Karar, C. Enz, F. Krummenacher, C. Neyer, G. Viertel, R. Hurst, L. Rossi, I. Debusschere, B. Dierickx, L. Hermans, G. Vanstraelen, J.C. Clemens, M. Cohen Solal, R. Potheau, D. Sauvage, N. Redaelli, G. Vegni, F. Nava, G. Ottaviani, L. Bosisio, L. Focardi, F. Forti and G. Tonelli
R&D Proposal: Development of hybrid and monolithic silicon micropattern detectors
CERN DRDC/90-81

Memorandum of understanding

Status report 28 January 1992 CERN DRDC/92-5

Status report 13 January 1993 CERN DRDC/93-6

Status report 20 January 1994 CERN DRDC/93-54

List of addresses of RD19 collaborators (update 18 December 1993)

2. Theses on pixel detectors in collaboration with CERN

Guy Vanstraelen Dec 1990
Monolithic integration of solid-state particle detectors and read-out electronics on high resistivity silicon
Katholieke Universiteit, Leuven, Belgium

Christian Neyer Nov 1993
The development of a pixel detector for high luminosity experiments
Swiss Federal Insitute of Technology Zürich Diss. ETH 10274

3.CERN/LAA/RD19 pixel publications

E.H.M. Heijne, P. Jarron, A. Olsen and N. Redaelli
The silicon micropattern detector: a dream ?
Nucl. Instr. Meth. A273 (1988) 615 (London PSD Conf.1987)

Erik H.M. Heijne and Pierre Jarron
Development of silicon pixel detectors: an introduction
Nucl. Instr. Meth. A275 (1989) 467 (1st Leuven Pixel Workshop)

Eric A. Vittoz
Tradeoffs in low-power CMOS analog circuits for pixel detectors
Nucl. Instr. Meth. A275 (1989) 472 (1st Leuven Pixel Workshop)

F. Krummenacher, C.C. Enz, M. Declercq, E. Vittoz, M. Campbell, E.H.M. Heijne, P. Jarron and G. Viertel
An experimental 10 MHz low power CMOS analog front-end for pixel detectors
Nucl. Instr. Meth. A288 (1990) 176 (5th Munich Symposium 1989)

Erik H.M. Heijne
Development of silicon pixel detectors for LHC
Proc. Large Hadron Collider Workshop Aachen, Oct.1990 CERN 90-10 Vol III p 237, 3 December 1990

M. Campbell, E.H.M. Heijne, P. Jarron, F. Krummenacher, C.C. Enz, M. Declerq, E. Vittoz and G. Viertel
A 10 MHz micropower CMOS front-end for direct readout of pixel detectors
Nucl. Instr. Meth. A290 (1990) 149

F. Krummenacher
Pixel detectors with local intelligence: an IC designer point of view
Nucl. Instr. Meth. A305 (1991) 527 (2nd Leuven Pixel Workshop)

P. Delpierre and J.J. Jaeger
A sparse data scan circuit for pixel detector chips
Nucl. Instr. Meth. A305 (1991) 627 (2nd Leuven Pixel Workshop)

P. Delpierre, W. Beusch, L. Bosisio, C. Boutonnet, M. Campbell, E. Chesi, J.C. Clemens, M. Cohen Solal, I. Debusschere, B. Dierickx, C. Enz, E. Focardi, F. Forti, M. Glaser, E. Heijne, L. Hermans, R. Hurst, A. Karar, F. Krummenacher, J.J. Jæger, P. Jarron, F. Lemeilleur, F. Nava, C. Neyer, G. Ottaviani, R. Potheau, E. Quercigh, N. Redaelli, L. Rossi, D. Sauvage, G. Tonelli, G. Vanstraelen, G. Vegni, G. Viertel and J. Waisbard
Development of silicon micropattern (pixel) detectors
Nucl. Instr. Meth. A315 (1992) 133 (5th Pisa Conf)

F. Anghinolfi, P. Aspell, K. Bass, W. Beusch, L. Bosisio, C. Boutonnet, P. Burger, M. Campbell, E. Chesi, C. Claeys, J.C. Clemens, M. Cohen Solal, I. Debusschere, P. Delpierre, D. Di Bari, B. Dierickx, C.C. Enz, E. Focardi, F. Forti, Y. Gally, M. Glaser, T. Gys, M.C. Habrard, E.H.M. Heijne, L. Hermans, R. Hurst, P. Inzani, J.J. Jæger, P. Jarron, F. Krummenacher, F. Lemeilleur, V. Lenti, V. Manzari, G. Meddeler, M. Morando, A. Munns, F. Nava, F. Navach, C. Neyer, G. Ottaviani, F. Pellegrini, F. Pengg, R. Perego, M. Pindo, R. Potheau, E. Quercigh, N. Redaelli, L. Rossi, D. Sauvage, G. Segato, S. Simone, G. Stefanini, G. Tonelli, G. Vanstraelen, G. Vegni, H. Verweij, G.M. Viertel and J. Waisbard
A 1006 element hybrid silicon pixel detector with strobed binary output
IEEE Trans. Nucl. Sci. NS-39 (1992) 650 also: CERN/ECP 91-26 (IEEE-NSS Santa Fe)

M. Campbell, F. Anghinolfi, P. Aspell, W. Beusch, E. Chesi, T. Gys, E.H.M. Heijne, P. Jarron, G. Meddeler, F. Pengg, E. Quercigh, G. Stefanini, H. Verweij, C. Boutonnet, P. Delpierre, J.J. Jæger, J. Waisbard, J.C. Clemens, M. Cohen Solal, Y. Gally, M.C. Habrard, R. Potheau, D. Sauvage, C. Neyer, G.M. Viertel, D. Di Bari, M.G. Catanesi, V. Lenti, V. Manzari, F. Navach, S. Simone, M. Morando, F. Pellegrini, P. Inzani, R. Perego, M. Pindo, N. Redaelli, P. Burger, K. Bass, A. Munns, C.C. Enz and F. Krummenacher
Design and performance of the 'Omega-ion' hybrid silicon pixel detector
internal report CERN/ECP 92-6 (presented at 6th Munich/Milano Symp. 1992)

M.G. Catanesi , H. Beker, W. Beusch, M. Campbell, E. Chesi, J.C. Clemens, P. Delpierre, D. DiBari, E.H.M. Heijne, P. Jarron, V. Lenti, V. Manzari, M. Morando, F. Navach, C. Neyer, F. Pengg, R. Perego, M. Pindo, E. Quercigh, N. Redaelli, D. Sauvage, G. Segato and S. Simone
Results from a hybrid silicon pixel telescope tested in a heavy ion experiment at the CERN Omega spectrometer
Nucl. Physics B (Proc. Suppl.) 32 (1993) 260 (Como 1992)

H. Beker, W. Beusch, M. Campbell, M.G. Catanesi, E. Chesi, J.C. Clemens, P. Delpierre, D. Di Bari, E.H.M. Heijne, P. Jarron, V. Lenti, V. Manzari, M. Morando, F. Navach, C. Neyer, F. Pengg, R. Perego, M. Pindo, E. Quercigh, N. Redaelli, D. Sauvage, G. Segato and S. Simone
A hybrid silicon pixel telescope tested in a heavy-ion experiment
Nucl. Instr. Meth. A332 (1993) 188 also CERN/ECP 92-18 (combination of previous 2 papers)

J.J. Jaeger, C. Boutonnet, P. Delpierre, J. Waisbard and F. Plisson
A sparse data scan circuit for pixel detector readout, design and methodology
EURO-ASIC 1992 & IEEE - NSS Conf. Proc. Oct 1992, Orlando & Collège de France LPC 92 11

L. Bosisio, E. Focardi, F. Forti, S. Kashigin, B. Dierickx, D. Wouters, G. Willems, G. Winderickx, I. Debusschere, E. Simoen, C. Claeys, H. Maes, L. Hermans, E.H.M. Heijne, P. Jarron, M. Campbell, F. Anghinolfi, P. Aspell, P. Delpierre, D. Sauvage and M.C. Habrard
Detector diodes and test devices fabricated in high resistivity SOI wafers
Conference Record IEEE Nucl. Science Symp. Orlando 1992

B. Dierickx, D. Wouters, G. Willems, G. Winderickx, A. Alaerts, I. Debusschere, E. Simoen, J. Vlummens, C. Claeys, H. Maes, L. Hermans, E.H.M. Heijne, P. Jarron, F. Anghinolfi, P. Aspell, M. Campbell, F.X. Pengg, L. Bosisio,E. Focardi, P. Delpierre, A. Mekkaoui, M.C. Habrard and D. Sauvage
Integration of CMOS-electronics in an SOI layer on high-resistivity silicon substrates
Conference Record IEEE Nucl. Science Symp. Orlando 1992

B. Dierickx, D. Wouters, G. Willems, A. Alaerts, I. Debusschere, E. Simoen, J. Vlummens, H. Akimoto, C. Claeys, H. Maes, L. Hermans, E.H.M. Heijne, P. Jarron, F. Anghinolfi, M. Campbell, F.X. Pengg, P. Aspell, L. Bosisio, E. Focardi, F. Forti, S. Kashigin, A. Mekkaoui, M.C. Habrard, D. Sauvage and P. Delpierre
Integration of CMOS-electronics and particle detector diodes in high-resistivity silicon-on-insulator wafers
IEEE Trans. Nucl. Sci. NS-40 (1993) 753 (combination of previous 2 papers)

S. Kavadias, K. Misiakos, D. Loukas and N. Haralabidis
A silicon pixel detector with integrated amplification devices
Nucl. Instr. Meth. A335 (1993) 266

M. Campbell, F. Antinori, H. Beker, W. Beusch, E. Chesi, E.H.M. Heijne, J. Heuser, P. Jarron, T. Karttaavi, L. Lopez, G. Meddeler, A. Menetrey, P. Middelkamp, C. Neyer, F. Pengg, M. Pindo, E. Quercigh, S. Simone and H. Verweij
Development of a pixel readout chip compatible with large area coverage
to be published in NIM CERN/ECP (Hiroshima Symp. 1993)

S. Kavadias, K. Misiakos and D. Loukas
Calculation of pixel detector capacitances through three dimensional numerical solution of Laplace equation
submitted to NIM

E.H.M. Heijne, F. Antinori, H. Beker, G. Batignani, W. Beusch,V. Bonvicini, L. Bosisio, C. Boutonnet, P. Burger, M. Campbell, P. Cantoni, M.G. Catanesi, E. Chesi, C. Claeys, J.C. Clemens, M. Cohen Solal, G. Darbo, C. DaVia', I. Debusschere, P. Delpierre, D. Di Bari, S. Di Liberto, B. Dierickx, C.C. Enz, E. Focardi, F. Forti, Y. Gally, M. Glaser, T. Gys, M.C. Habrard, G. Hallewell, L. Hermans, J. Heuser, R. Hurst, P. Inzani, J.J. Jæger, P. Jarron, T. Karttaavi, S. Kersten, F. Krummenacher, R. Leitner, F. Lemeilleur, V. Lenti, M. Letheren, M. Lokajicek, D. Loukas, M. Macdermott, G. Maggi, V. Manzari, P. Martinengo, G. Meddeler,F. Meddi, A. Mekkaoui, A. Menetrey, P. Middelkamp, M. Morando, A. Munns, P. Musico, F. Nava, F. Navach, C. Neyer, F. Pellegrini, F. Pengg, R. Perego, M. Pindo, S. Pospisil, R. Potheau, E. Quercigh, N. Redaelli, J. Ridky, L. Rossi, D. Sauvage, G. Segato, S. Simone, B. Sopko, G. Stefanini, V. Strakos, P. Tempesta, G. Tonelli, G. Vegni, H. Verweij, G.M. Viertel, V. Vrba and J. Waisbard
Development of silicon micropattern pixel detectors
subm. to NIM PSD3, London, Sept 1993

C. Da Via', M. Campbell, E.H.M. Heijne and G. Stefanini
Imaging of visible photons using hybrid silicon pixel detectors
submitted to NIM, PSD3, London, Sept 1993 also: CERN/ECP 93

L. Bosisio, F. Forti and E. Tomacruz
Measurement and tridimensional simulation of silicon pixel detector capacitance
submitted IEEE Trans. Nucl. Sci. NS-41 (1994) 1 IEEE-NSS 1993 San Francisco (LBL collaboration)

M. Alietti, F. Nava, R. Tonini, P. Cantoni, L. Stagni and A. Cavallini
Rapid thermal process-induced defects in silicon position detectors
to be published in NIM

P. Delpierre
Large area pixel detectors, developments and proposals for high energy physics experiments
to be published in Proceedings Marseille Conference August 1993

E.H.M. Heijne, F. Antinori, R. Arnold, H. Beker, W. Beusch, P. Burger, M. Campbell, E. Chesi, G. Darbo, C. DaVia', D. Di Bari, S. Di Liberto, D. Elia, C.C. Enz, M. Glaser, J.L. Guyonnet, T. Gys, H. Helstrup, J. Heuser, R. Hurst, A. Jacholkowski, P. Jarron, S. Kersten, F. Krummenacher, R. Leitner, F. Lemeilleur, V. Lenti, M. Letheren, M. Lokajicek, L. Lopez, M. LoVetere, G. Maggi, P. Martinengo, G. Meddeler, F. Meddi, A. Menetrey, P. Middelkamp, M. Morando, A. Munns, P. Musico, C. Neyer, M. Pallavicini, F. Pellegrini, F. Pengg, S. Pospisil, E. Quercigh, J. Ridky, L. Rossi, K. Safarik, G. Segato, S. Simone, P. Tempesta, H. Verweij, G.M. Viertel and V. Vrba
First operation of a 72k element hybrid silicon micropattern pixel detector array
to be submitted to NIM

V. Bonvicini, P. Inzani, M. Pindo, N. Redaelli, F. Severi, M. Campbell, E.H.M. Heijne, P. Jarron, P. Middelkamp and F. Krummenacher
Performance of a VLSI analogue readout cell for hybrid silicon pixel detectors (ANAPIX)
to be submitted to NIM

4. Design Reports

F. Krummenacher and C.C. Enz
Electronique integree pour detecteurs a pixels, LEG/EPFL 1989
LAA design, cell A with latched comparator

F. Krummenacher and C. Enz
Developpement d'une cellule digitale pour detecteur a pixel, SSS nov.1990
cell B, asynchronous comparator

F. Krummenacher
Amelioration des performances de la cellule de lecture digitale asynchrone pour detecteur a pixels, SSS june 1991
cell C

F. Krummenacher and C. Enz
Developpement d'une cellule de lecture avec sortie analogique pour detecteur a pixel, SSS January 1991

F. Krummenacher
Cellule de lecture a sortie analogique pour detecteur a pixels ou a strips courts, SSS January 1992
anapix cell

5. SOI notes RD19/IMEC

SP/CCD-523/91-01, B. Dierickx 30 May 1991
Monolithic SOI-HΩ processing, Phase 1: SOI-HΩ feasibility

SP/CCD-523/91-02, B. Dierickx 8 Aug 1991
"HRTEST" (SOI/HR testchip) Description and pin configuration

SP/CCD-523/91-03, B. Dierickx 9 Sept 1991
SOI-HΩ processing Phase 2: SOI-HΩ mask design and fabrication

SP/CCD-523/92-02, B. Dierickx 27 April 1992
Intermediate report on results of SOI-HΩ p-line 402-run (SIMOX wafers)

SP/CCD-523/92-01, B. Dierickx, H. Akimoto 29 June 1992
Further evaluation of HR-SOI SIMOX run

SP/CCD-523/92-04, G. Willems and D. Wouters July 1992
Study of the Laser-ZMR material

SP/CCD-523/92-03 31 Aug 1992
Final Report on the results of the SOI-on-HΩ PL402-run (SIMOX wafers) and PL549-run (ZMR wafers)

P43004-93-04-EX 10 June 1993
Final Report on the results of the SOI-on-HΩ PL984-run (SIMOX and ZMR wafers)

6. Chip list: cells,readout matrices and detector matrices

August 1991
new update to be made

7. Technical notes TN

#1	Erik Heijne Details concerning design of Omega chip, bonding compatibility etc.	21 June 1991
#2	Erik Heijne Size of readout chip, thinning, MCM	10 Oct 1991
#3	Erik Heijne Array 5x5 cm, bumping and planning	18 Dec 1991
#4	Enrico Chesi Si pixel readout for March 1991: layout, readout,etc.	30 Nov 1991
#5	R. Perego, M. Pindo and Nicola Redaelli Leakage current measurements before and after wafer metallization for bumping	29 May 1992
#6	Erik Heijne Laser testing at CPPM, first ladder testing and plans test beam April	27 March 1992
#7	Erik Heijne Thickness and size of Wafers, Si-MCM. Discussion with GEC-Marconi at CERN	1 April 1992
#8	Christian Neyer, Harry Beker and Peter Middelkamp Measurements for determining the yield of the Omega pixel chip	May 1992
#9	Timo Karttaavi and Michael Campbell Sensitivity of D-Omega readout circuit for process variations and mismatches	May 1992
#10	Franz Pengg and Michael Campbell Measurements of pixel TST chip	May 1992
#11	Erik Heijne Project for multichip silicon base pixel module	26 May 1992
#12	R. Perego, M. Pindo, N. Redaelli Results of leakage current measurements on test structures of pixel detectors	29 May 1992
#13	C. Boutonnet, J.-J. Jaeger, J. Waisbard Notice d'utilisation Circuit CDFSP2	Nov 1992
#14	C. Boutonnet, J.-J. Jaeger, J. Waisbard Notice d'utilisation Circuit CDFSP3	Dec 1992
#15	M. Pindo, M. Campbell, P. Middelkamp and C. Neyer Omega2 cell measurement report	Feb 1993
#16	Johann M. Heuser Electrical and source measurements with LAA pixel detectors+addendum 22-6-93	3 Feb. 1993

#17	Erik Heijne Instructions for micropattern detector ladder mounting	26 March 1993
#18	Erik Heijne MCM Si base pixel module	March 1993
#19	Johann M. Heuser Electrical and laser measurements with CDF2 readout chips+ addendum	19 May 1993
#20	C. Boutonnet, J.-J. Jaeger, J. Waisbard Notice d'utilisation Circuit CDFSP4	Juillet 1993
#21	Prague group: T. Chábera, J. Kubasta, R. Leitner, M. Lakajícek, S. Pospísil, J. Rídky and V. Vrba Analysis of data from pixel detectors run RD19, 7-12 May 1993	Aug 1993
#22	Johann Heuser Beam test with 3-plane OMEGA D telescope	2 Sept 1993
#23	S. Kavadias, D. Loukas and K. Misiakos Calculation of pixel capacitances and noise measurements of the readout electronics in the Omega silicon hybrid detector	27 September 1993
#24	Johann Heuser Sparse data scan tests with CdF.SPARSE3 Pixel detector readout chips	19/25 October 1993
#25	Roger Arnold Résumé de l'analyse des données du pixel detector (1&6 ladder array in Run T9)	19 Nov 1993
#26	Franz Pengg Monolithically integrated silicon pixel detectors in SOI technology	Dec 1993
#27	Peter Middelkamp, Johann Heuser, Christian Neyer, Michael Campbell Test beam report H6, run Nov 1993	Dec 1993
#28	D. DiBari and D. Elia Pixel detector in WA97 test	Dec 1993

8. Various papers on pixel detectors.

Erik H.M. Heijne, Ingrid Debusschere and Hobart W. Kraner, editors
Proceedings of " Workshop on Silicon Pixel Detectors", June 1988 Leuven Belgium
Nucl. Instr. Meth. A275 (3)

Eric A. Vittoz
Tradeoffs in low-power CMOS analog circuits for pixel detectors
Nucl. Instr. Meth. A275 (1989) 472 (1st Leuven Workshop)

Erik H.M. Heijne, Ingrid Debusschere and Hobart W. Kraner, editors
Proceedings of " 2nd Workshop on Silicon Pixel Detectors" , June 1990 Leuven
Nucl. Instr. Meth. A305 (3)

Paul E. Karchin
Use of pixel detectors in elementary particle physics
Nucl. Instr. Meth. A305 (1991) 497 (2nd Leuven Workshop)

J. Ardelean, R.L. Chase and A. Hrisoho
A proposed pixel detector based on floating base transistors
Nucl. Instr. Meth. A305 (1991) 549 (2nd Leuven Workshop)

Z.Y. Chang and W. Sansen
Effect of 1/f noise on the resolution of CMOS analog readout systems for microstrip and pixel detectors
Nucl. Instr. Meth. A305 (1991) 553 (2nd Leuven Workshop)

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PRELIMINARY VERSION

First operation of a 72 k element hybrid silicon micropattern pixel detector array

E.H.M. Heijne[1], F. Antinori[1], R. Arnold[10], D. Barberis[5], H. Beker[7], W. Beusch[1], P. Burger[11], M. Campbell[1], E. Chesi[1], G. Darbo[5], C. Da Via[1], D. Di Bari[4], S. Di Liberto[7], D. Elia[4], C.C. Enz[2], M. Glaser[1], J.L. Guyonnet[10], T. Gys[1], H. Helstrup[1], J. Heuser[8], R. Hurst[5], A. Jacholkowski[4], P. Jarron[1], S. Kersten[8], F. Krummenacher[13*], R. Leitner[9], F. Lemeilleur[1], V. Lenti[4], M. Letheren[1], M. Lokajicek[9], L. Lopez[1], M. LoVetere[5], G. Maggi[4], P. Martinengo[1,5], G. Meddeler[1], F. Meddi[7], A. Menetrey[1], P. Middelkamp[1,8], M. Morando[6], A. Munns[12], P. Musico[5], C. Neyer[3], M. Pallavicini[5], F. Pellegrini[6], F. Pengg[1†], S. Pospisil[9], E. Quercigh[1], J. Ridky[9], L. Rossi[5], K. Safarik[1], G. Segato[6], S. Simone[4], P. Tempesta[4], H. Verweij[1], G.M. Viertel[3] and V. Vrba[9]

CERN RD19 collaboration

CERN[1] (CH1211 Geneva 23), EPFLausanne[2], ETH Zurich[3], INFN and University of Bari[4], Genova[5], Padova[6], Roma[7], University GHS Wuppertal[8], Group Praha[9], CRN/University Louis Pasteur Strasbourg[10], Canberra Semiconductor NV[11], GEC-Marconi (Caswell)[12] and Smart Silicon Systems SA[13]

* Also with EPF Lausanne, Switzerland,
† Fellowship Austria

Abstract

We have constructed and tested pixel detector arrays of 96 x 378 (36288) sensor elements with associated low noise signal processing circuits contained within each 75 μm x 500 μm pixel area. Two such arrays together, staggered by ~4 mm cover hermetically a 53 mm x 55 mm area with 72576 pixels. The pixel cell response for ionizing particles is binary with an adjustable threshold between 4000 e^- and 15000 e^-. Single chips, the array of 6 ladders and a fully hermetic, double array have been characterized in particle test beams and in the Omega experiment WA97 at CERN. With a beam trigger most events consist of a single cluster with a single hit. The ~11% of double hits depends only slightly on threshold and detector bias voltage. Tracks were reconstructed with a precision of 22 μm and an efficiency >99% was measured. The proportion of properly functioning pixels was 98% in the first 36k pixel array and 80% in the second. 1% of "always-on" pixels could be masked electronically. After masking the proportion of "spurious noise hits" was $< 10^{-6}$ of the identified particle hits while with beam-off no hits at all were recorded.

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1. INTRODUCTION

The first fully operational hybrid silicon micropattern particle detector assemblies with 1006 sensitive pixels, which contain a low noise signal processing circuit within the 75 µm x 500 µm area of every single pixel have been used already at the end of 1991 in the 'Omega-Ion' experiment WA94 at CERN [1] which was the predecessor of the current experiment Omega WA97. Now we have constructed two detector arrays each with 96x378 i.e. 36288 pixel cells, covering a 53 mm x 55 mm area. The detector matrix and the chip with the readout circuits are made on separate silicon wafers and are connected in a "hybrid" assembly using solder bump bonding. The readout chip consists of a matrix with 16 columns and 63 rows together with a test row at the top and some peripheral electronics at the bottom. Such a readout chip can be assembled with a single high resistivity silicon detector chip with identically corresponding geometry, or six chips on a row can be placed on a common detector matrix called "ladder". This ladder has 96 columns and 63 rows of detecting elements. A complete array with 6 ladders is illustrated in fig. 1 and it carries 36 readout chips. Two such arrays together, staggered by ~4mm cover hermetically the 53x55 mm^2 area (29.15 cm^2) with a total of 72576 detector elements.

First we have separately studied the performance of the new single chip assemblies with 1008 cells using a telescope arrangement in the H6 120 GeV pion beam. In the following step we have tested the complete arrays of 6 ladders, using the test row with electrical input on each chip. Then we have used electrons from a radioactive source to study the response of the pixel cells and we have measured efficiency and overall performance in the CERN T9 test beam and finally in WA97.

The driving force behind pixel detector development are the high intensity, high rate particle physics experiments which are expected around the year 2000, e.g. at the proposed Large Hadron Collider LHC, where a true 2-dimensional microdetector will enable efficient and fast pattern recognition and can provide a desirable improvement in selectivity for various types of reactions. Our aim is first to prove the feasibility of the micropattern detector concept in the Omega WA97 heavy ion fixed target experiment rather than pushing immediately for the more demanding designs for such future experiments. It is important to encounter and solve practical problems associated with building a micropattern detector in a real particle physics application. A second reason for the cautious approach is to increase the level of confidence and support in the particle physics community for what is still considered an exotic detector. At the same time, if the micropattern detector is shown to function well, it could provide easier access to various types of more immediate phycics research in beauty factories, heavy ion colliders, etc. Finally, the concept of the micropattern detector looks very promising for applications like high speed X-ray imaging [2].

2. DESCRIPTION OF THE HYBRID PIXEL ARRAY

A photograph of the pixel array together with the intermediate readout electronics card and the VME readout module is shown in fig. 1. This system was installed in October 1993 in the T9 test beam and in November in the WA97 Omega heavy ion experiment.

2.1 The silicon detector ladders

The detector "ladder" is the building block of the array and consists of a "chip" of high resistivity n-type silicon (~5 kΩcm) with dimensions 54 x 6 mm^2 and 300 µm thick. It is organized as a matrix of 96 columns and 64 rows of independent, ion-implanted diodes of rectangular shape. The dimensions of most of these diodes are 500 µm x 75 µm. The cells in the columns which correspond to the edges of the readout chips are twice as long, 1000 µm instead of 500 µm, in order to "stitch" the two regions of coverage together, as is illustrated in the photograph of fig. 2 which shows the right-hand one-third of the rectifying front side of the detector chip. Each diode can be DC connnected by a tiny solder bump to a virtual ground via its front-end amplifier circuit on the associated readout chip. The complete matrix is surrounded by an ion-implanted guard ring diode which also is grounded via the readout chips. The rear side of the detector wafer is ion-implanted in order to obtain a common n+ ohmic contact without segmentation. The bias voltage, typically 40 to 70 V is applied to this rear side of the ladder and the usual bias filter network is placed on the ceramic substrate besides each of the ladders. This can be seen on the photograph of a completed array in fig. 3.

Ten detector ladders are manufactured on a 100 mm diameter wafer, together with some single chip matrix detectors with 1024 diode cells and a few test structures. The reverse diode leakage current for the detector ladders is typically a few nA per cm^2 at 50 V applied bias and can be measured only after assembly of the ladder. It is virtually impossible to make reliable contacts to all ~6000 diodes on a ladder without bump-bonding. The detector wafer quality, however, was checked before the bump-bonding step by measuring several test diodes of 1 cm^2.

2.2 Mechanical construction and electrical connections of the array

The pixel detector array has to provide hermetic coverage of an area of 5 x 5 cm^2 but this is difficult to achieve with a single plane because of the need for electrical connections to each of the readout chips. We have chosen to cover the full "logical" plane using 2 staggered arrays as illustrated in fig. 4. The support plate for each array is a 380 µm thick ceramic substrate with thin-film metal conductors which act as the connection lines for all readout chips, as shown in fig. 5. The building block for the array, the detector "ladder" carries 6 readout chips which are bump-bonded to the individual detector diodes as described hereafter and the common electrical connection to the rear side of these readout chips is provided by a 55 mm long and 250 µm thick ceramic slab which is metallized facing the readout chips. The slab isolates the chips from the conductors on the support plate and provides a homogeneous surface for glueing the ladder in place. A schematic drawing with one complete ladder-assembly and its connections is shown in fig. 6. The 6 ladder-assemblies are glued side by side on the thin-film ceramic substrate with a space of a few mm in between. The ladders are positioned on the ceramic with a precision of ±10 μm using a special table with x-, y-, z- and rotational movements. After positioning the ladder is secured in place by temporary fixtures. The epoxy glue is cured in an oven at 60 °C for several hours. A ceramic support with the first ladder positioned and secured can be seen in fig. 7. In this way the mounting of a full array took ~one week.

After all 6 ladders have been glued the external electrical connections are made between the buslines on the ceramic and the bonding pads on the readout chips using ultrasonic wirebonding as can be seen in fig. 8. In this close-up one may see the readout chips just stick out from underneath the detector ladders. The bias connections to the detector ladders are made by wirebonding to the rear side of the ladders. A flexible multilayer circuit visible in fig. 1 is glued onto the edge of the ceramic support plate and carries the supply voltages and the 32-bit data bus lines from the intermediate readout card onto the ceramic. Some of the distribution and decoupling of the voltage supplies is situated on this flexible circuit. A flat cable makes the connection between the intermediate readout card and the VME card in the control room, about 30 m away. This VME card will be described in sect. 2.5.

Finally, each array is held on a U-shaped, 3 mm thick ceramic plate of outer dimensions 132 mm x 132 mm. The smaller, thin ceramic support plate braces the 9 cm wide, open center of the U and the flexible circuit is fixed onto the lower part of the U-ceramic. The U is the handling unit that is placed on the optical rail for the silicon detectors in the Omega spectrometer.

2.3 Frontend electronics, threshold calibration and timing

The electronics readout chip is named Omega2 and its schematic and layout are similar to the Omega-D chip for which the details have been described earlier [1]. Both integrated circuits have been made in the 3 μm Self-Aligned Contact CMOS (SACMOS3) technology of Faselec, Zurich, which offers a very dense layout, actually comparable to an effective 1.5 μm circuit technology. In each pixel cell a low noise frontend amplifier is followed by a comparator with adjustable threshold.

The threshold setting in each pixel depends on a current source which can be adjusted via an external bias voltage. Because this current source also supplies the frontend amplifier its response varies at the same time and this causes non-linearity in the threshold as a function of bias voltage. Realistic average values for the threshold are between 4000 and 15000 equivalent electrons at the amplifier input. In fig. 9 the threshold for a single chip is shown as a function of the applied voltage Udis2. The threshold curve (at 50% response) is measured for single pixels, using the row of 16 test pixels at the top of each matrix which can be pulsed via a built-in capacitor. In the same fig. 9 absolute calibration points are shown which are obtained from normal pixels connected to the detector matrix using photon-emitting radioactive sources of ^{109}Cd, ^{241}Am and ^{57}Co. A good correspondence between the electrical test and the absolute calibration is found if we assume an injection capacitor value of 30 fF which is 50% higher than the designed value of this parasitic field oxide capacitor. At the same time an absolute calibration of the noise of the complete detector with associated electronics could be performed with the ^{109}Cd source and 170 e^- r.m.s. or 1.4 keV FWHM has been measured [3].

From the layout of the ceramic support illustrated in fig. 5 one can see that the 6 chips in a column of the detector array have common power supplies for all the functions, like gain, threshold, delay, etc. It can be expected that if a bad chip would corrupt a supply line all the other chips on the same line may misbehave. In fact, externally on the VME card there is only a single settable value provided for each parameter for the whole array. Therefore, prior to bump-bonding all chips have been tested on wafer in order to ascertain that the DC values are compatible within small tolerances as will be discussed in sect. 2.6.

The threshold for a 6-ladder array is plotted as a function of Udis2 in fig. 10 using electron irradiation data instead of the electrical test row. Because here a 100% response has been taken as threshold this curve is shifted towards values that are ~3000 e^- higher than in fig. 9. More irradiation data for the 6-ladder array will be discussed in sect. 4.1.

If a particle signal exceeds the threshold the bit resulting from this 'hit' is delayed in a 'pipeline' in the pixel such that a logic coincidence can be made with the external strobe signal which is derived from a positive first level trigger. A schematic diagram of the timing sequence is shown in fig. 11. The internal pipeline delay is adjustable between ~100 ns and ~ 1 μs. If there is coincidence the databit is stored in a local memory in the pixel, otherwise it is lost. It can then be read out via the vertical shift register or it can be reset in case of an abortive higher level trigger. The average delay time of the signals in the pixel pipelines for the 6-ladder array as a function of the adjustable voltage parameter Udn is plotted in fig. 12.

Several improvements have been implemented in the new chip in order to obtain a better matching of the timing between pixel cells [3]. Although the timing uniformity within a single chip has been tightened and a distribution with a standard deviation of ~20 ns rms has been measured, it now is found that a non-uniformity exists in the pipeline delays between the ladders on the array. This effect can be attributed to small voltage drops due to resistance of the supply lines on the ceramic support. In fig. 13 is shown that for the external strobe delay different values are needed for each ladder in order to obtain optimal detection efficiency. The difference in internal delay leads to a loss of recognized hits but can be compensated by making the external strobe signal long enough to cover the range of delay values. In fig. 14 a histogram is shown for the separate chips in the array and a difference of nearly 200 ns between the top and the bottom of the array is seen. Therefore, a fairly long coincidence strobe signal of ~500 ns has been necessary. This external strobe signal is issued with some delay after the time-zero of the event.

An average value had to be determined for the array as a whole, and often 150 ns was used which corresponds then with an overall internal delay of 800 ns.

2.4 Assembly by bump-bonding

The deposition of the various metal layers and the forming of the Pb-Sn solder bumps on the readout wafers was performed by GEC-Marconi Materials Ltd at Caswell [4]. Reflow results in hemispherical bumps with a diameter of 38 µm [1]. After dicing of the wafers previously selected chips are aligned on a flip-chip bonding machine and the chips stick together temporarily. The bonding is achieved by heating the chips in an oven above the eutectic temperature of the solder (183 °C). The final alignment of the chips is facilitated by the surface tension in the molten solder which adheres to the wettable metal pads on both sides but does not wet elsewhere on the chips. After bonding the height of the bumps is 13 µm. The averaged amount of solder between the chips represents 0.4 µm of Pb-Sn or 0.04% of a radiation length which is a very small fraction of the total thickness of 1.4 mm or 1.2% radiation length of the present array. Development is under way which aims at reducing this thickness further.

During the development of the detector arrays already over 500 chip placements have been made involving the production and inspection of over a million bumps. The failure rate in the bonding is better than 10^{-3} and could be further improved by enhancing the already existing quality inspections at critical steps. Some of the observed failures were related to debris or dust particles deposited well outside the matrix of bumps and which prevented the chips to mate properly. We have not yet found means to distinguish a faulty electronic pixel circuit from a faulty bump connection and therefore the yield numbers relate to the combination of both phenomena.

2.5 Readout organization and "on-board" intelligence

The schematic diagrams of the readout cards are shown in fig.15. An intermediate card is placed close to the detector and a VME card in the control room. The readout sequence for the chips is schematically given in fig. 16. The array is split into 2 parts which are read in parallel. In each clock cycle the 16-bit data from 2 chips are combined into one 32-bit word. Tri-state drivers were added on the Omega2 chips and these allow the different chips in the array to send their data serially via the bus.

In this way, in spite of the large number of sensor elements only one card is needed for an array and data are transmitted as 32-bit words. The readout speed in the laboratory was up to 20 MHz but in the experimental situation with transmission over 30 m only 2 MHz was achieved. The readout time of the array was 576 µs, well below the readout time for the other detector systems in the Omega experiment.

The VME card performs data acquisition including masking of noisy pixels and zero suppression as well as various other functions. It only transmits to the data-acquisition computer the non-zero data words with their corresponding address indication. The hardware masking possibility is an essential feature in a pixel detector in view of the large number of sensor elements and the unavoidable occurrence of bad pixels. After it is found which pixels are "always-on" or are abnormally noisy these can be masked and can further be treated as in "off" state. In the experiment the number of pixels that had to be masked was about 600 or 1% of the double array, mostly because they were "always-on". "Always-on" pixels create problems of dead time and also make on-line histogramming difficult and it is essential to eliminate them from the real time data flow, given the large number of sensor elements in a pixel detector. It is intended to eventually transfer on-chip both the zero-suppression and the masking. This is a first step towards an intelligent ("smart") micropattern detector.

The VME card supplies the programmable voltages for the various adjustments needed for the operation of the array. The values for gain and threshold have been optimized in a laboratory test using a radioactive electron source and a scintillator trigger (sect.4.1). The delay optimization has been done in the beam test itself.

2.6 Testing and reliability including preassembly tests

The feasibility of multi-chip arrays depends crucially on the availibility of tested, fully functional components. In a 2-step procedure the components are tested before the array construction. The DC parameters have been tested on wafer using a standard probe station with dedicated probe card. Afterwards, these wafers are bumped, diced and bonded to the matching detectors. The second step is the test of finished, bump-bonded 'ladders' before glueing these on a common ceramic support. Pulsing of the test row and irradiation of the detector with an electron source have been performed on the finished ladders, for one readout chip at the time. Acceptance limits for the measured parameters were defined, in order to decide which chips and which ladders can be mounted. The yield of good chips in the wafer test was 70% [3] while the ladder test has not yet been performed in a systematic way. In the first experience it appears that the DC wafer test has eliminated most of the bad chips.

3. TESTING OF A TELESCOPE OF SINGLE MATRIX ASSEMBLIES IN A 120 GEV BEAM

A "telescope" test setup of 3 pixel matrix assemblies similar to the one described in [1] has been installed in the H6 beam at CERN and a schematic drawing is shown in fig. 18. The beam was operated most of the time with 120 GeV/c negative pions. A large number of events with single beam tracks has been recorded for different values of the electrical parameters. A small proportion shows large clusters in one of the detector planes, in 0.15 % of events, followed by multiple tracks downstream as illustrated in fig. 18. This occurrence is compatible with the interaction cross section for pions in the 1.6 mm of material of the detector and its support. The pixel detectors provide an on-line pictorial description of such events. A histogram of the hit distribution over the detector plane is accumulated in fig. 19 and this gives an image of the beam as defined by the scintillators. The low background around the peak can be attributed to tracks from interactions as described above. The addition of a veto counter should make it possible to eliminate most of the events with multiplicity due to the interactions in upstream material.

TABLE 1 Distribution of multiple hits by # of rows and # of columns in 99184 events

# of colmns # of rows	1	2	3	4	5	6	7
1	84265	1221	8	1	-	-	-
2	11530	363	3	-	-	-	-
3	816	168	62	2	-	-	-
4	288	79	42	2	2	1	-
5	105	39	15	6	-	-	-
6	60	21	13	6	-	-	-
7	29	9	6	4	1	-	-
8	8	1	1	1	-	-	-
9	-	-	-	-	-	-	-

The total statistics of the hits in the middle plane for 99184 beam track events is shown in table 1. These data include some hits from multiple cluster events. If one selects only the clusters which are related to a beam track identified in the upstream and downstream planes the distribution of the cluster size in fig. 20 shows 88% single hits. The efficiency for the middle plane in this sample was determined at 99.8%.

3.1 Detectors of 150 μm thick

In the H6 beam we also tested the first pixel detector asemblies with a 150 μm thick sensitive silicon layer [5,6]. Because the signal from such a detector is only ~10^4 e-h pairs for minimum ionizing particles a low threshold of ~5000 e^- is needed in order to achieve 95% efficiency. For higher thresholds there is a loss of efficiency as illustrated in fig. 21.

3.2 Hit "propagation"

At low thresholds we discovered previously in the OmegaD chip that sometimes 'propagation' of a hit occurs on subsequent clock periods from one cell to the adjacent one in the direction of the output periphery of the array, along the column [6]. Such a propagated hit may be seen as background in a following event, and because the propagation always goes in the same direction, acumulation of spurious hits occurs towards one side. This phenomenon was particularly present in the first test of the thin detectors. The propagation was thought to be caused by digital cross-talk into the adjacent pixel from the reset signal at the end of the memory cycle. The use of a shielded reset line has practically eliminated this phenomenon in the Omega2 chip as can be seen in fig. 22 which shows the number of hits in a 6-ladder array for different delays between the event and the start of the 200 ns strobe width. In fig. 23 similar data have been taken at an exceptionally low threshold level of ~3000 e$^-$ and here a small proportion of "propagated" hits can still be seen at 700-800 ns strobe delay.

4. A 6-LADDER ARRAY IN THE 10 GEV TEST BEAM

The first 6-ladder array has been tested electrically and with a radioactive electron source in the laboratory and in the T9 beam with 10 GeV/c pions.

4.1 Testing in the laboratory

Prior to testing in the beam the operational parameters of the array have been studied in the laboratory using a radioactive electron source and an event trigger derived from a single scintillator placed behind the pixel detector array. A comprehensive study was made of the sensitivity of the adjustable parameters. The external voltages are multiplexed via 6 resistors and each current source then supplies the 6 chips on the corresponding vertical bus. Several of the results concerning threshold and delay timing have been shown already in sect. 2.3. The efficiency and the average number of hit pixels per triggered event caused by a traversing electron from a radioactive source are plotted in fig. 24 as a function of the comparator threshold setting Udis2. Up to a value of 4 V the efficiency is ~100% and goes down gently for larger thresholds. The proportion of double hits decreases steeply above 3.5 V but only a gradual loss occurs from 4 V upwards.

The efficiency and proportion of double hits as a function of the applied detector bias voltage are plotted in fig. 25. The total depletion voltage of the detector is 30 V and close to 100% efficiency is achieved from there upwards. There is a slight increase of double hits at higher bias.

4.2 Beam test

The 6-ladder array was positioned between 4 high-precision wirechambers and several scintillator planes which provided coincidence and position information for the beam events generated by 10 GeV/c particles. This beam could cover a fair part of the surface of the array as is shown in the scatter plot of fig. 26 where the hit pixels for 50 000 events are plotted on-line in a histogram with an approximate geometry of the 6 ladders. The detector pixel cells in the overlap region between readout chips are 1000 μm wide instead of 500 μm and the double count rate in these cells is visible as a darker band. This double count rate is particularly clear in the histogram of the projection of these data for each ladder in the direction of the columns, fig. 27. A similar dataset, not shown here, has been obtained in the upper part of the array and few columns were found to be "always-on" or dead, as can be seen e.g. in ladder 2, columns 67,68 and the upper part of ladder 4, columns 33, 34 and 35.

In the off-line analysis the data are corrected for the ladder geometry and a fiducial volume selection is made on the basis of the predicted position using the wirechamber information. Tracks that are predicted to be within 3 standard deviations from the edge of a ladder have been discarded from the sample. The remaining data are shown in fig. 28. The vertical dark bands have been eliminated by the geometrical correction. In the upper part are plotted the hits that could be associated with the beam tracks in 24148 events with only a single cluster of hits. In the lower part are plotted the hits in the **not**-associated cluster which were found in 757 events with two clusters of which the other one was associated with a good track. From this scatter plot it can be concluded that most of these spurious hits also are associated with the beam. Those 'spurious' particles are really detected by the pixel array during the 500 ns strobe time. They were not tracked by the wirechambers because these had only a 40 ns sensitive gate period. With a beam intensity of ~15000 in 300ms the expected background is 555 uncorrelated clusters in 24148 events. There might then be at most 200 real noise hits in this sample, for 25000 events and for 36k pixel cells. The upper limit for the incidence of Gaussian noise is then < 2 x 10-7 of the real hits.

A scintillating fiber allowed the definition of a small apparent beam spot of 10 mm width (~18 pixels of 500 μm + 2 pixels of 100 μm) and 2 mm height (~30 pixels). The sensitive area of a single ladder is 53 mm x 4.7 mm and covers easily the reduced beam spot. The on-line scatter plot is shown in fig. 29 with the corresponding column projection in fig. 30. The efficiency determined e.g. in ladder 3 was 99.4%. The cluster topology is described in table 2 for low, normal and high thresholds. There is only a small influence of the threshold on the double hits.

TABLE 2 Cluster Topology 6-ladder Array

	Low threshold			Normal threshold			High threshold		
# cols	1	2	> 2	1	2	> 2	1	2	> 2
# rows									
1	84.0	0.8	0	84.1	0.8	0	86.5	0.8	0
2	11.9	0.3	0.12	11.8	0.3	0.15	9.6	0.3	0.14
> 2	2.3	0.4	0.17	2.2	0.4	0.22	2.1	0.3	0.21

These results corroborate essentially those reported in table 1 for single chip assemblies where 85% of single hits were found. The performance of the array apparently does not suffer from unexpected interference effects due to the larger number of chips. The double hits consist predominantly of 2 rows (11.8%). If one supposes that double hits are caused by particles crossing the boundary of a pixel one finds a sensitive edge region of 4.5 μm on either side. Note that in the test beams the particles cross the detectors under an angle very close to 90°. If double hits are caused by geometry alone there should be 1.6% of double hits with 2 columns and these are, at first sight, with 0.8% under-represented. In the single assembly test 1.2% was found. However, the data in the ladder test are biased because the small scintillator intentionally was placed across the region between two chips (see fig. 29) in order to detect any possible inefficiency of the "stitching" region. Therefore there is less boundary between columns, and therefore fewer 'double column' hits. Nevertheless, there still may be a slight deficit of 'double column' events and this has to be investigated in more detail.

In this first array the number of dead pixels and masked noisy pixels was ~700 which results in a dead area of less than 2%.

5. FIRST USE OF A DOUBLE ARRAY IN THE OMEGA WA97 EXPERIMENT

A complete, double array has been installed in the WA97 experiment in the Omega spectrometer in November 1993 during the test run with protons. A sketch of the position of the double array between the other Omega detectors is shown in fig. 31. Silicon microstrip detectors with 50 μm and 100 μm pitch allowed track reconstruction in both y- and z-coordinates with a precision at the pixel plane of respectively 15 μm and 20 μm. The distributions of residuals shown in fig. 32 have standard deviations of 157 μm along y and 30 μm along z. These numbers allow to deduce a precision of respectively 150 μm and 22 μm in the pixel detector measurement , which values agree fairly well with the expected values based on the $1/\sqrt{12}$ rule.

If an event selection is made with only double hits in the pixel plane the distribution of residuals has a standard deviation of 22.6 μm (fig. 33) which indicates a <10 μm precision of the coordinate determined by the pixel detector.

It has been again confirmed that most events with a reconstructed beam particle are characterized by a single cluster with a single hit. The proportion of double hits and number of clusters has been studied as a function of the threshold adjustment and the applied detector bias voltage. Data have been taken with focussed and defocussed beam and with an interaction trigger which required a large energy deposit in a scintillator placed just in front of the pixel detector plane (fig. 31). A complete analysis of this run will be available later.

By defocussing the beam it was possible to 'illuminate' practically the complete array and the less efficient or dead areas become clearly visible in fig. 34 which shows a scatter plot for 50 000 events. The vertical dark bands due to the larger pixels are again clearly seen as well as some dead columns. 3 complete readout chips see few or no hits but they did not disturb the other chips in their columns. Several other chips have a reduced efficiency towards the upper part. Most of these are on the 2nd array that before its use was not as much characterized as the first one. Although several adjustable parameters have been varied during the run it is possible that an improved operating condition could have been established with sufficient preparation. In total, about 10% of the pixels were inoperative, most of them on the second array.

6. CONCLUSIONS

For the first time a large, active pixel detector array, consisting of 72 readout chips associated with 72576 sensor elements has been operated in a particle physics experiment. The success of such a device depends on the design of the electronics functions as well as on a careful preliminary characterization of the operational parameters of the finished array.

We have elaborated on the study of threshold adjustments, timing, etc. in order to show the importance of optimization in this multiparameter detector device. A precision better than 22 µm and an efficiency of >99% were measured on the 'good' regions of the detector. Bad regions accounted for 2% of the area in the first array and for 20% of the area in the second one. A major cause for loss of efficiency was found to be improper timing for the various delays. One has to recognize and correct the variations in signal transmission due to the variations in semiconductor chip processing per wafer or per lot. In these first arrays it was found that line resistances on the mechanical support plate are an important factor that influences the settings of the delays on the chips. This will be easy to remedy in the following arrays. In larger systems it might be necessary to adjust timing and thresholds locally on each "ladder" or even on each chip, using built-in feedback loops.

The incidence of spurious noise hits is found to be $<<10^{-6}$, as expected from the electrical noise measurements giving 170 e^- r.m.s. Some pixels (here ~1%), however, are "always-on" and hardware masking of these is essential in order to limit the data transmission to manageable proportions, particularly in a large area system which may have $>10^8$ sensor elements.

The future introduction of on-chip timing adjustment, masking, zero suppression, etc. will make the active pixel detector increasingly "intelligent" and at the same time this could widen the acceptance limits for chips from different wafers or different lots, and increase the yield in production.

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References

[1] F. Anghinolfi, P. Aspell, K. Bass, W. Beusch, L. Bosisio, C. Boutonnet, P. Burger, M. Campbell, E. Chesi, C. Claeys, J.C. Clemens, M. Cohen Solal, I. Debusschere, P. Delpierre, D. Di Bari, B. Dierickx, C.C. Enz, E. Focardi, F. Forti, Y. Gally, M. Glaser, T. Gys, M.C. Habrard, E.H.M. Heijne, L. Hermans, R. Hurst, P. Inzani, J.J. Jæger, P. Jarron, F. Krummenacher, F. Lemeilleur, V. Lenti, V. Manzari, G. Meddeler, M. Morando, A. Munns, F. Nava, F. Navach, C. Neyer, G. Ottaviani, F. Pellegrini, F. Pengg, R. Perego, M. Pindo, R. Potheau, E. Quercigh, N. Redaelli, L. Rossi, D. Sauvage, G. Segato, S. Simone, G. Stefanini, G. Tonelli, G. Vanstraelen, G. Vegni, H. Verweij, G.M. Viertel and J. Waisbard

A 1006 element hybrid silicon pixel detector with strobed binary output, IEEE Trans. Nucl. Sci. NS-39 (1992) 654

[2] Erik H.M. Heijne

Imaging with 2D and 3D integrated semiconductor detectors using VLSI technology,

Physica Medica 9 (1993) 109 (Proc.Conf. on Physics in Medecine and Biology)

[3] M. Campbell, F. Antinori, H. Beker, W. Beusch, E. Chesi, E.H.M. Heijne, J. Heuser, P. Jarron, T. Karttaavi, L. Lopez, G. Meddeler, A. Menetrey, P. Middelkamp, C. Neyer, F. Pengg, M. Pindo, E. Quercigh, S. Simone and H. Verweij

Development of a pixel readout chip compatible with large area coverage, to be published in NIM (Hiroshima Symp. 1993)

[4] D.J. Pedder

Flip-chip solder bonding for advanced device structures, Plessey Research Rev. 1989, 69

[5] E.H.M. Heijne, F. Antinori, H. Beker, G. Batignani, W. Beusch,V. Bonvicini, L. Bosisio, C. Boutonnet, P. Burger, M. Campbell, P. Cantoni, M.G. Catanesi, E. Chesi, C. Claeys, J.C. Clemens, M. Cohen Solal, G. Darbo, C. DaVia', I. Debusschere, P. Delpierre, D. Di Bari, S. Di Liberto, B. Dierickx, C.C. Enz, E. Focardi, F. Forti, Y. Gally, M. Glaser, T. Gys, M.C. Habrard, G. Hallewell, L. Hermans, J. Heuser, R. Hurst, P. Inzani, J.J. Jæger, P. Jarron, T. Karttaavi, S. Kersten, F. Krummenacher, R. Leitner, F. Lemeilleur, V. Lenti, M. Letheren, M. Lokajicek, D. Loukas, M. Macdermott, G. Maggi, V. Manzari, P. Martinengo, G. Meddeler,F. Meddi, A. Mekkaoui, A. Menetrey, P. Middelkamp, M. Morando, A. Munns, P. Musico, F. Nava, F. Navach, C. Neyer, F. Pellegrini, F. Pengg, R. Perego, M. Pindo, S. Pospisil, R. Potheau, E. Quercigh, N. Redaelli, J. Ridky, L. Rossi, D. Sauvage, G. Segato, S. Simone, B. Sopko, G. Stefanini, V. Strakos, P. Tempesta, G. Tonelli, G. Vegni, H. Verweij, G.M. Viertel, V. Vrba and J. Waisbard

Development of silicon micropattern pixel detectors, submitted to NIM (PSD3, London, Sept 1993)

[6] T. Chábera, J. Kubasta, R. Leitner, M. Lokajicek, S. Pospisil, J. Ridky and V. Vrba

Analysis of data from 150 µm and 300 µm pixel detectors, RD19 Technical note*21 31 May 1993

Figure Captions

Fig. 1 Photograph of a single array consisting of 6 ladders with the associated local driver card and the VME readout module(not shown). This array has 32288 detecting elements and a second, identical array, staggered over the open 'slots' completes a full detector plane.

Fig. 2 Picture of the front side of the detector matrix showing in the middle the region between the two rightmost readout chips. The cells which are to be connected to the edge columns of the readout chips are twice as long: 1000 µm instead of 500 µm. The height of the cells is 75 µm everywhere. A close up is shown in the lower part.

Fig. 3 Photograph of a complete array. One can see the dark back side of the detector chips and the bias filter capacitors besides each ladder. The vertical lines are the connecting lines on the ceramic, as shown in fig. 5.

Fig. 4 Schematic drawing in side-view of a fully hermetic, "logical" detector plane. The 3 mm thick ceramic is U-shaped and the detectors are mounted on the open area.

Fig. 5 Layout of the connecting lines on the thin-film ceramic plate which carries the array of 6 detector ladders with altogether 36 readout chips.

Fig. 6 Drawing of the assembly of ceramic support plate, supply and bus conductors, isolation ceramic, readout chips and detector ladder from bottom to top. The thicknesses are indicated in µm.

Fig. 7 Photograph taken during the processing of the ceramic support plate on which the first ladder is positioned and secured, before heat treatment in order to cure the non-conductive epoxy.

Fig. 8 Close-up of the array. The buslines on the light ceramic plate run vertically underneath the ladders. Bonding wires can be seen connecting the bondpads on the readout chips to these buslines.

Fig. 9 Threshold at 50% countrate of electrical pulses in a single Omega2 chip as a function of the external threshold supply voltage Udis2 which is transformed in a current Idis2 via a 100 kΩ resistor. E.g. Udis2=5V is supplied to obtain Idis2=50 µA. The other external settings were Idis1=30 µA, Ifn=-3.5 µA, Idn=8µA and Iqa=-80 µA. Absolute calibration points are shown at 22 keV, 60 keV and 122 keV and these have been used to fit the left-hand vertical scale in electrons.

Fig. 10 Average threshold at 100% efficiency for a 6-ladder array measured with an electron source, as a function of the adjustable voltage Udis2. The other external settings were Udis1=3.57 V, Ufn=0.5 V, Udn=2.41 V, Uqa=0.7 V, Vbias=40 V, strobe duration 500 ns and strobe delay 800 ns.

Fig. 11 Timing sequence with internal delay and external strobe signal.

Fig. 12 Average delay for a 6-ladder array as a function of the adjustable voltage Udn. The other external settings were as in fig. 10 with Udis2=3.75 V. The strobe durations were respectively 800 ns, 500 ns and 400 ns.

Fig. 13 Measured number of counts for each ladder as a function of the external strobe delay. The optimal values are not identical for each ladder. The duration of the strobe signal itself was 500 ns.

Fig. 14 Histogram of delays in the pipelines averaged for each chip in the array. A top (ladder 1)-bottom (ladder 6) non-uniformity can be observed.

Fig. 15 Block diagram for the intermediate readout card (top) and the VME board at the bottom.

Fig. 16 Readout sequence of the chips. 1A and 1B are read first, then 2A and 2B, etc.

Fig. 17 Setup of the telescope of 3 single assemblies in the H6 test beam, with various scintillators for beam definition. Beam particles are defined by the coincidence of several small scintillators, in particular 2 crossed scintillating fibers PM3 and PM4. The resulting spot measures only ~1 mm x 2 mm.

Fig. 18 Pictorial representation of the statistics of single, double and multi-hit clusters in the beam test with 3 detector planes. It shows the powerful pattern recognition of the micropattern detector even for large numbers of hits in a cluster.

Fig. 19 Histogram of the beam spot consisting of the coordinates of hits as recorded by a 300 μm thick micropattern detector.

Fig. 20 Histogram of the cluster size for single beam tracks in a 300 μm thick detector.

Fig. 21 Comparison of detector efficiency for a 150 μm and a 300 μm thick detector as a function of the discriminator threshold.

Fig. 22 Scan of the delay time after which the 200 ns strobe signal is issued. Each point represents 5000 event triggers, generated by an electron traversing the detector. External settings for low threshold: Udis1=1.5 V, Udis2=1.6 V, Uqa=1.5 V, Udn=1.1 V, Vbias=50 V.

Fig. 23 Idem as fig. 22 but with a very low threshold of ~3000 electrons: Udis2=1.4 V.

Fig. 24 Efficiency and number of hits per event for a 6-ladder array as a function of external threshold voltage Udis2. Each point represents 2000 triggers, strobe duration was 500 ns and strobe delay 50 ns. Udis1=3.57 V. Udn=2.4 V.

Fig. 25 Efficiency and number of hits per event for a 6-ladder array as a function of detector bias voltage Vbias. Udis1=Udis2=1.5 V, Udn=1.1 V, strobe duration 200 ns, strobe delay 150 ns.

Fig. 26 On-line scatter plot of the hits from 50000 events in the 6-ladder array. The dark bands are explained in the text.

Fig. 27 Projection of the hits in each ladder in fig. 26 in the direction of the columns. Note the change of the vertical scales from ladder to ladder.

Fig. 28 Top: Off-line representation of selected data from fig. 26, geometrically corrected. Only hits from single cluster events are plotted.
Bottom: Idem for 2-cluster events with only those hits that are **not** associated with the wirechamber-determined beam track. These hits are nevertheless correlated with the beam position and can be explained by the longer strobe time of the pixel array.

Fig. 29 On-line scatter plot of the hits with the scintillating fiber in the event trigger. The fiber is covering the “stitching”area between 2 readout chips.

Fig. 30 Projection of the hits of fig. 29 in the direction of the columns.

Fig. 31 The layout of the pixel detector and microstrip vertex detectors in the Omega WA97 run in November 1993.

Fig. 32 Histograms of the distribution of residual values between predicted and measured coordinates in the y- and z-projection (see fig.31). Standard deviations of 157,1 μm (y) and 30.5 μm (z) are calculated which lead to a precision of the pixel detector of 150 μm and 22 μm in the y- resp. z directions.

Fig. 33 Distribution as in fig. 32 but for selected events with 2 adjacent row cells hit in the pixel detector. The standard deviation is now only 22.6 μm giving a precision better than 10 μm in the pixel detector.

Fig. 34 Scatter plot for a complete, double array with 72 readout chips. The separations between the chips are visible as vertical, dark bands.

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1	84265	1221	8	1	-	-	-
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5	105	39	15	6	-	-	-
6	60	21	13	6	-	-	-
7	29	9	6	4	1	-	-
8	8	1	1	1	-	-	-
9	-	-	-	-	-	-	-

TABLE 2 Cluster Topology 6-ladder Array

	Low threshold			Normal threshold			High threshold		
# cols	1	2	> 2	1	2	> 2	1	2	> 2
# rows									
1	84.0	0.8	0	84.1	0.8	0	86.5	0.8	0
2	11.9	0.3	0.12	11.8	0.3	0.15	9.6	0.3	0.14
> 2	2.3	0.4	0.17	2.2	0.4	0.22	2.1	0.3	0.21

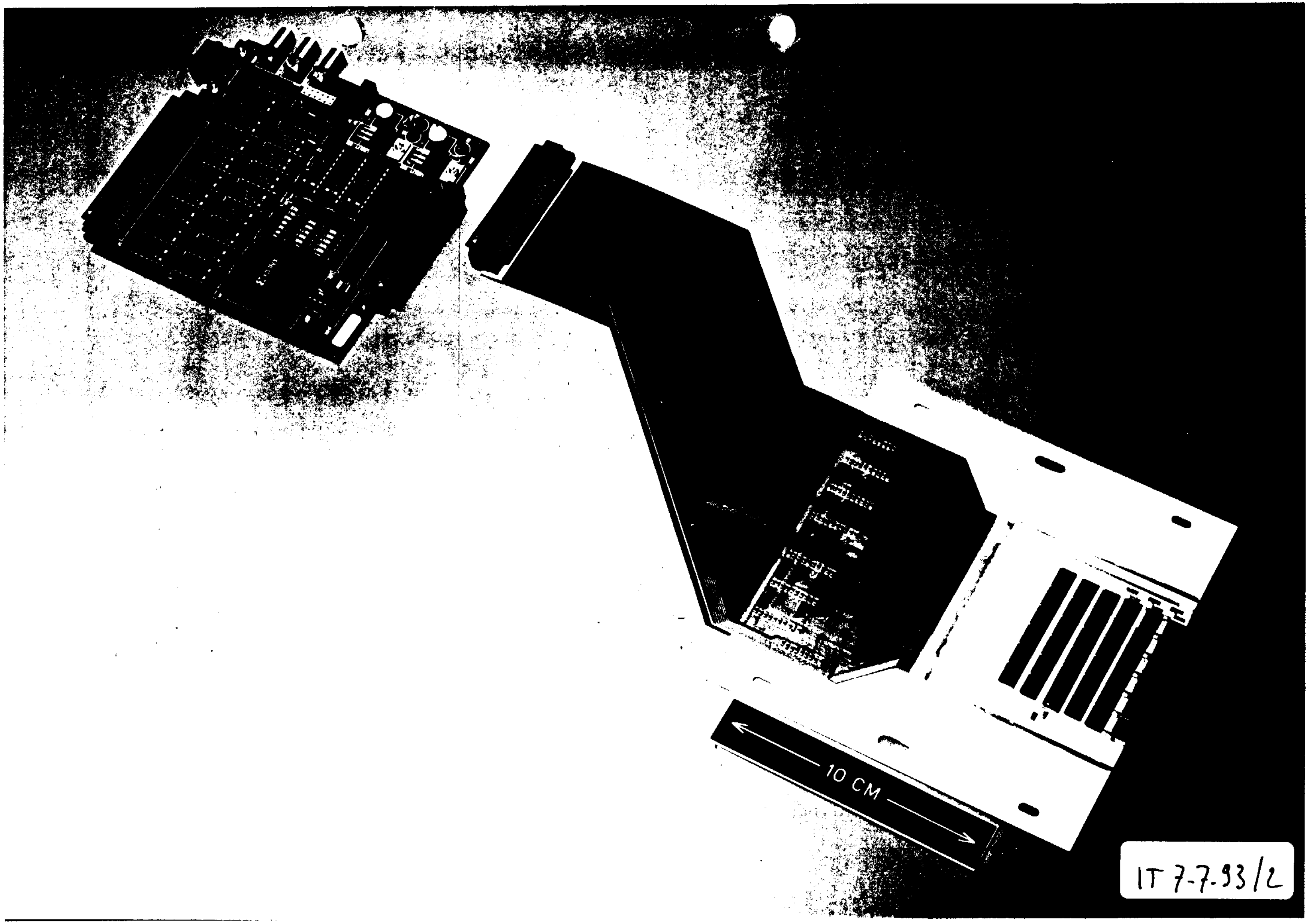


Fig. 1 Photograph of a single array consisting of 6 ladders with the associated local driver card and the VME readout module (not shown). This array has 32288 detecting elements and a second, identical array, staggered over the open 'slots' completes a full detector plane.

Fig. 2 Picture of the front side of the detector matrix showing in the middle the region between the two rightmost readout chips. The cells which are to be connected to the edge columns of the readout chips are twice as long: 1000 μm instead of 500 μm. The height of the cells is 75 μm everywhere. A close up is shown in the lower part.

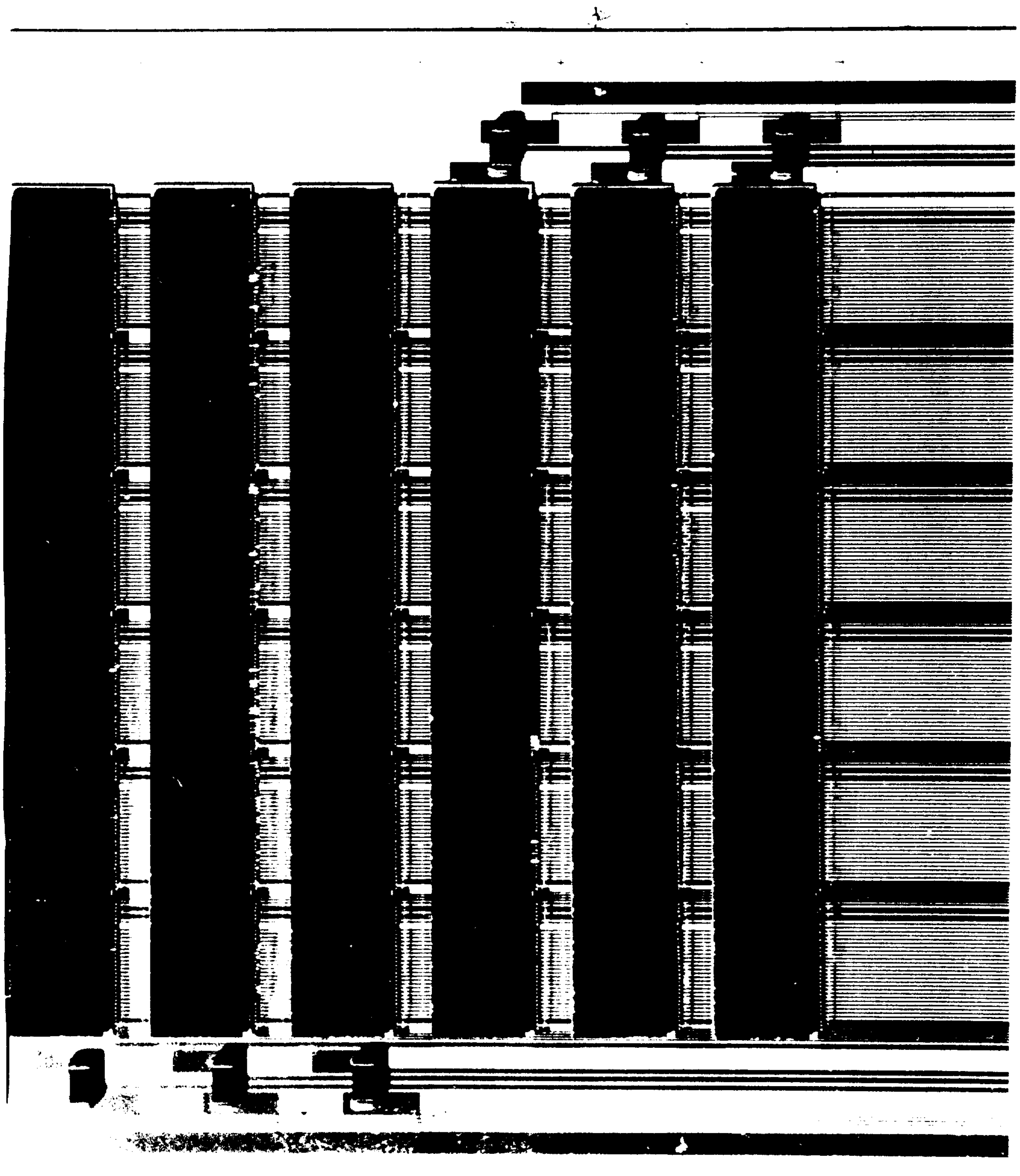


Fig. 3 Photograph of a complete array. One can see the dark back side of the detector chips and the bias filter capacitors besides each ladder. The vertical lines are the connecting lines on the ceramic, as shown in fig. 5.

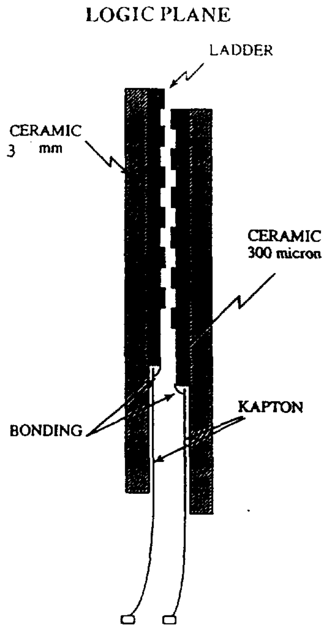


Fig. 4 Schematic drawing in side-view of a fully hermetic, "logical" detector plane. The 3 mm thick ceramic is U-shaped and the detectors are mounted on the open area.

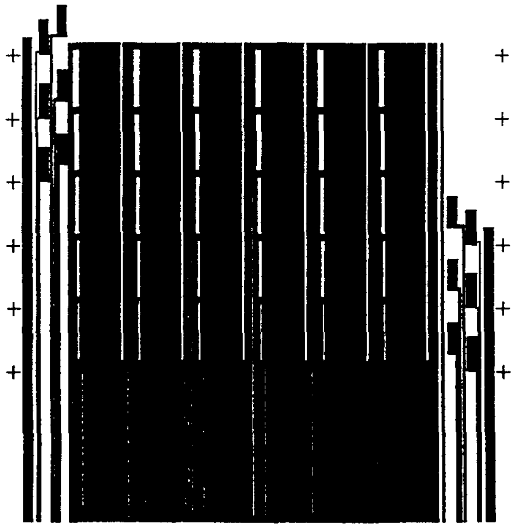


Fig. 5 Layout of the connecting lines on the thin-film ceramic plate which carries the array of 6 detector ladders with altogether 36 readout chips

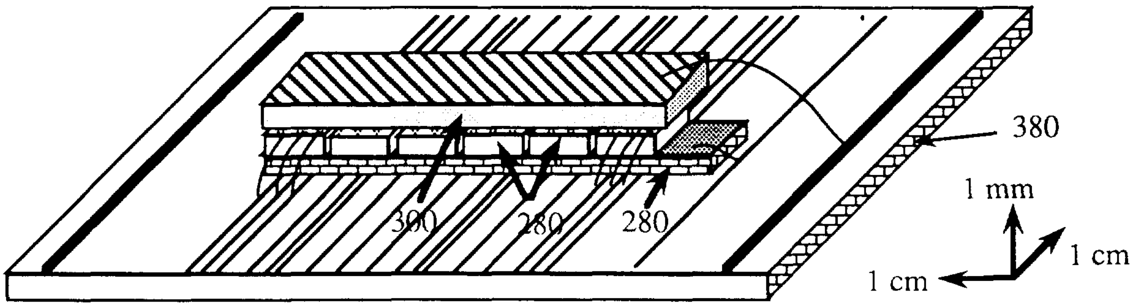


Fig. 6 Drawing of the assembly of ceramic support plate, supply and bus conductors, isolation ceramic, readout chips and detector ladder, from bottom to top. The thicknesses are indicated in µm.

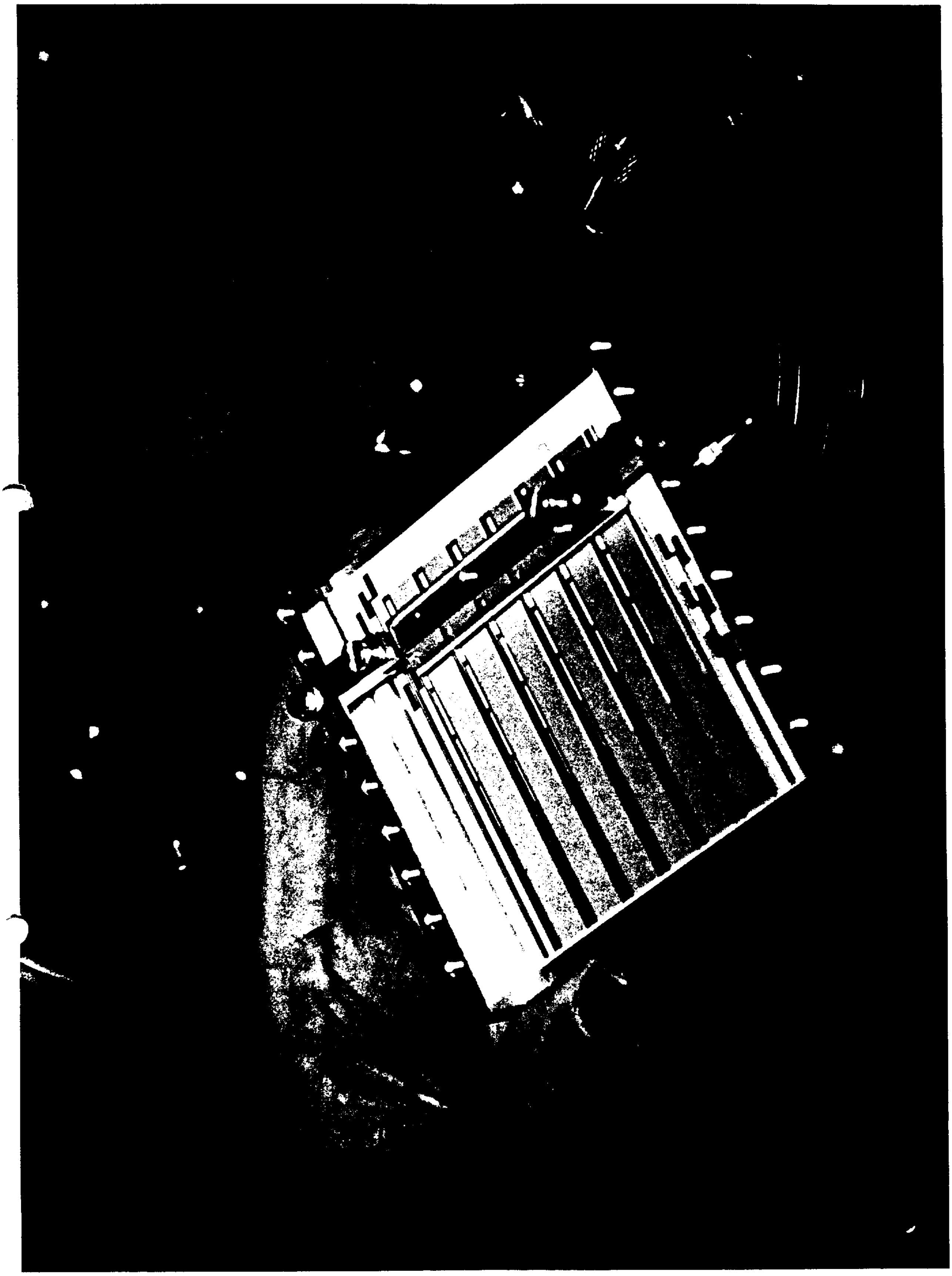


Fig. 7 Photograph taken during the processing of the ceramic support plate on which the first ladder is positioned and secured, before heat treatment in order to cure the non-conductive epoxy.

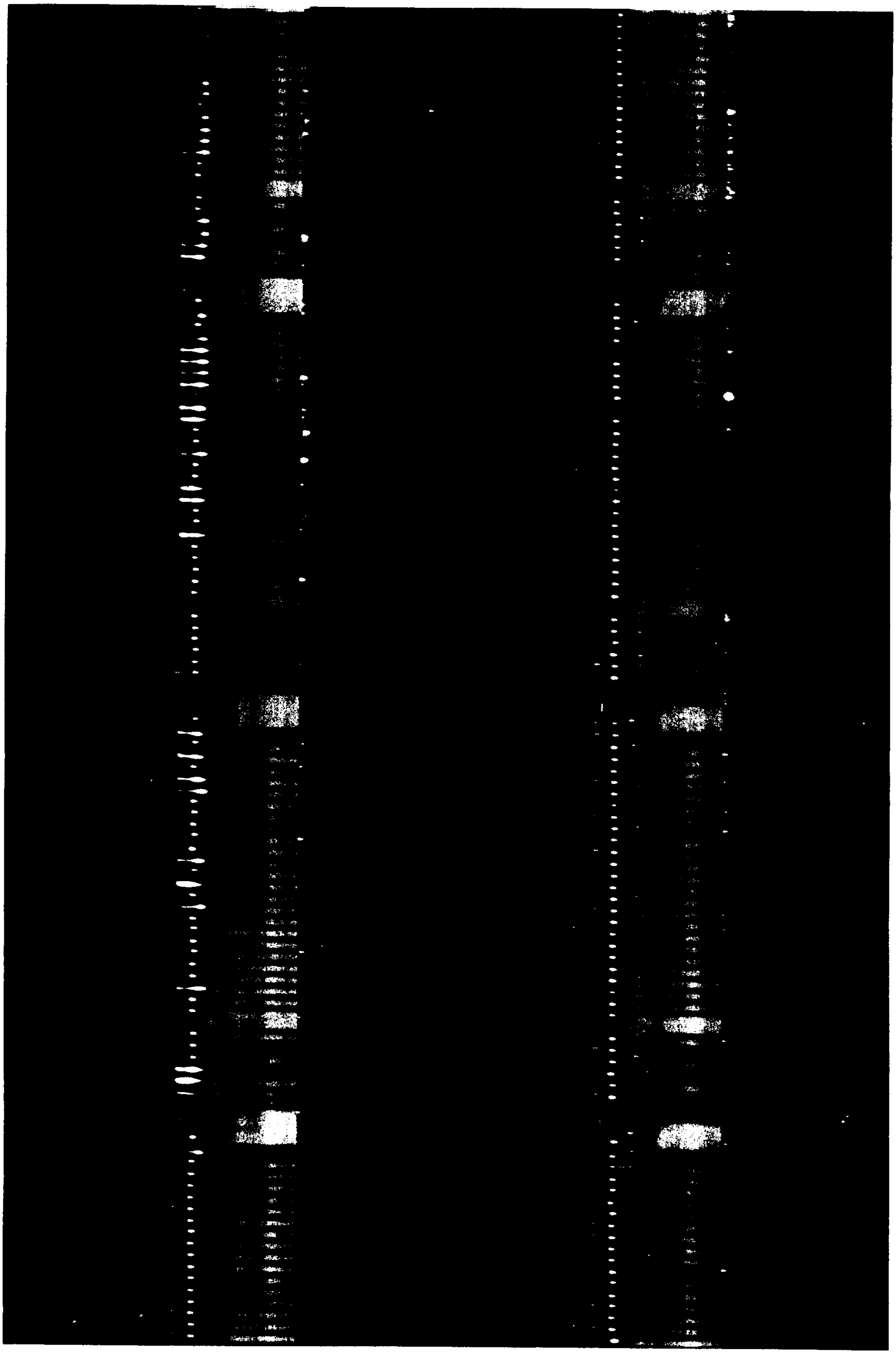


Fig. 8 Close-up of the array. The buslines on the light ceramic plate run vertically underneath the ladders. Bonding wires can be seen connecting the bondpads on the readout chips to these buslines.

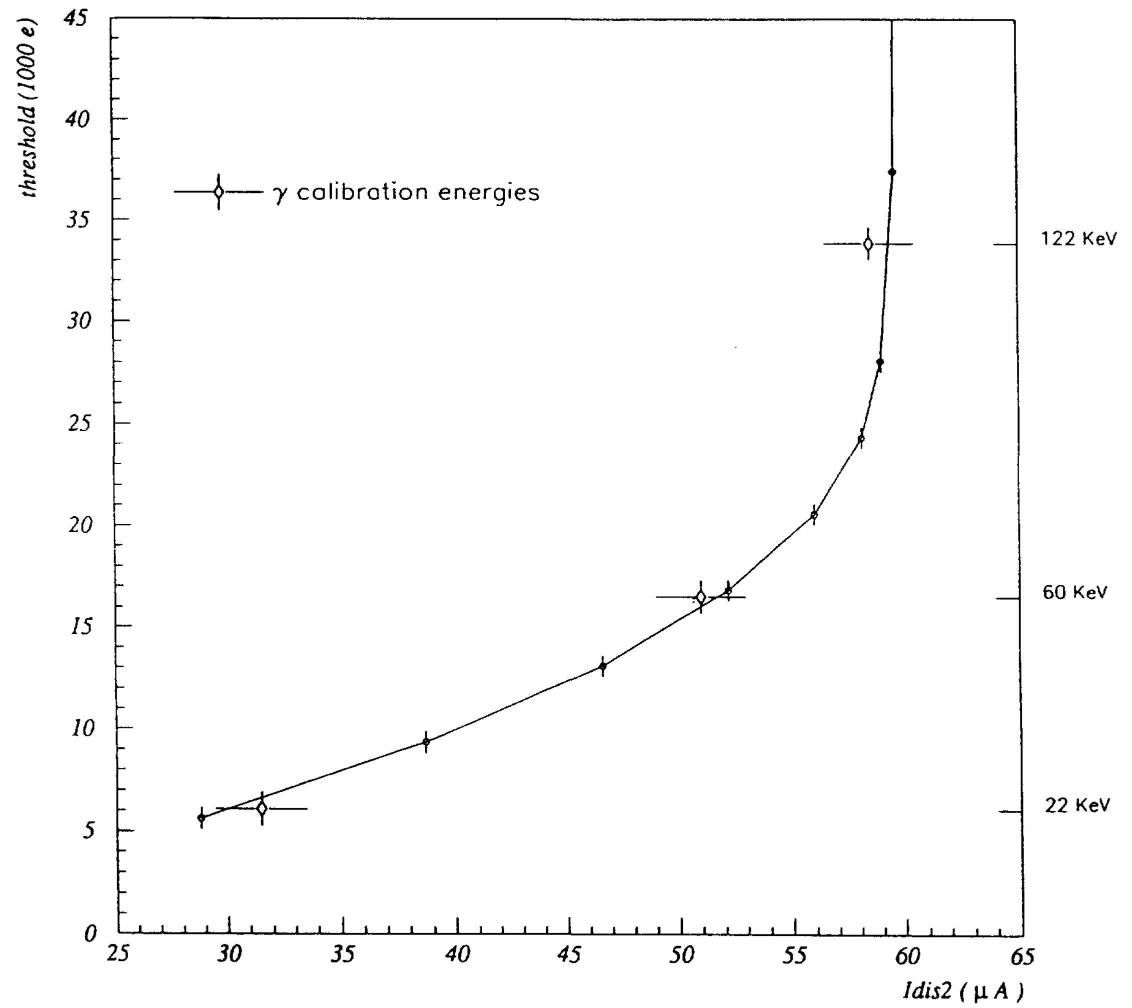


Fig. 9 Threshold at 50% countrate of electrical pulses in a single Omega2 chip as a function of the external threshold supply voltage Udis2 which is transformed in a current Idis2 via a 100 kΩ resistor. E.g. Udis2=5V is supplied to obtain Idis2=50 μA. The other external settings were Idis1=30 μA, Ifn=-3.5 μA, Idn=8μA and Iqa=-80 μA. Absolute calibration points are shown at 22 keV, 60 keV and 122 keV and these have been used to fit the left-hand vertical scale in electrons.

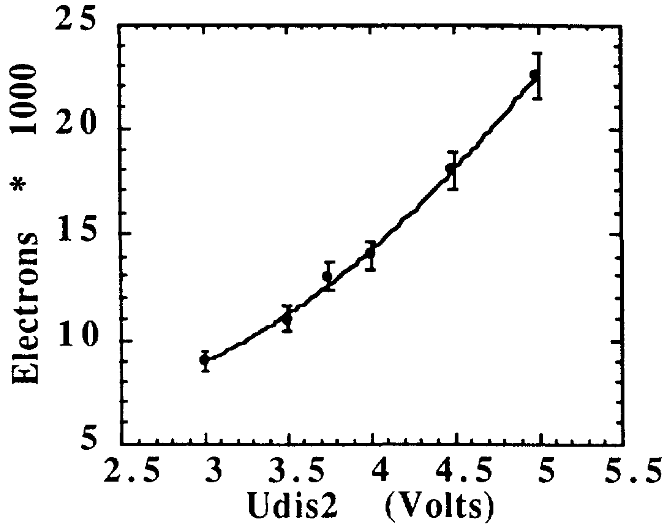


Fig. 10 Average threshold at 100% efficiency for a 6-ladder array measured with an electron source, as a function of the adjustable voltage Udis2. The other external settings were Udis1=3.57 V, Ufn=0.5 V, Udn=2.41 V, Uqa=0.7 V, Vbias=40 V, strobe duration 500 ns and strobe delay 800 ns.

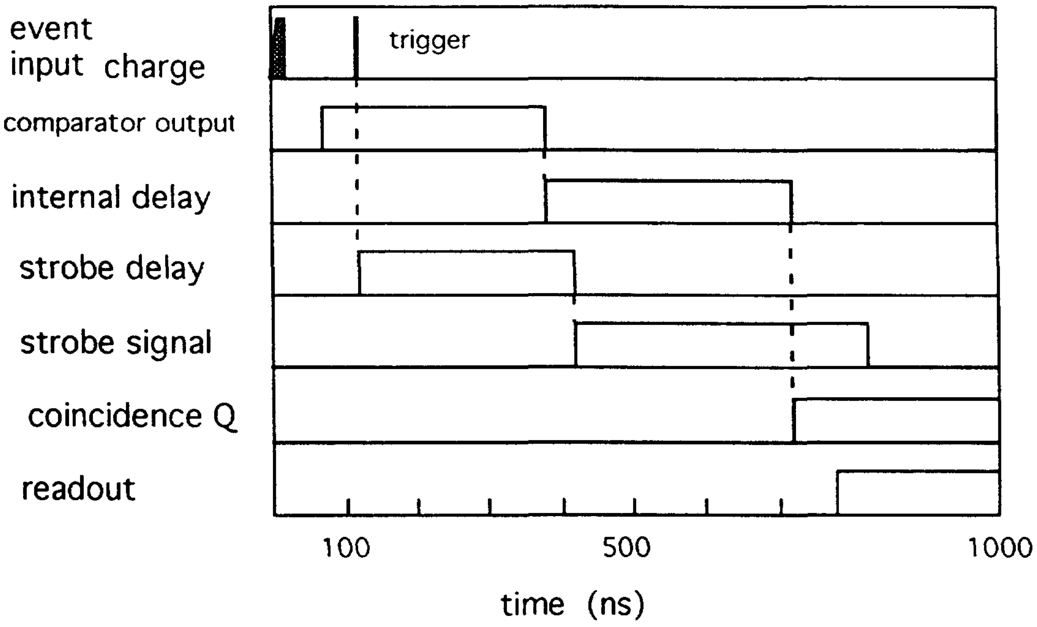


Fig. 11 Timing sequence with internal delay and external strobe signal.

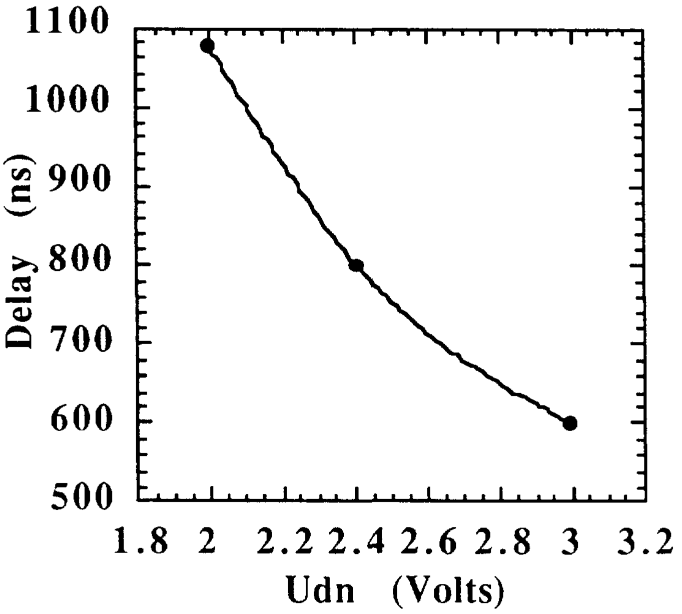


Fig. 12 Average delay for a 6-ladder array as a function of the adjustable voltage Udn. The other external settings were as in fig. 11 with Udis2=3.75 V. The strobe durations were respectively 800 ns, 500 ns and 400 ns.

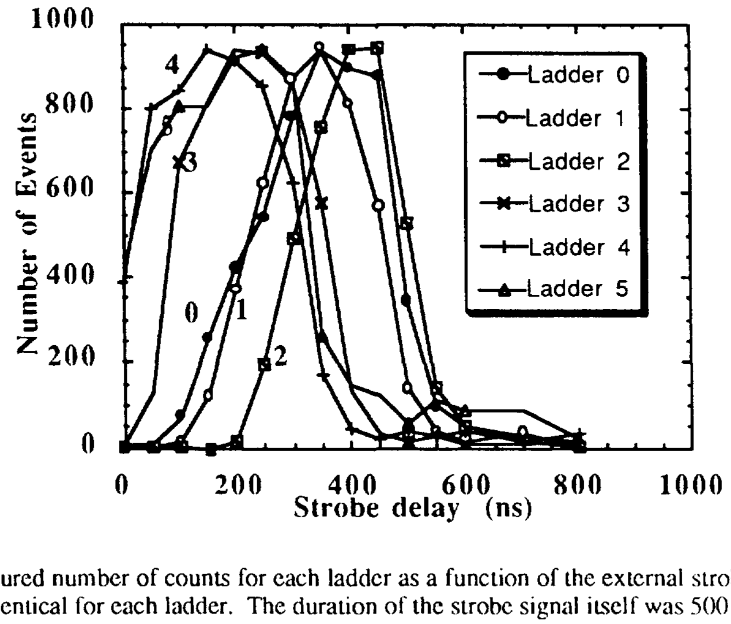


Fig. 13 Measured number of counts for each ladder as a function of the external strobe delay. The optimal values are not identical for each ladder. The duration of the strobe signal itself was 500 ns.

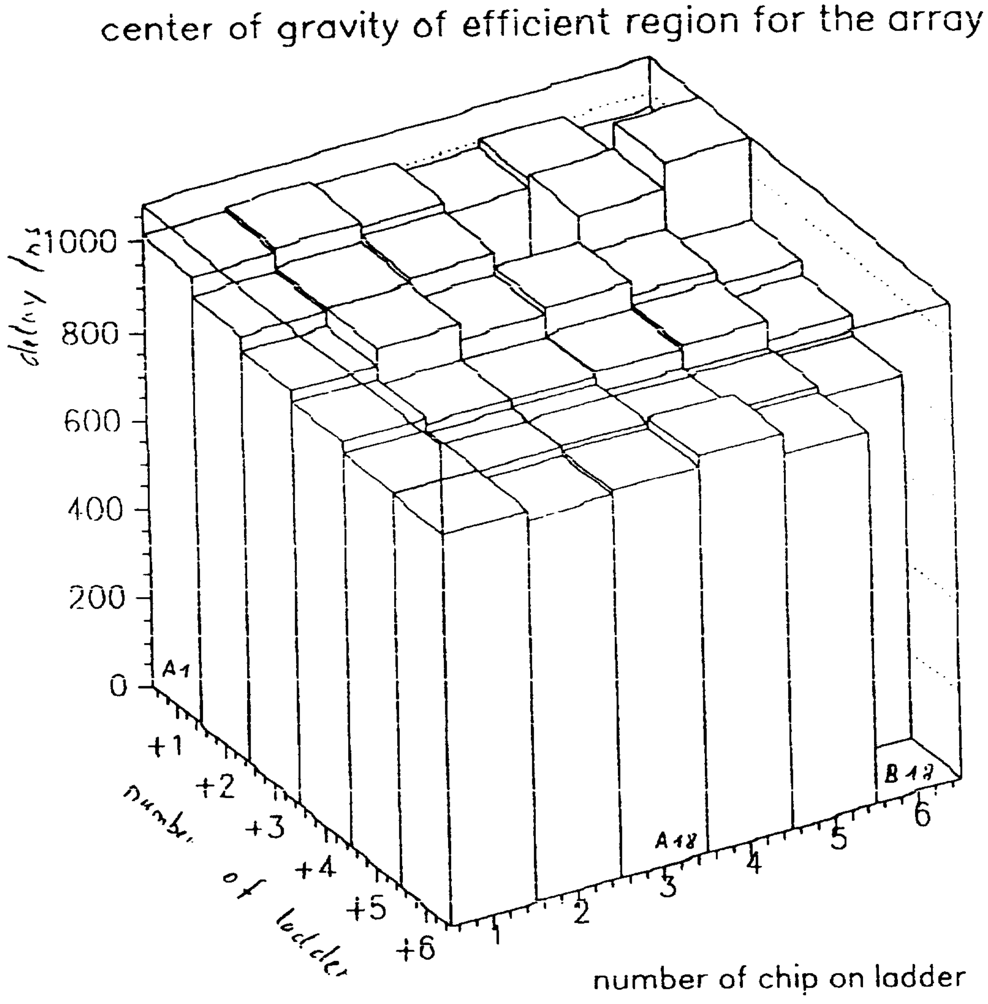


Fig. 14 Histogram of delays in the pipelines averaged for each chip in the array. A top (ladder 1)-bottom (ladder 6) non-uniformity can be observed.

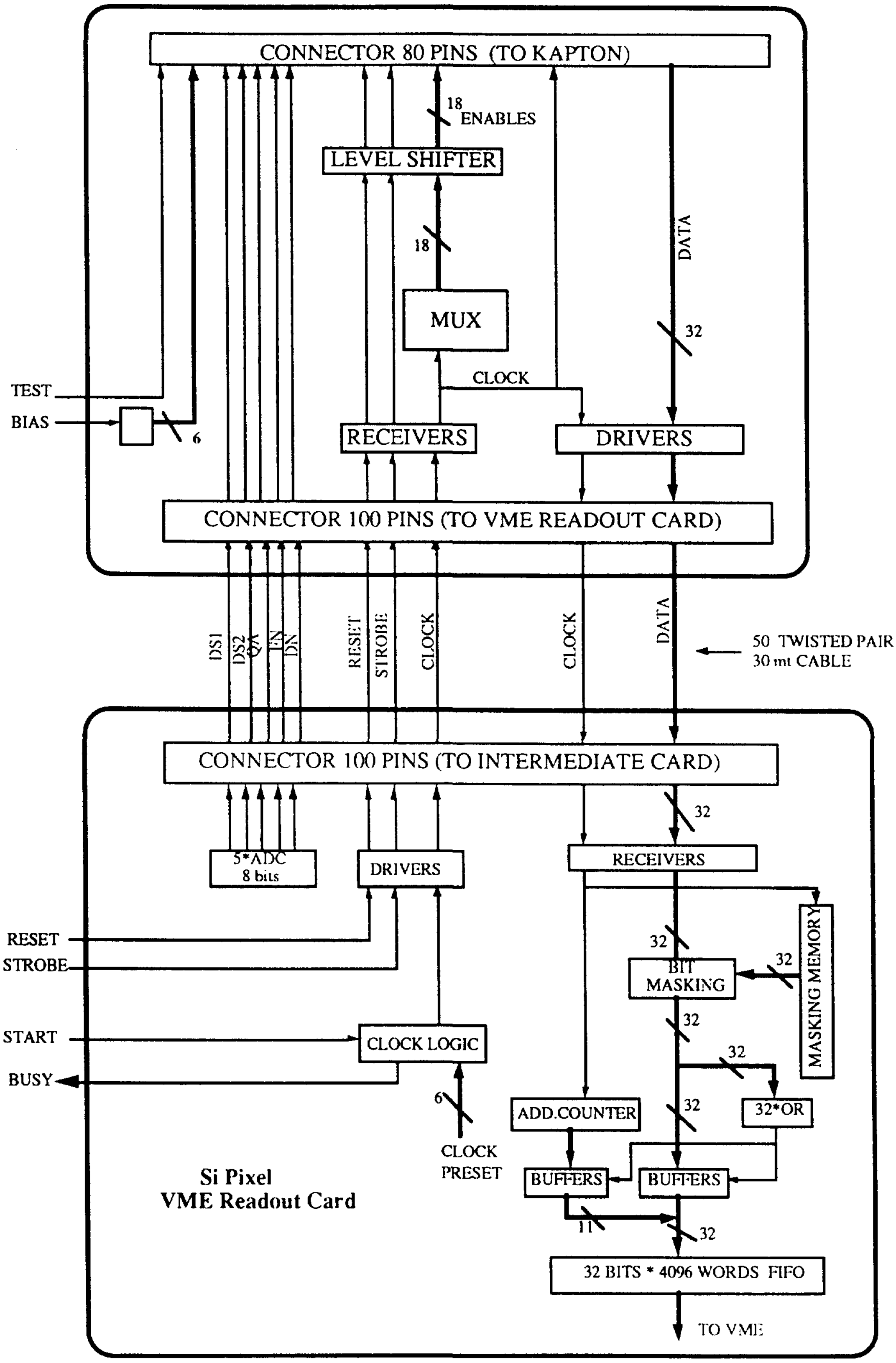


Fig. 16 Block diagram for the intermediate readout card (top) and the VME board at the bottom.

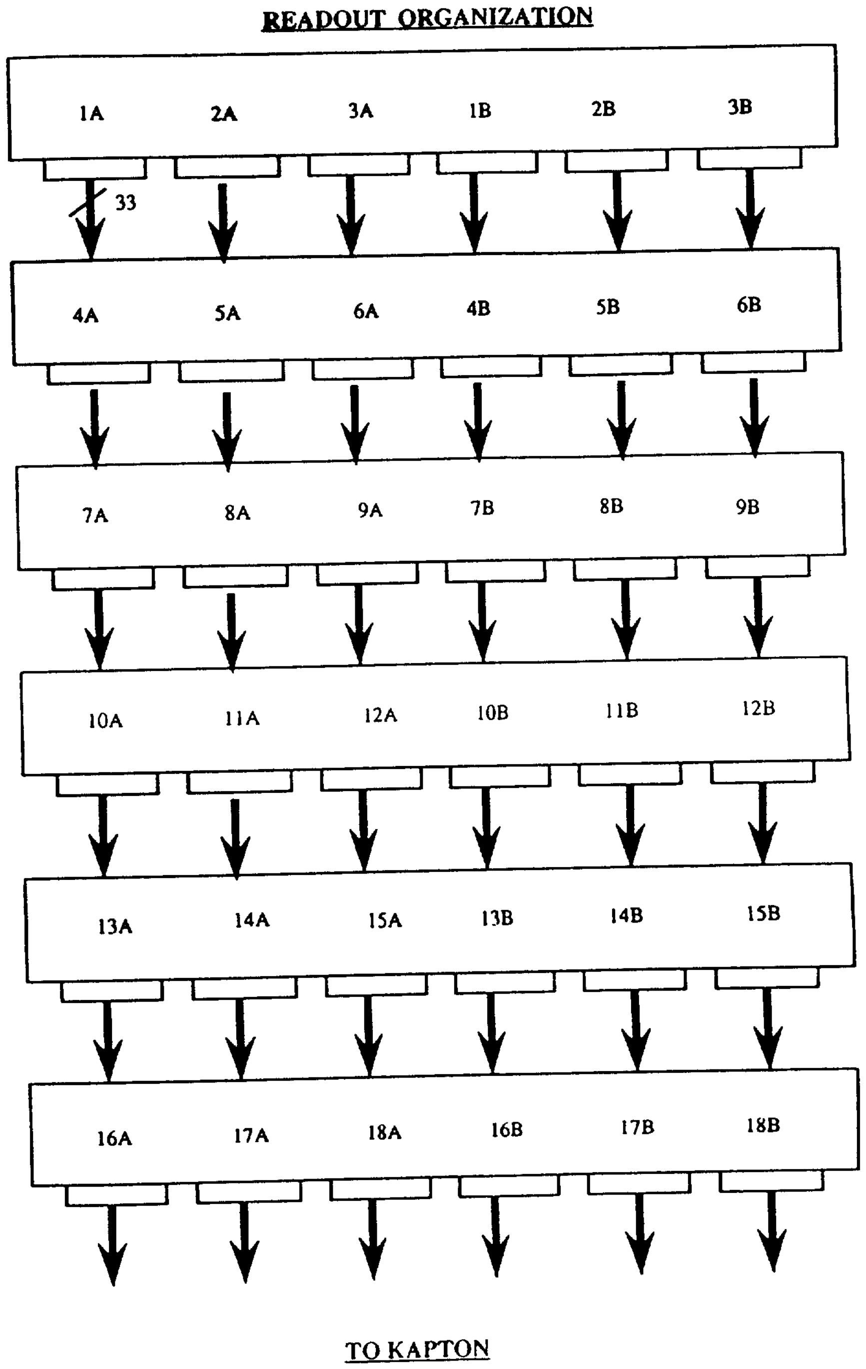


Fig. 17 Readout sequence of the chips. 1A and 1B are read first, then 2A and 2B, etc.

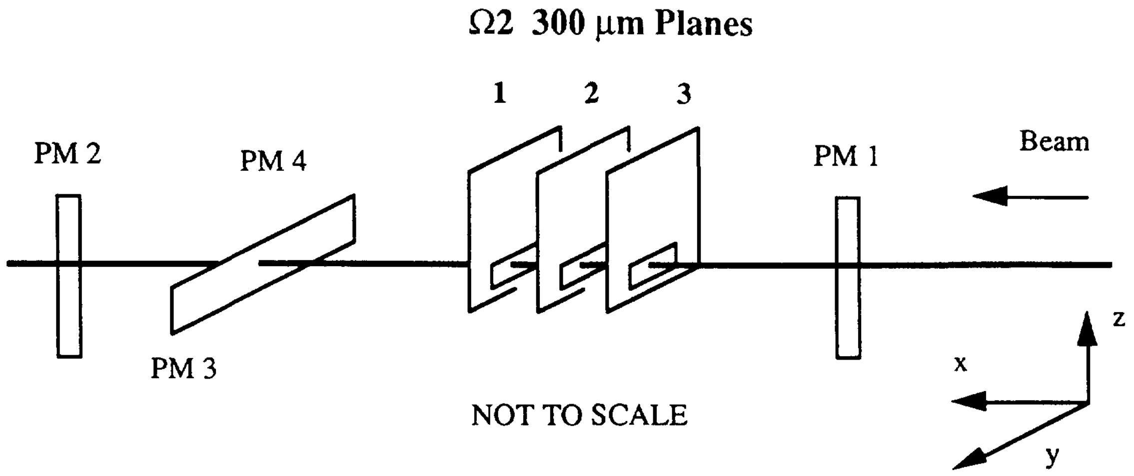


Fig. 18 Setup of the telescope of 3 single assemblies in the H6 test beam, with various scintillators for beam definition. Beam particles are defined by the coincidence of several small scintillators. The resulting spot measures only ~1 mm x 2 mm.

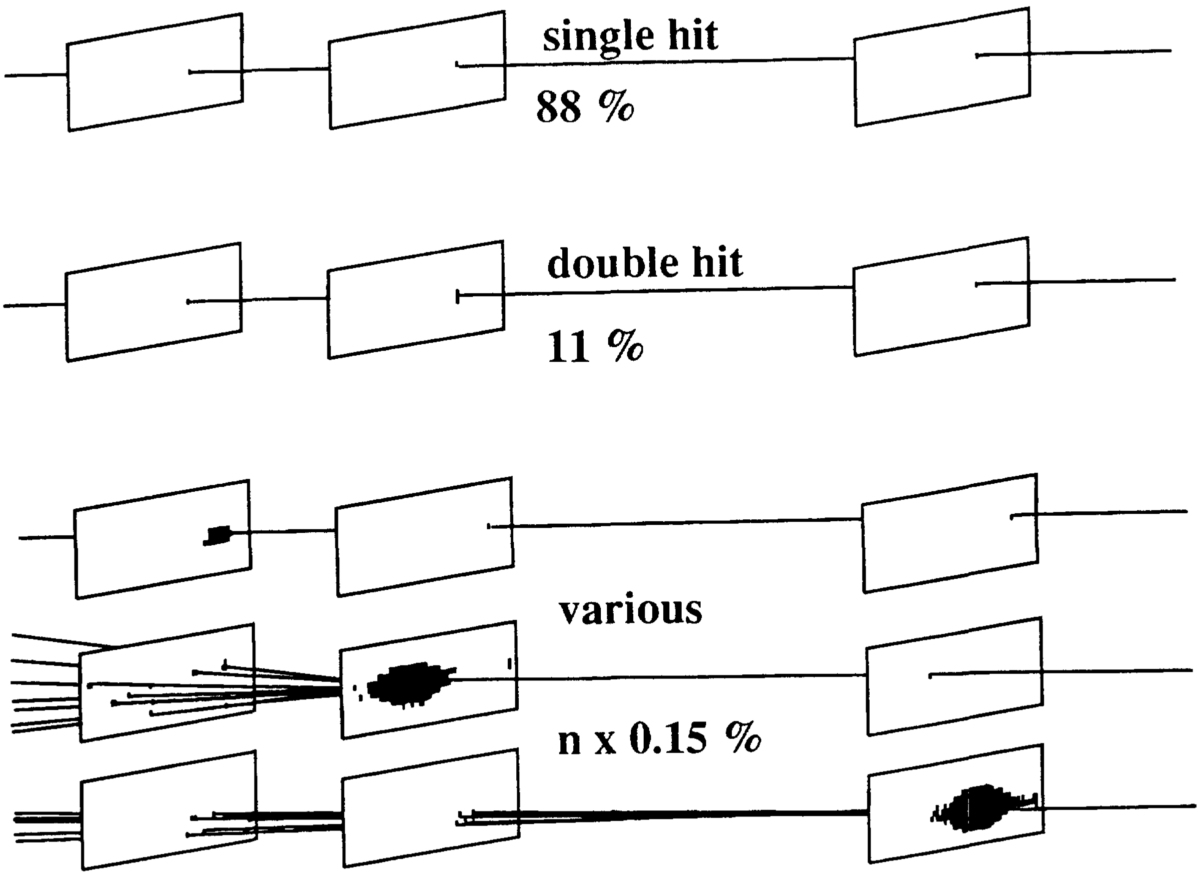


Fig. 19 Pictorial representation of the statistics of single and multi-hit clusters in the beam test with 3 detector planes. It shows the powerful pattern recognition of the micropattern detector even for large numbers of hits in a cluster.

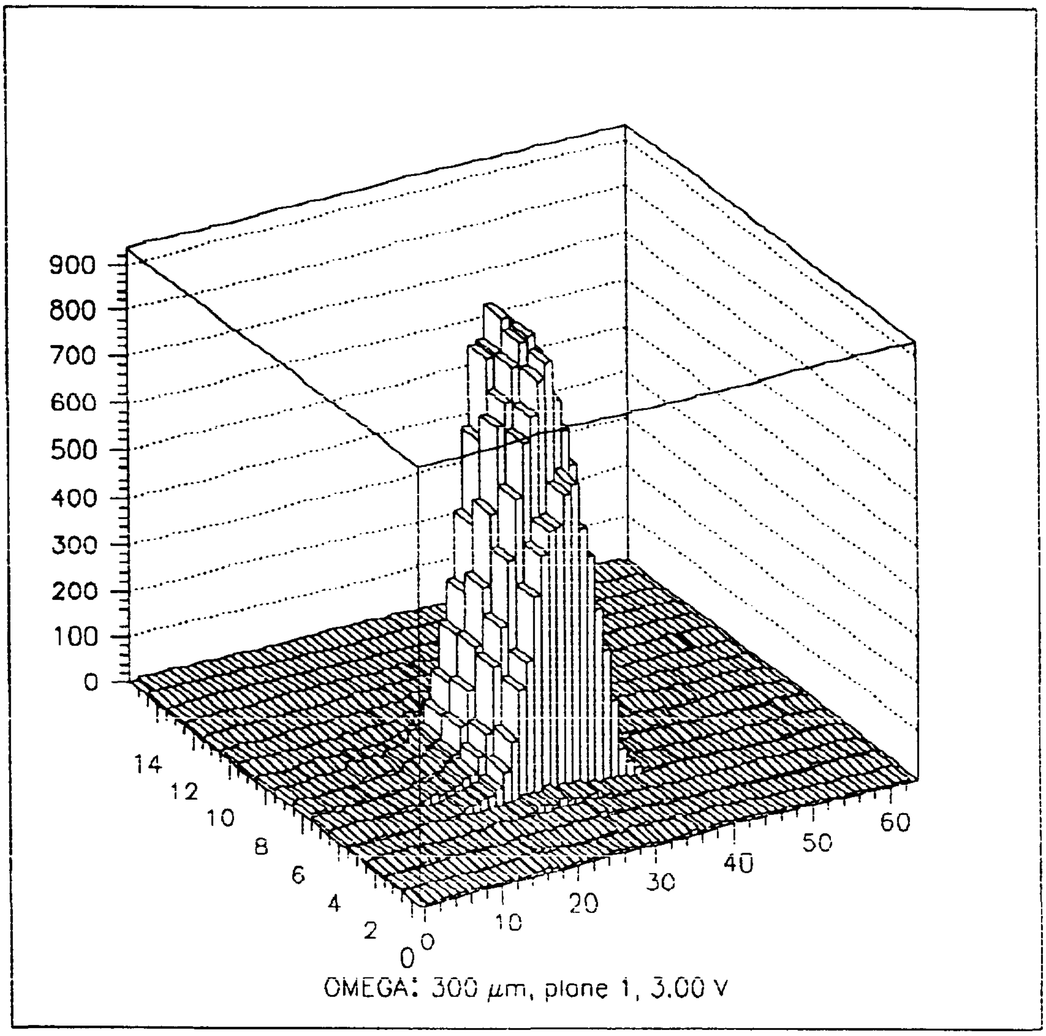


Fig. 20 Histogram of the beam spot consisting of the coordinates of hits as recorded by a micropattern detector assembly.

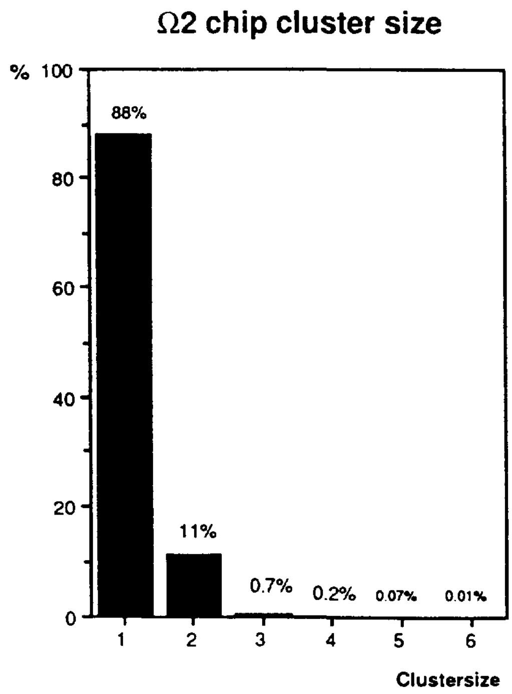


Fig. 21 Histogram of the cluster size for single beam tracks.

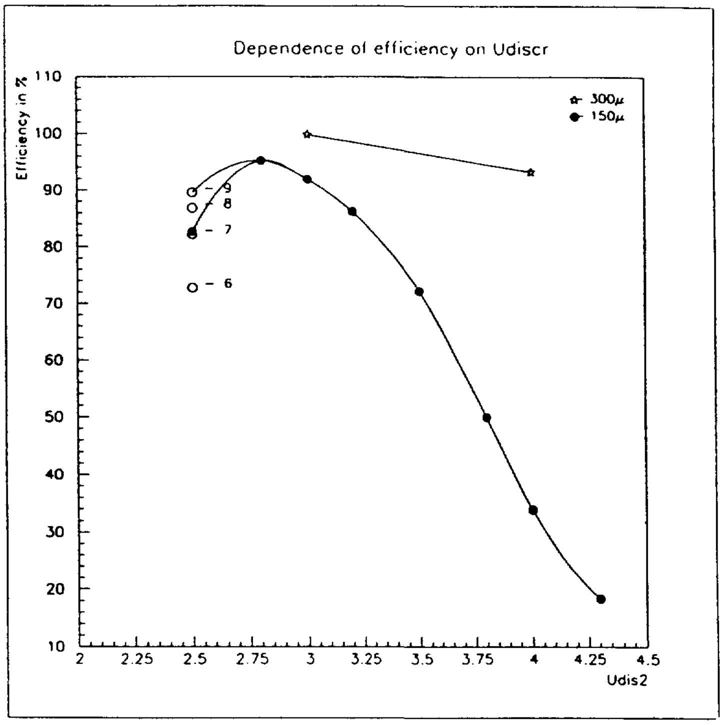


Fig. 22 Comparison of detector efficiency for a 150 μm and a 300 μm thick detector as a function of the discriminator threshold.

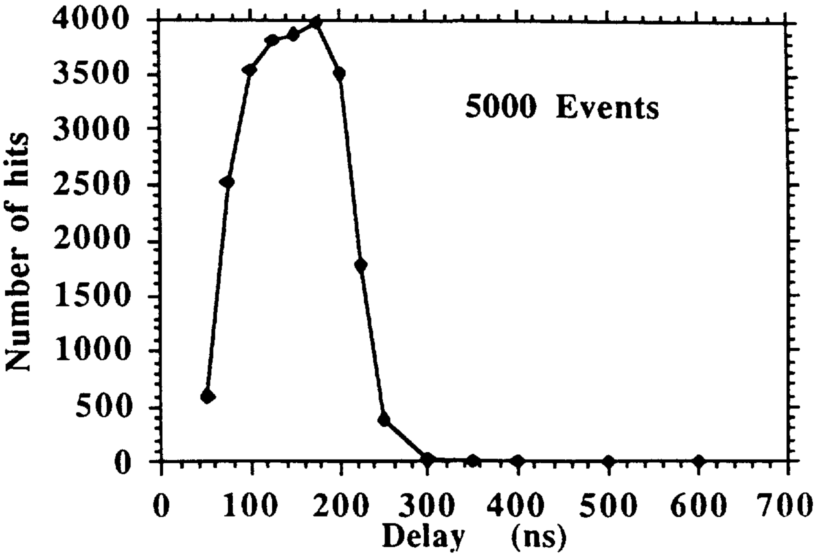


Fig. 23 Scan of the delay time after which the 200 ns strobe signal is issued. Each point represents 5000 event triggers, generated by an electron traversing the detector. External settings for low threshold: Udis1=1.5 V, Udis2=1.6 V, Uqa=1.5 V, Udn=1.1 V, Vbias=50 V.

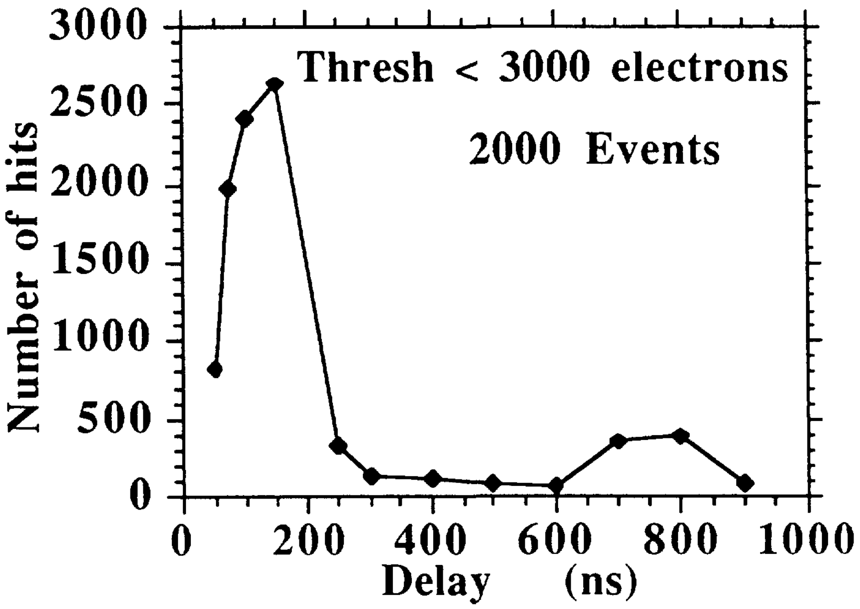


Fig. 24 Idem as fig. 23 but with a very low threshold of ~3000 electrons: Udis2=1.4 V.

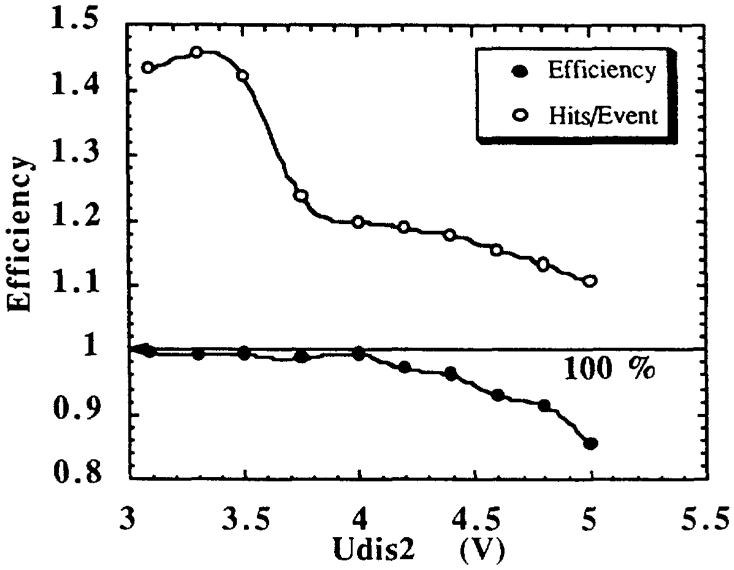


Fig. 25 Efficiency and number of hits per event for a 6-ladder array as a function of external threshold voltage Udis2. Each point represents 2000 triggers, strobe duration was 500 ns and strobe delay 50 ns. Udis1=3.57 V. Udn=2.4 V.

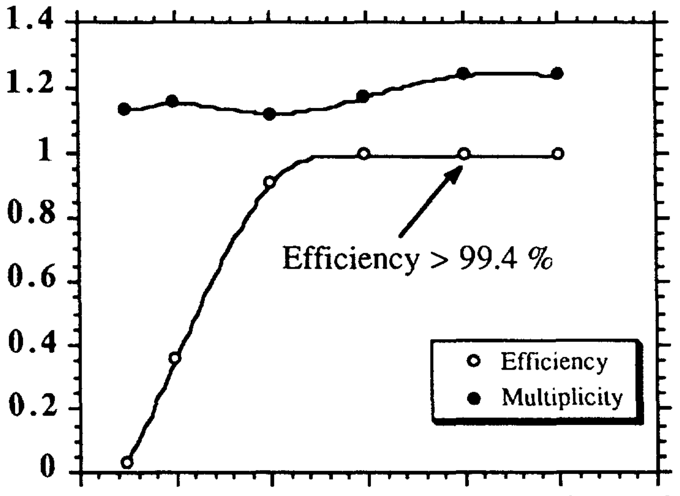


Fig. 26 Efficiency and number of hits per event for a 6-ladder array as a function of detector bias voltage Vbias. Udis1=Udis2=1.5 V, Udn=1.1 V, strobe duration 200 ns, strobe delay 150 ns.

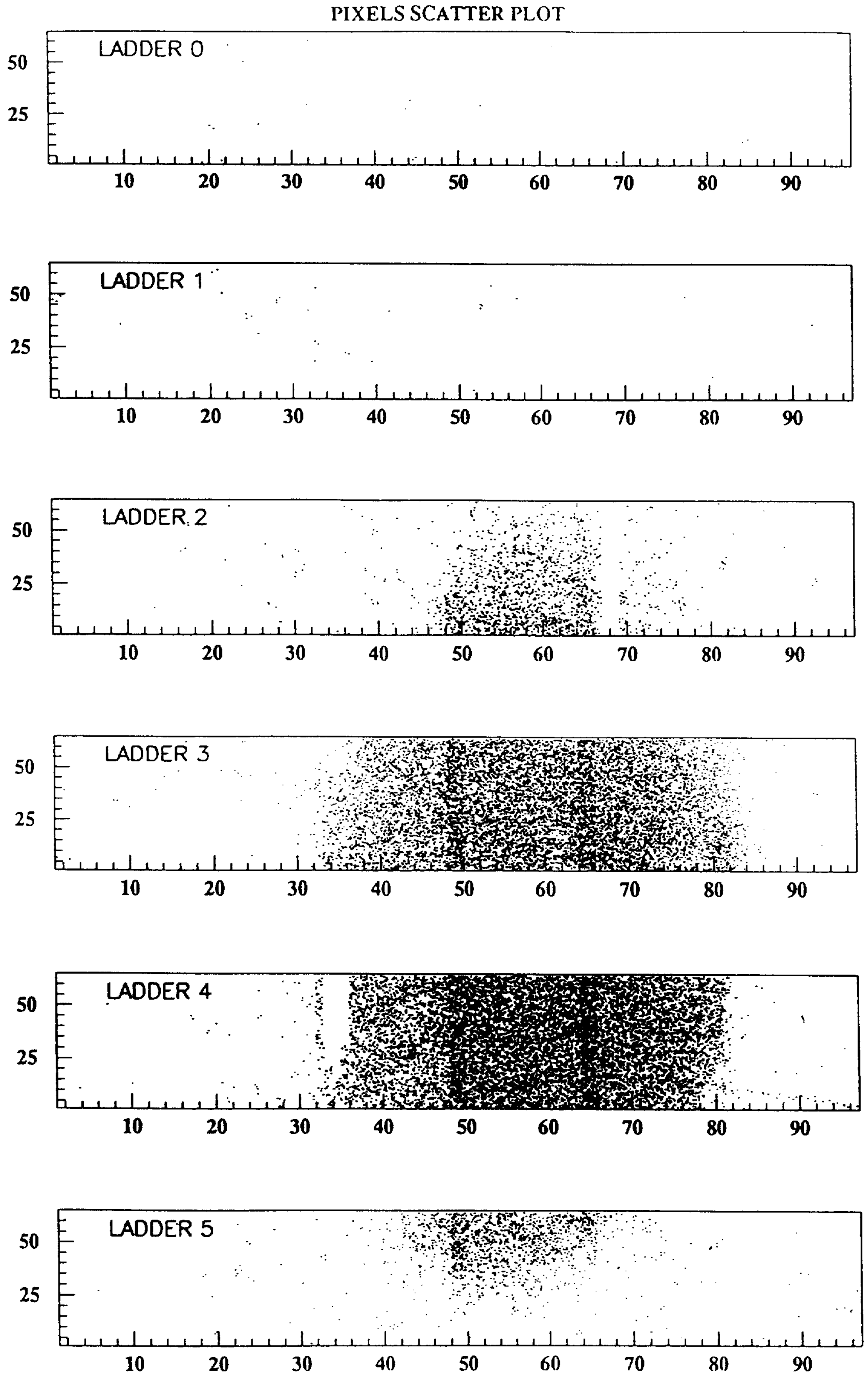


Fig. 27 On-line scatter plot of the hits from 50000 events in the 6-ladder array. The dark bands are explained in the text.

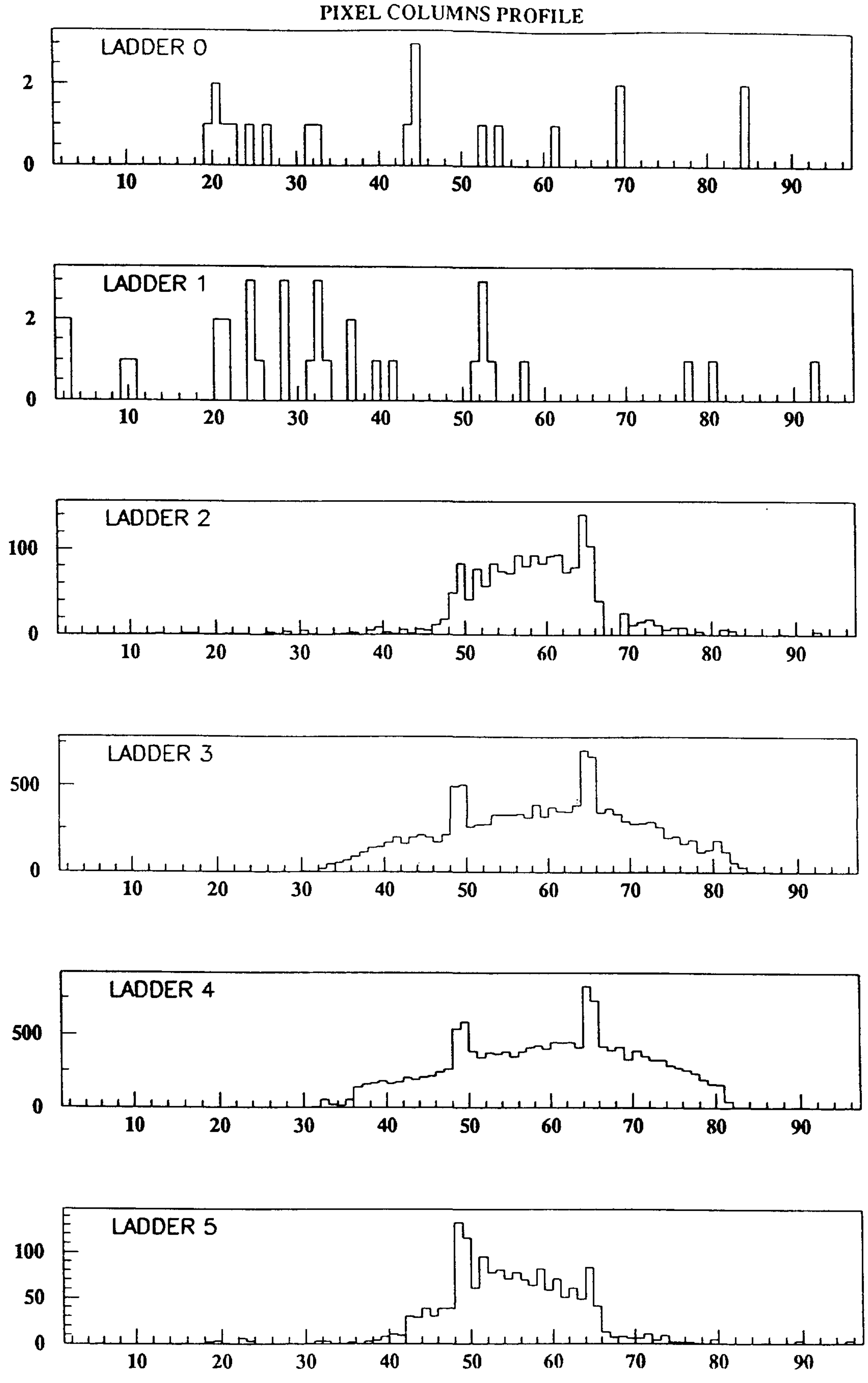
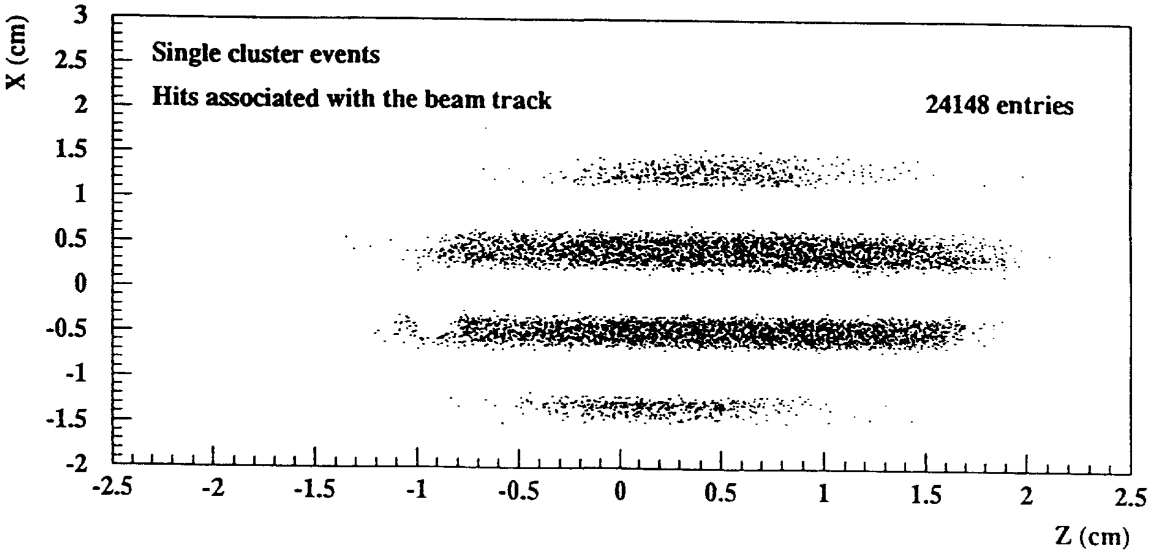


Fig. 28 Projection of the hits in each ladder in fig. 27 in the direction of the columns. Note the change of the vertical scales from ladder to ladder.



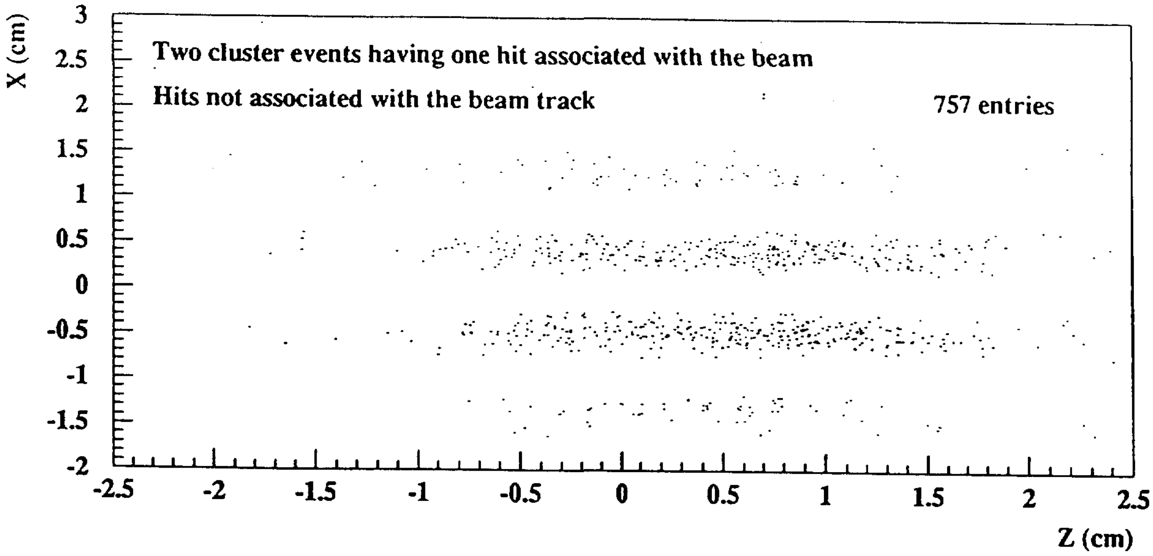


Fig. 29 Top: Off-line representation of selected data from fig. 27, geometrically corrected. Only hits from single cluster events are plotted.

Bottom: Idem for 2-cluster events with only those hits that are **not** associated with the wirechamber-determined beam track. These hits are nevertheless correlated with the beam position and can be explained by the longer strobe time of the pixel array.

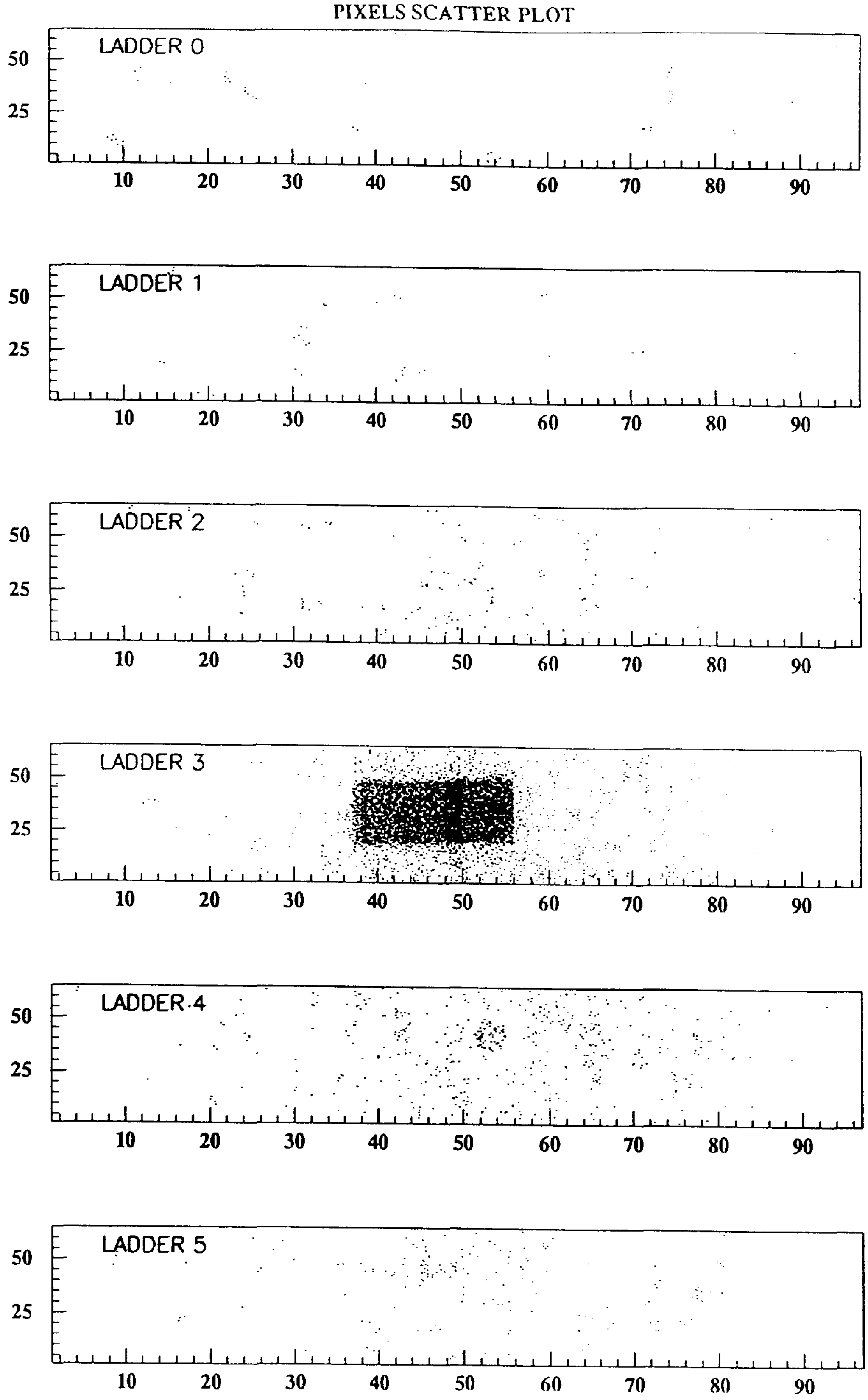


Fig. 30 On-line scatter plot of the hits with the scintillating fiber in the event trigger.

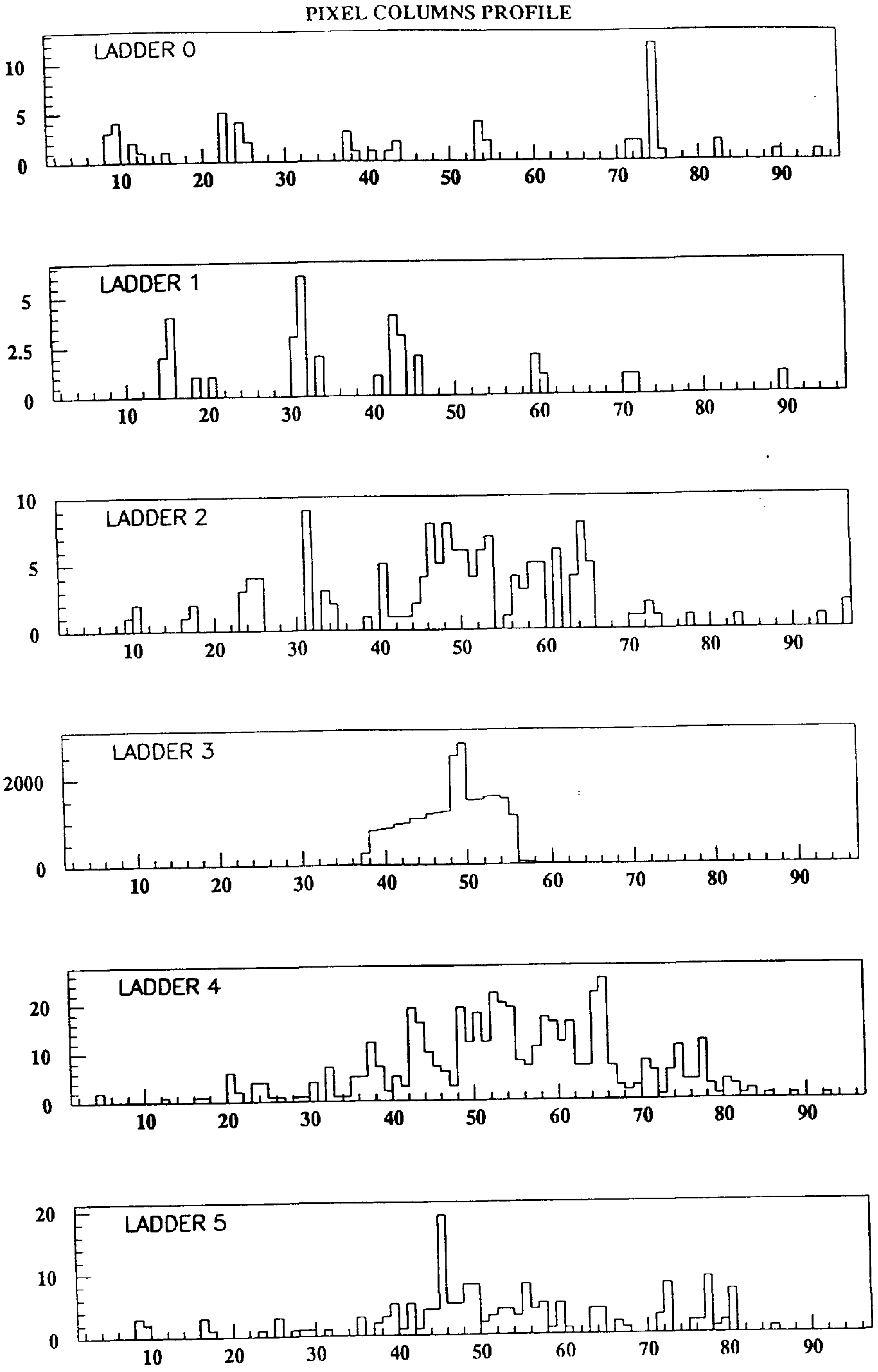


Fig. 30 Projection of the hits of fig. 30 in the direction of the columns.

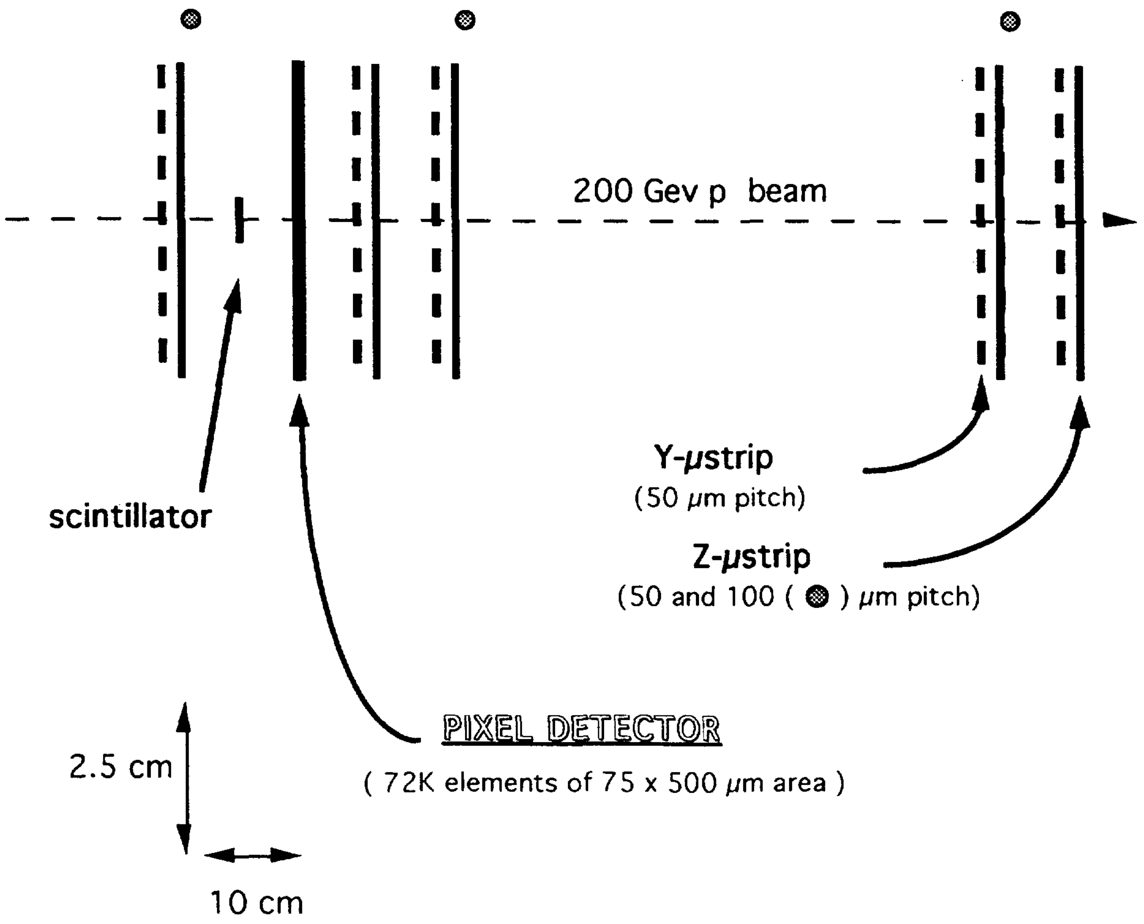


Fig. 31 The layout of the pixel detector and microstrip vertex detectors in the Omega WA97 run in November 1993.

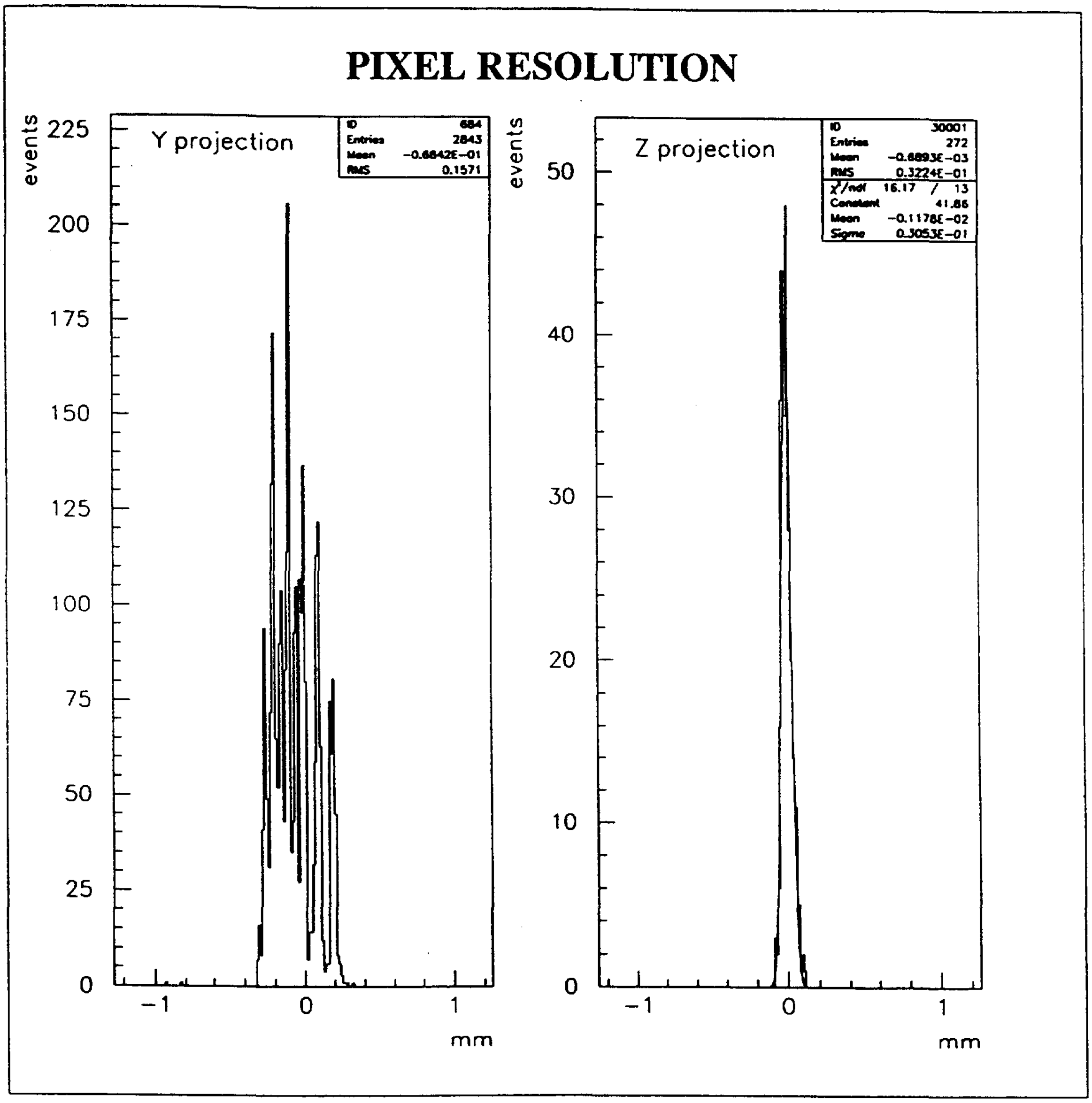


Fig. 32 Histograms of the distribution of residual values between predicted and measured coordinates in the y- and z-projection (see fig.31). Standard deviations of 157,1 μm (y) and 30.5 μm (z) are calculated which lead to a precision of the pixel detector of 150 μm and 22 μm in the y- resp. z directions.

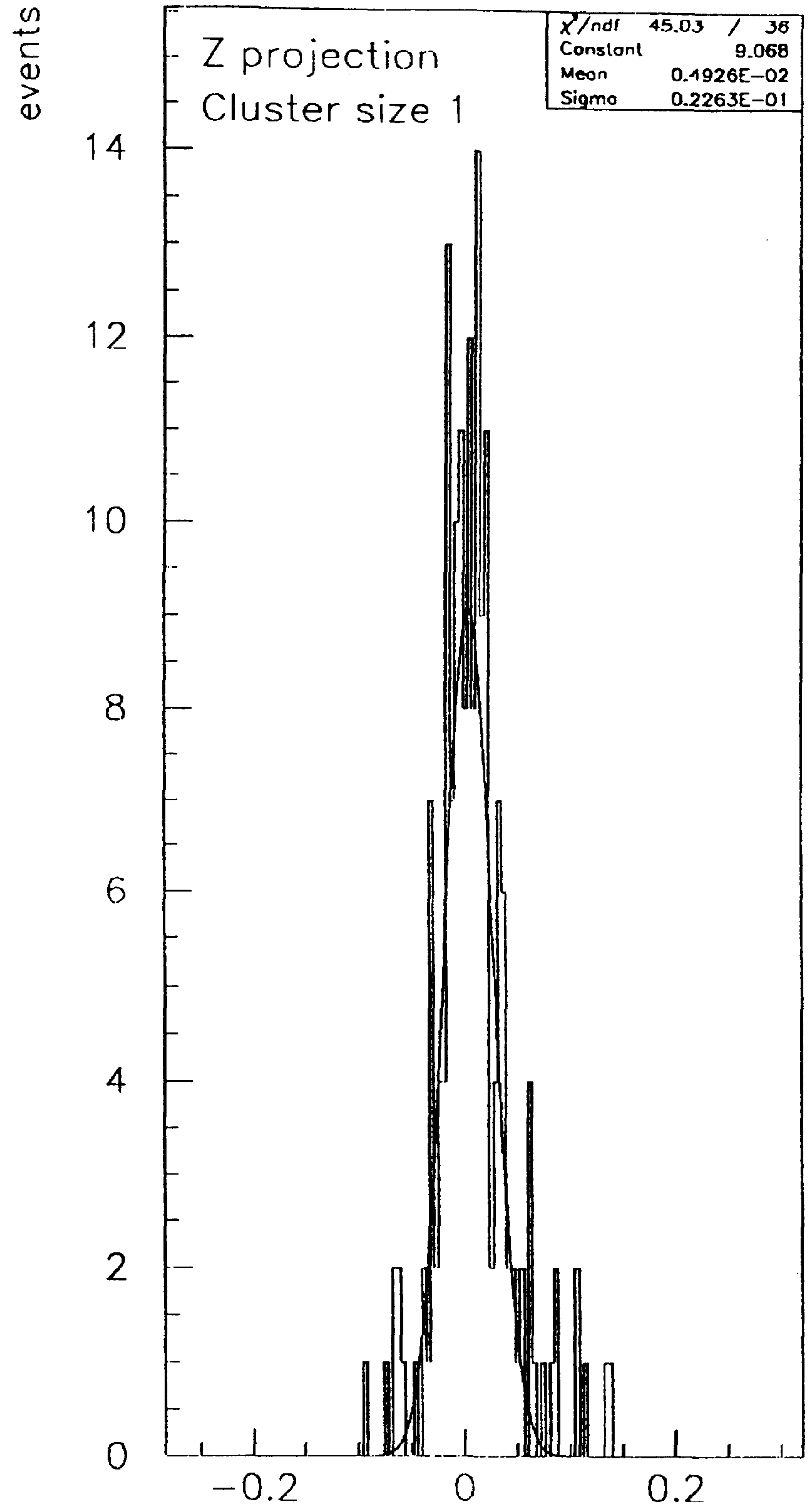


Fig. 33 Distribution as in fig. 32 but for selected events with 2 adjacent row cells hit in the pixel detector. The standard deviation is now only 22.6 µm giving a precision better than 10 µm in the pixel detector.

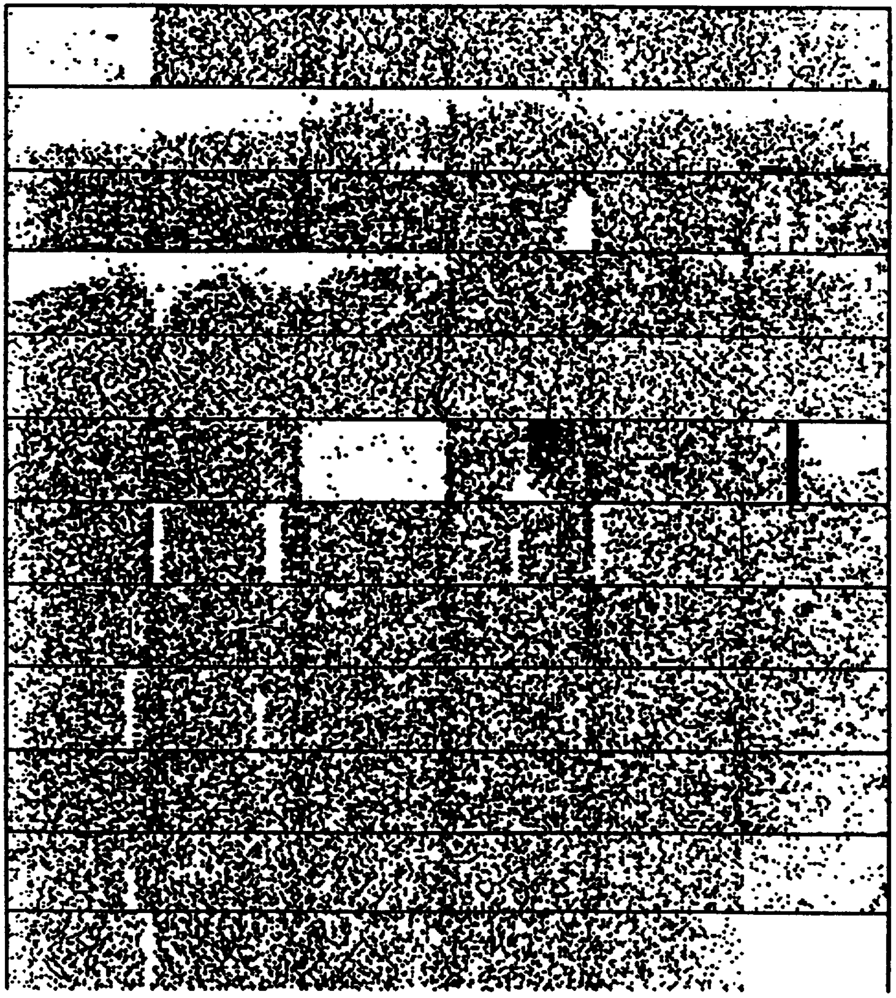


Fig. 34 Scatter plot for a complete, double array with 72 readout chips. The separations between the chips are visible as vertical, dark bands.