Analysis of MOS capacitor with p layer with TCAD simulation

Y. Unno[c,*], E. Bach[b], J. Dandoy[a], V. Fadeyev[d], C. Fleta[b], C. Jessiman[a], J. Keller[a], C.T. Klein[a], T. Koffas[a], E. Staats[a], M. Ullan[b]

[a] *Physics Department, Carleton University, 1125 Colonel By Drive, Ottawa, Ontario, K1S 5B6, Canada*
[b] *Instituto de Microelectrónica de Barcelona (IMB-CNM), CSIC, Campus UAB-Bellaterra, 08193 Barcelona, Spain*
[c] *Institute of Particle and Nuclear Study, High Energy Accelerator Research Organization (KEK), 1-1 Oho, Tsukuba, Ibaraki 305-0801, Japan*
[d] *Santa Cruz Institute for Particle Physics (SCIPP), University of California, Santa Cruz, CA 95064, USA*

Abstract

The ATLAS18 strip sensors of the ATLAS inner tracker upgrade (ITk) are in production since 2021. Along with the large-format n^+-in-p strip sensor in the center of 6-inch wafer, test structures are laid out in the open space for monitoring the performance of the strip sensor and its fabrication process. One of the structures is a 1.2×1.0 cm^2 test chip that includes representative structures of the strips, and Metal-Oxide-Silicon (MOS) capacitors. In addition to the standard MOS capacitor, a MOS capacitor is designed with a p-implantation in the surface of silicon, representative of the p-stop doping for isolating the n^+ strips, the MOS-p capacitor. The capacitance measurement of the standard MOS capacitor as a function of bias voltage (C-V) shows characteristic behavior in the accumulation, depletion, and inversion regimes, from which one can deduce the amount of the interface charge. The MOS-p capacitor shows the C-V behavior modulated by the properties of the p-layer. With over 50% of the full production complement delivered, we have observed consistent characteristics in the MOS-p capacitors. Rarely and currently only in three batches, we have observed abnormalities which have implied lower density of p-implantation in the p-layer. To study the cause, we have simulated the MOS-p capacitor with a TCAD software, which successfully reproduces the normal behavior, with the p-density and the interface charge within the expected ranges, including a feature caused by a geometrical offset of the areas of the metal and the p-implantation. By contrast, overall shapes of the abnormal cases are only reproduced when introducing 1/10 of p-density, larger interface charge, charge traps in the p-layer, and/or n-type surface contamination. A smaller but distinctive feature in the C-V behavior might also be caused by non-uniform distribution of these or other components. These simulations help to take final acceptance decisions for the batches in production.

Keywords: n-in-p, p-type, strip, silicon, radiation tolerant, HL-LHC, TCAD, simulation
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1. Introduction

We are producing 20800 strip sensors for the upgraded ATLAS inner tracker (ITk), in 8 different shapes (2 in the barrel and 6 in the endcap sections) [1]. The strip sensors are made of n^+ readout strips in p-type silicon bulk, with p-stop isolation structure between the n^+ strips, so-called n^+-in-p sensors. In the wafer layout (Fig. 1), we have implemented two Metal-Oxide-Silicon (MOS) capacitors in the Quality Assurance (QA) chips (Fig. 2)[2]: (1) a standard MOS capacitor and (2) a special MOS capacitor, MOS-p, with a p-layer in the surface of the silicon bulk with density that of the p-stop isolation (Fig. 3), to evaluate the interface charge and the density of the p-stop implantation.

As of November 2023, we have received over 50% of the sensors, in 300 or more batches. Among the batches, we have observed abnormal behaviors in the MOS-p capacitors in 3 batches: VPA37921, 42646, and 46225 [3]. Such abnormal behaviors are shown together with normal behaviors of VPA37914 and other batches, as an example (Fig. 4). To understand the origin of the abnormalities, we have tried to reproduce them with a technology CAD program (TCAD).

2. TCAD setup

We have used a TCAD 3D device simulator, HyDeLEOS VER. 8.5k [4]. The MOS structure is implemented in 2D geometry (Fig. 3) with the representative parameters as listed in Table 1. We have varied mainly the interface charge with a surface density of Q_{if} (shown with "x" in Fig. 3) and the density of p-layer with a surface density of D_s. We set the insulator thickness to a typical value obtained with the C-V measurement of the MOS capacitor.

Table 1: Representtive parameters of the MOS-p capacitor in TCAD simulations

Parameter	Value
Capacitor area	746×746 μm^2
Insulator (Oxide) thickness	0.5 μm
Silicon bulk thickness	320 μm
Silicon bulk characteristics	p-type 3 kΩcm
Silicon bulk Impurity concentration	Boron 4.7×10^{12} cm^{-3}
p-layer thickness	3 μm
Edge smearing of p-layer	sigma of 0.5 μm

*Corresponding author. e-mail: yoshinobu.unno@kek.jp

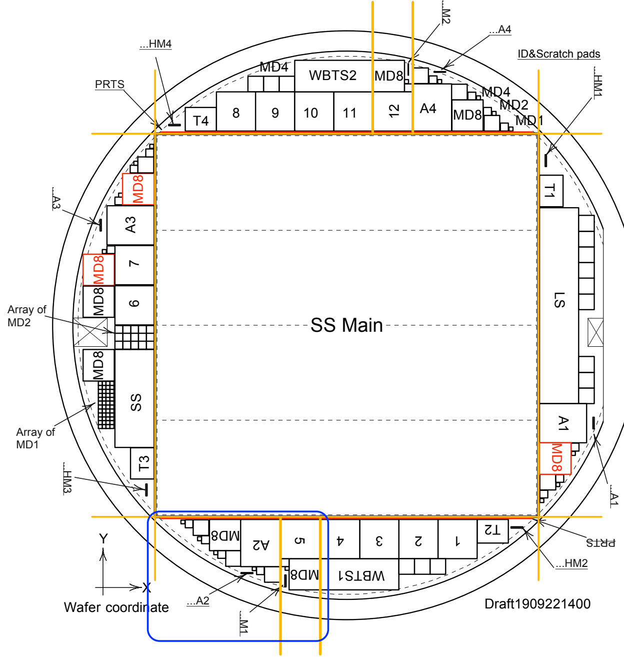

Fig. 1: Wafer layout of barrel sensor, Short-strip type (SS) [1]. QA chips are groups of test structures (encircled in blue), diced out in orange lines into Testchip&MD8 and Mini&MD8, one set per wafer.

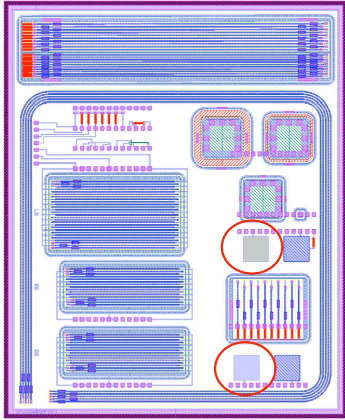

Fig. 2: ATLAS test chip [2] (labeled as A1 to A4 in the wafer layout). Two MOS capacitors are encircled in red.

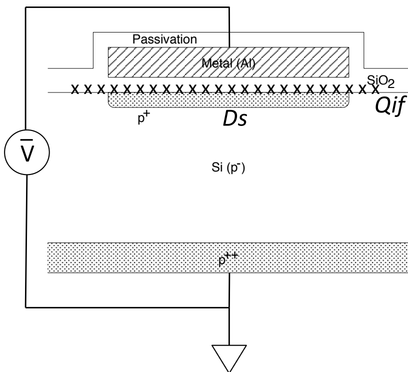

Fig. 3: MOS-p capacitor, implemented in 2D in TCAD. Q_{if} is the interface charge in the interface of oxide and silicon bulk. D_s is the density of p-implantation.

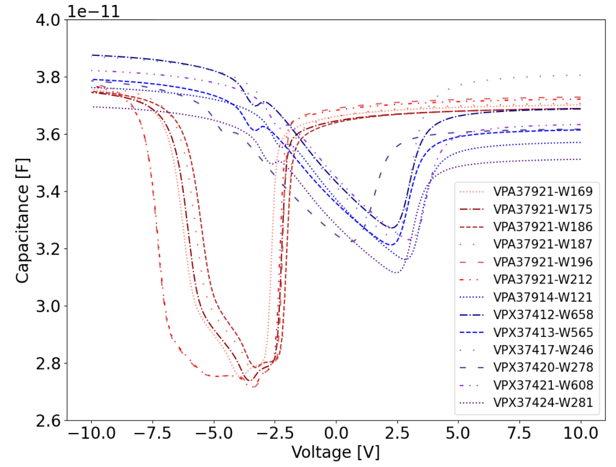

Fig. 4: C-V measurements of normal (VPA37914 and else) and abnormal (VPA37921) MOS-p capacitors, at a frequency of 10 kHz.

3. Standard MOS capacitor

With the standard MOS capacitor, we can extract the surface density of the interface charge (Q_{if}) through the measurement of the capacitance of the MOS capacitor as a function of DC bias voltage (C-V measurement), between the metal and the backplane. A typical C-V measurement is shown in Fig. 5 [5]. The characteristic behavior of the capacitance is governed by two thresholds: one is the "flatband voltage (V_{FB})" where the interface charge, which is positive, at the Si-SiO_2 boundary is cancelled out by a negative bias voltage; the other is the threshold (V_T) where the inversion layer is created at the silicon surface. The voltage range below V_{FB} is called the "accumulation" regime where majority carriers are accumulated at the silicon surface; the capacitance stays intrinsic to the MOS insulator. The range between V_{FB} and V_T is called the "depletion" regime where the bias voltage starts to deplete the silicon bulk; two capacitances, the intrinsic and the depletion region in the silicon bulk, are in series, thus the total capacitance becomes smaller. The range above V_T is called the "inversion" regime where the minority carriers are accumulated at the silicon surface; the capacitance varies according to the AC frequency of the capacitance measurement depending on how fast the inversion layer responds to the AC voltage. From V_{FB}, we can calculate the surface density of the interface charge, Q_{if} [2].

We have a typical C-V measurement of the standard MOS capacitors, measured at a frequency of 1 kHz (Fig. 6) [2], from which we estimate Q_{if} being approximately 8×10^{10} ions/cm^2. We have simulated the C-V measurement with Q_{if} of 1×10^{10}, 5×10^{10}, 1×10^{11}, 2×10^{11} ions/cm^2 (Fig. 7)[1]. The simulation with 5×10^{10} ions/cm^2 is consistent with the measurement. The TCAD software simulates the device at thermal equilibrium, equivalent to the low frequency capacitance.

[1]The vertical axis of TCAD simulations are in arbitrary scale.

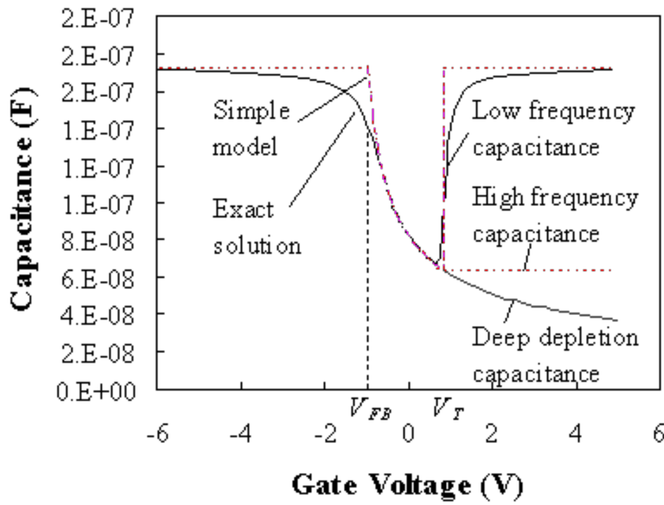

Fig. 5: Typical behavior of the capacitance as a function of bias voltage. B. Van Zeghbroeck, 2011 [5]

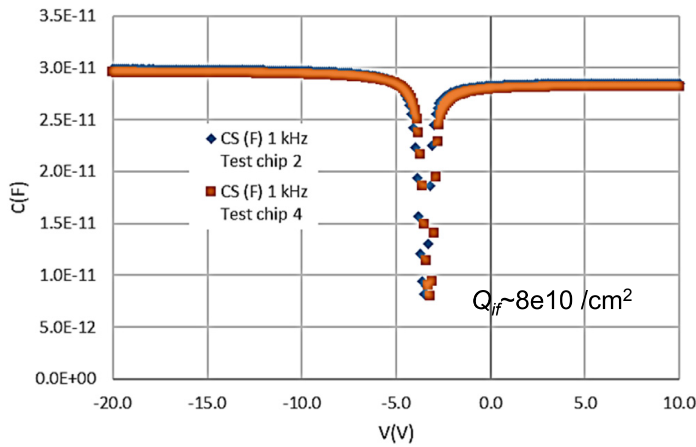

Fig. 6: Typical C-V measurement of the standard MOS capacitors [2]

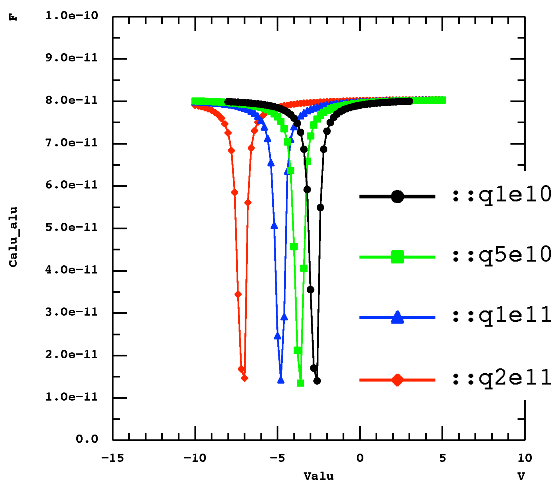

Fig. 7: TCAD simulations of C-V measurement of the MOS capacitor with Q_{if} of 1×10^{10}, 5×10^{10}, 1×10^{11}, 2×10^{11} ions/cm^2.

4. MOS capacitor with p-layer (I) : p-density and interface charge

We have specified the surface density, D_s, of the p-stop structure to be approximately 4×10^{12} ions/cm^2 [1]. Under the condition of an interface charge, Q_{if}, of 1×10^{11} ions/cm^2, we have simulated the C-V measurements with the p-layer densities, D_s, of 2×10^{12}, 4×10^{11}, 2×10^{11} ions/cm^2 (Fig. 8). The triangular shape of the dip with D_s of 2×10^{12} is consistent with that of the normal batch of VPA37914 (in Fig. 4). A lower density of D_s moves the location of the dip along the bias voltage towards more negative voltages, however, an order of magnitude lower density D_s of 2×10^{11} ions/cm^2 is not enough to be consistent with the abnormal one. Lowering the density further did not help; the location of the dip tends to saturate. An increase of the interface charge Q_{if} to 3×10^{11} ions/cm^2 moves the location further in lower voltage to be consistent with the abnormal ones. With the values of the p-density and the interface charge, although the location of the dip can be reproduced, the shapes of the dips are triangular and too sharp.

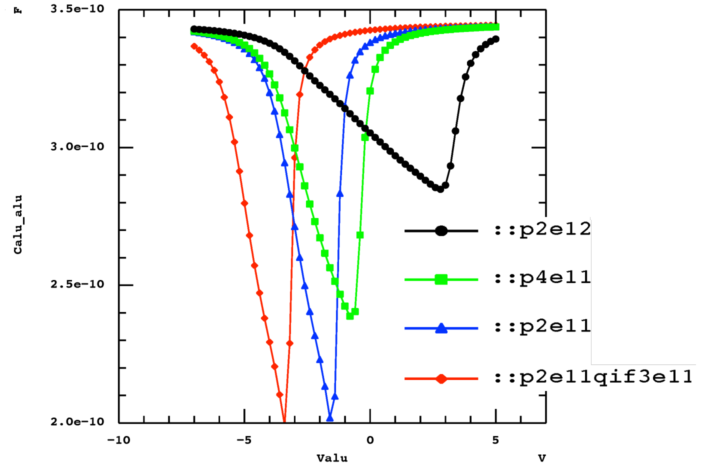

Fig. 8: TCAD simulations of C-V measurements with D_s of 2×10^{12}, 4×10^{11}, 2×10^{11} ions/cm^2, under Q_{if} of 1×10^{11} ions/cm^2. An extra curve is shown for D_s of 2×10^{11} ions/cm^2 under Q_{if} of 3×10^{11} ions/cm^2.

5. MOS capacitor with p-layer (II) : Charge traps in p-layer

The p-implantation creates charge traps in the p-layer as a remnant of radiation damage, which are to be "annealed away" with temperature treatment in the fabrication process. The traps can be negatively (p-type) or positively (n-type) charged-up after absorbing electrons or holes or releasing holes or electrons. We have simulated the C-V measurement by introducing charge traps in the p-layer (Fig. 9). Only positive traps (n-type) have affected the C-V behavior.

In this case, the dips are flattened in the abnormal behavior (of the plot with D_s of 6×10^{11}, highlighted with a red circle). Even in the normal one, the charge traps introduce a kink (with D_s of 6×10^{12}, highlighted with a red circle). We have observed such a kink in the VPA37914 (in Fig. 4). We set the density of

the traps not to deviate too much in the normal one. Despite tuning the density of the traps, the relative locations of the dips of normal and abnormal stay the same.

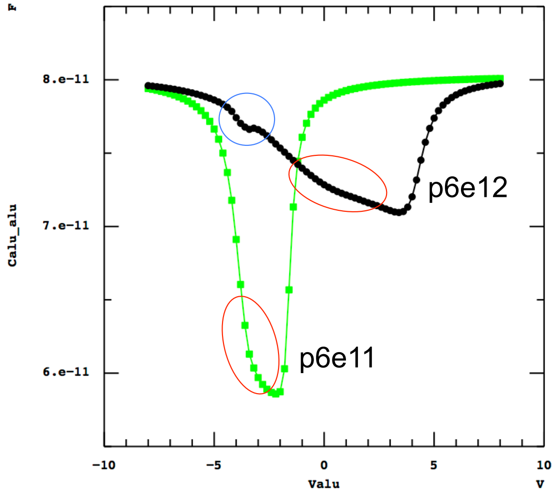

Fig. 9: TCAD simulations of C-V measurement with D_s of $6{\times}10^{12}$ and $6{\times}10^{11}$ ions/cm^2, under Q_{if} of 1×10^{11} ions/cm^2 and n-type charge traps in the p-layer region. An introduction of the "setback" of p-layer to the metal area is also included (highlighted with a blue circle).

6. MOS capacitor with p-layer (III) : Setback of p-layer to metal

We have observed a tiny dip at around -3 V in the C-V measurement of the MOS-p capacitors (Fig. 4). With the TCAD simulations, this dip (Fig. 9, highlighted with a blue circle) is identified to be caused by the existence of "setback" of the area of the p-layer to the area of the metal.

We have reproduced two factors from the simulations: the location along the bias voltage and the depth, of the dip. The former is caused by the p-density of the area of the "setback" and the latter by the size of the area. We set the p-density to that of the silicon bulk. The "setback" is 4.5 μm in the perimeter of the capacitor, which results in the ratio of the area of the p-layer to that of the metal being 0.976. A bit smaller ratio of 0.970, which corresponds to a setback of 5.5 μm, has reproduced the depth of the dip better.

7. MOS capacitor with p-layer (IV) : Surface contamination

The introduction of charge traps in the p-layer is not enough to reproduce the "width" and the "flatness of the bottom" of the dip in the abnormal behaviors. For this case, we have introduced a surface contamination with n-type impurity, with the surface densities of null, 6×10^{10}, 8×10^{10}, and 1×10^{11} ions/cm^2 (Fig. 10). The location of the dips has moved. The bottom of the dips seems to be flatter, but the widths remain similar. We also observe that the introduction of n-type surface contamination induces similar effects as the interface charge, shifting the location of the dip, as expected.

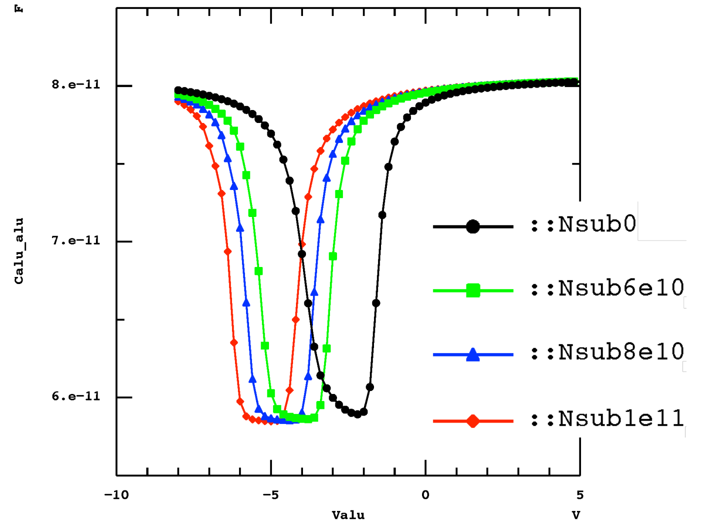

Fig. 10: TCAD simulations of C-V measurement with n-type surface contamination of null, 6×10^{10}, 8×10^{10}, and 1×10^{11} ions/cm^2, under D_s of 6×10^{11} ions/cm^2 and n-type charge traps in the p-layer.

8. Discussion

With TCAD simulations, we have understood that the location along the bias voltage and the shape of the dip in the C-V measurement of the MOS-p capacitor are affected by the p-density, amount of the interface charge, possible charge traps in the p-layer, and n-type surface contamination. There could be other factors that we have not considered.

One of the abnormal cases with a rather wide width of the dip, however, still requires further investigation. We have applied these factors uniformly over the relevant areas in the previous sections. There could be local non-uniformity in these factors which might modify the shape further. We have already tried such possibilities but have not yet identified a cause for the anomalous width of the dip.

The results that we have already obtained imply qualitatively that there could have been issues in the fabrication process such as p-implantation, etching, insulator deposition, heat treatment, and even very local non-uniformity. We are in communication with the vendor to improve the fabrication quality.

9. Conclusion

We have understood the C-V behaviors of the MOS capacitors, with and without p-layer at the silicon surface (MOS and MOS-p capacitors, respectively) with TCAD simulations. The rare but abnormal C-V behavior of the MOS-p capacitor in the production batches has been understood to be caused by a low p-density of the p-layer (1/10 or less of the specification) and potentially other factors such as larger interface charge, issues in heat treatment, and others. The results have helped increase confidence in the decisions for accepting or rejecting abnormal batches. Also, the findings are communicated to the vendor to improve the process quality.

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References

[1] Y. Unno et al, *Specifications and pre-production of n^+-in-p large-format strip sensors fabricated in 6-inch silicon wafers, ATLAS18, for the Inner Tracker of the ATLAS Detector for High-Luminosity Large Hadron Collider*, 2023 JINST 18 T03008

[2] M. Ullan et al., *Quality Assurance methodology for the ATLAS Inner Tracker strip sensor production*, Nuclear Instruments and Methods in Physics Research A, 981 (2020) 164521, https://doi.org/10.1016/j.nima.2020.164521

[3] E. Bach-Marques et al, *Analysis of the quality assurance results from the initial part of production of the ATLAS18 ITk strip sensors*; P. Miyagawa et al, *Analysis of the results from Quality Control tests performed on ATLAS18 Strip Sensors during on-going production*, in Nuclear Instruments and Methods in Physics Research A, SI:HSTD13 special issues

[4] Keio University, TCAD R&D Center (TRDEC), *HyDeLEOS Ver. 8.5k User's manual*, 2019

[5] B. Van Zeghbroeck, *Principles of Semiconductor Devices*, Figure 6.3.4, https://truenano.com/PSD20/chapter6/ch6_3.htm#6_3_4_3