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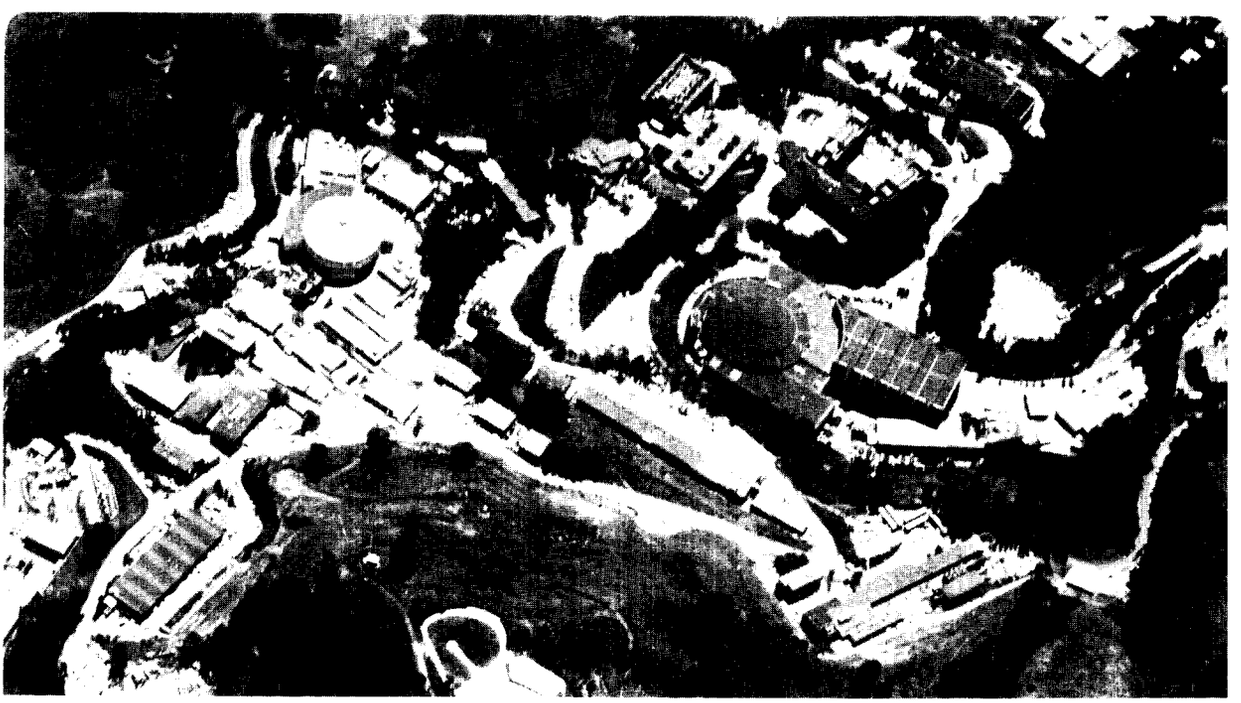

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Wan-Shick Hong, John S. Drewery, Tao Jing, Hyong-Koo Lee,
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Physics Division
Lawrence Berkeley Laboratory
University of California
Berkeley, CA 94720

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Physics Division, Lawrence Berkeley Laboratory,
Berkeley, CA 94720, U.S.A.

Abstract

Thick (~50 μm) amorphous silicon (a-Si:H) p-i-n diodes of device quality are made by helium dilution of the process gas and heat treatment for application to minimum ionizing particle detection. Dilution of SiH_4 with He decreased the dangling bond density and increased the deposition rate. The internal stress, which causes substrate bending and delamination, was reduced by a factor of 4 to ~90 MPa when deposited at low (150°C) temperature. The electronic quality of the a-Si:H film was somewhat degraded when grown at a low temperature, but could be mostly recovered by subsequent annealing at 160°C. By this technique 50 μm-thick n-i-p diodes were made without significant substrate bending, and the electronic properties, such as electron mobility and ionized dangling bond density, were suitable for detecting minimum ionizing particles. Diode readouts and integrated amplifiers for pixel arrays are also described.

I. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) p-i-n diodes are good candidates for radiation detectors for applications in high energy physics experiments, medical imaging, materials and life sciences.[1, 2, 3, 4] Advantages of the amorphous silicon layer are: (a) The disordered Si network makes the material less sensitive to radiation induced damaged which can be annealed subsequently at low temperature. (b) Unlike crystalline silicon, the area of the a-Si:H film is not limited by the wafer diameter, and the deposition requires less energy and fewer purification steps which save cost. A further advantage is that the readout electronics, thin film transistors, or diodes can be deposited on the a-Si:H layers. Additionally, at a cost of further processing, polysilicon layers can be made by laser heating allowing for the possibility of making low noise charge sensitive amplifier readout for pixel or strip detectors.[5]

A schematic diagram of an a-Si:H radiation detector is shown in Fig. 1. Incident radiation interacts with the intrinsic layer which is fully depleted under appropriate reverse bias, and produces electron hole pairs. The collected electron and holes, arising from the interaction of the

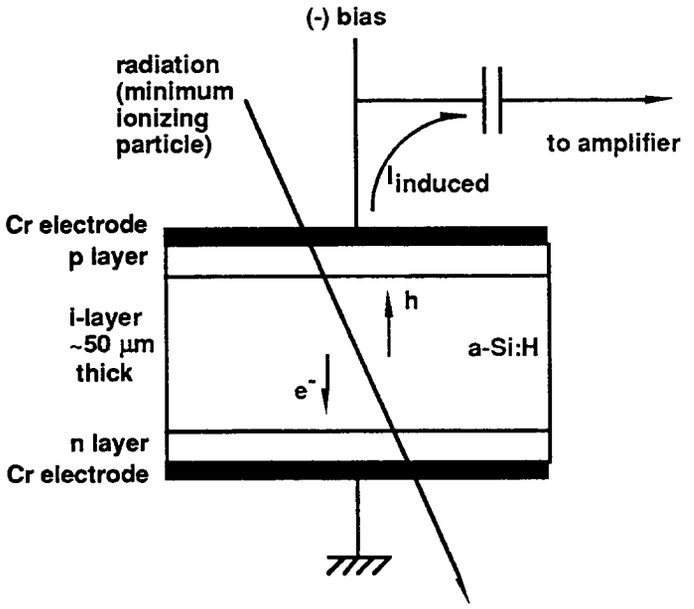

Figure 1 Schematic diagram of a-Si:H detectors for minimum ionizing particles

incident radiation in this region, generate a signal which is picked up by a charge sensitive pre-amplifier.

For charged particles, especially minimum ionizing particles (MIPs), p-i-n diodes with thick (> 50 μm) i layers are required to produce sufficient number of e-h pairs in the intrinsic layer. Usually, the i layer has a density of dangling bonds which are ionized by releasing non-bonding electrons under a sufficient electric field and are positively charged. These space charges cause the electric field in the i layer to drop linearly with distance. Therefore, ionized dangling bond density, N_D^*, is a major quantity of interest in the fabrication of good detectors. It has been shown empirically that N_D^* is approximately one-third of the total dangling bond density N_D.[6] Device quality a-Si:H films are made mostly by plasma-enhanced chemical vapor deposition (PECVD) technique and have N_D^* of 5~10 x 10^{14} cm^{-3}.[7]

Table I. Material properties of a-Si:H and c-Si

Properties	c-Si	a-Si:H
density (g/cm^3)	2.3	~2.25
electron mobility ($cm^2/Vsec$)	1350	1~4 (*)
hole mobility	480	0.004~0.007
W (eV)	3.6	4.8 ± 0.3
radiation hardness (maximum fluence of 1 MeV neutron, cm^{-2})	10^{13}	4 x 10^{14}
($\mu\tau$), electron		1.2 x 10^{-7}
($\mu\tau$), hole		2.6 x 10^{-8}
band gap energy (eV)	1.1	1.7~1.9

(*) The higher values of electron and hole mobilities can be made by hydrogen dilution of silane in the i-layer [9]

For a good detection efficiency, the mean free path of the radiation-generated carriers must be sufficiently long, and W, the average energy required to produce one electron-hole pair, be adequately small. The mobility-lifetime product, $\mu\tau$, is a useful parameter as it determines the mean drift length, $d = \mu\tau E$, of carriers where E is the electric field of the external bias. Also, a low density of dangling bonds ($< 2 \times 10^{15}$ cm^{-3}) is required for a large value of $\mu\tau$, since $\mu\tau N_D = 2.5 \times 10^8$ in i layers made using pure silane gas.[8] In Table I, material properties of a-Si:H are compared with those of crystalline silicon.

In this paper we describe a growth technique of thick a-Si:H layers that have good electronic quality and low internal stress for increased mechanical stability. Also, the property of the a-Si:H p-i-n diode and its applications for large area position sensitive detectors are discussed.

II. PREPARATION METHODS

In order to detect radiation particles, p-i-n diodes deposited on substrates coated with Cr or indium tin oxide (ITO) are used. In the PECVD technique, SiH_4 gas molecules are decomposed by radio frequency plasma and deposit on the substrate in an amorphous phase. The layer can also be doped by mixing PH_3 for n-type or B_2H_6 for p-type to the SiH_4 during the glow discharge deposition.[10]

Growth rate of a good quality intrinsic layer at the conventional plasma excitation frequency of 13.56 MHz is ~0.7 μm/hr., but a higher deposition rate is useful for commercial applications. Increasing the plasma frequency to 100 ~ 110 MHz has been shown to enhance the growth rate without any deterioration of the electronic properties of the deposited film.[11, 12] We have adopted this method and achieved a deposition rate of 2.3 μm/hr. at 85 MHz.

Further improvement in the growth rate can be achieved by adding inert gas to the silane. Dilution of silane with inert gas enhances ion bombardment during deposition, which facilitates the diffusion of radicals at the growing surface and etches away weakly bonded atoms.[13, 14] It has been reported that the deposition rate of the amorphous silicon film can be increased by mixing silane with helium, and the "He-diluted" n-i-p diode can be used to detect α-particles.[15] However, the reported value of N_D^* in the He-diluted i-layer was about 2 times larger than that in

Table II. Deposition Parameters for Conventional and He-diluted a-Si:H

Gas	Temp.(°C)	Power Density (mW/cm^2)	Pressure (mTorr)	Deposition Rate (μm/hr.)
100% SiH_4	250	40	300	2.3
60% SiH_4-40% He	250	90	500	3.5~4

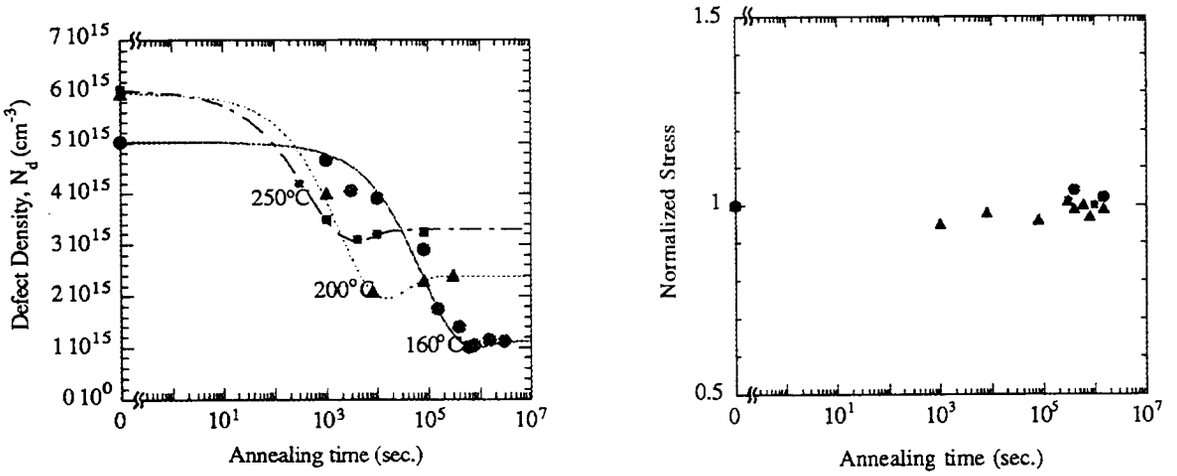

Figure 2 Time dependence of (a) defect density and (b) normalized residual stress during annealing at different temperatures. Circles, triangles, and squares represent the annealing temperatures of 160°C, 200°C, and 250°C, respectively.

the standard a-Si:H materials.[15, 16] Hence, we modified the deposition parameters and achieved both a moderate enhancement in the deposition rate and a reduction in the N_D^*. We used a 60% SiH_4 - 40% He mixture as a source gas and obtained a growth rate of 3.5 ~ 4 μm/hr. at the excitation frequency of 85 MHz. The ionized dangling bond density of 2.5 x 10^{14} cm^{-3} was obtained when the substrate temperature was held at 250°C. The deposition parameters of the He-diluted and conventional a-Si:H are summarized in Table II.

Another issue in making thick a-Si:H layers is a high built-in stress. Electronic quality films often have 300~400 MPa of compressive stress which is large enough to bend the substrate or to cause the film to peel off spontaneously. Extensive research has been done to reduce the residual stress by changing deposition parameters, but it produced a trade-off between the ionized dangling bond density and the stress.[14, 17, 18] For example, lowering the substrate temperature from 250°C to 150°C can decreases the stress from 350 MPa to 100 MPa, but at the same time the N_D^* jumps from 5 x 10^{14} cm^{-3} to 3 x 10^{15} cm^{-3}.

However, if the low temperature deposition is combined with He-dilution and heat treatment, we can make thick films at a reduced stress with good electrical properties. If we lower the growth temperature, the film stress will decrease and the N_D^* will increase.[17, 18, 19] However, for standard a-Si:H films, the increased N_D^* can be mostly recovered by annealing at a proper temperature without affecting the stress appreciably.[20] In Fig.2, relaxation of defect density and residual stress with annealing time was plotted for standard a-Si:H diodes. The

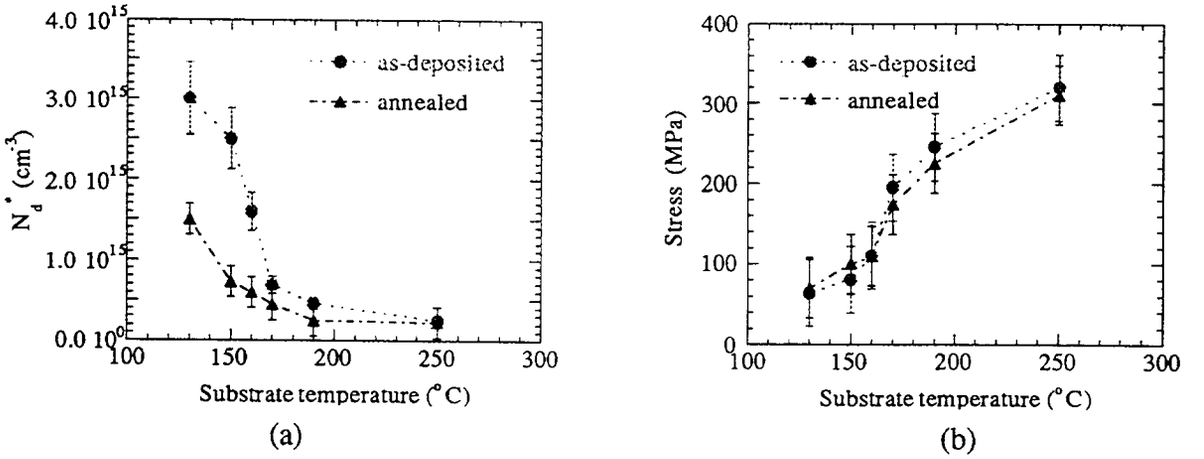

Fig. 3. Change in (a) ionized dangling bond density and (b) stress with deposition temperature of He-diluted p-i-n diodes before and after annealing

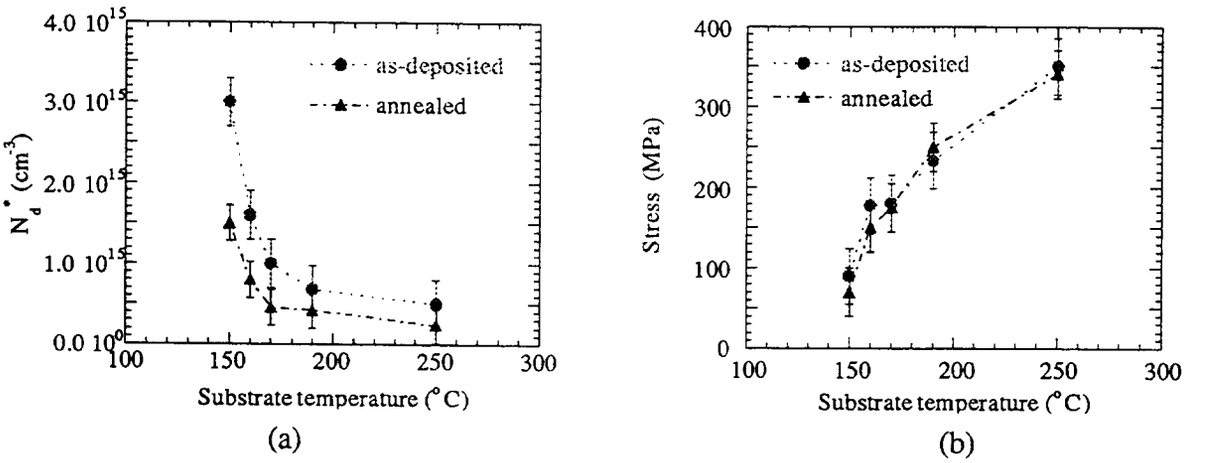

Fig. 4. Change in (a) ionized dangling bond density and (b) stress with deposition temperature of standard p-i-n diodes before and after annealing

samples were degraded by heating at 300°C for 10 minutes and quenched in water prior to annealing. The stress values are normalized to the stress of the samples quenched from 300°C. At the annealing temperature of 160°C, the dangling bond density was reduced by a factor of 5 after ~80 hours and underwent little change with further heat treatment. The stress did not change with annealing in all cases.

Based on this result, we deposited 5 to 50 μm-thick p-i-n diodes with He-dilution at temperatures between 130°C and 250°C, and annealed them at 160°C for ~100 hours. All the other deposition conditions are fixed at the values listed in table I, and only the substrate temperature was varied. In Fig.3, the changes in stress and dangling bond density of He-diluted samples, before

and after the heat treatment, are plotted according the deposition temperature. Standard samples were prepared under the same conditions but from pure silane for references, and the results are plotted in Fig. 4.

For both the He-diluted and standard samples, the N_D^* decreased and the stress increased monotonously with increasing deposition temperature. Both the N_D^* and the stress underwent a sharp transition between the substrate temperature of 150°C and 170°C. This abrupt change in both parameters can be attributed to the increased content of SiH_2 bond configuration below 170°C and agrees well with other works.[21, 22] The SiH_2 bonds in the 3-dimensional amorphous network is an evidence of the existence of microvoids which in turn imply a large number of dangling bonds at the inside wall of the voids. These microvoids provide spaces for the compressively stressed a-Si:H network to relax, but introduce additional defect states. Annealing at 160°C seemed to rearrange the interstitial hydrogen atoms so that they passivate dangling bonds. The annealing effect on the N_D^* is more pronounced in the low temperature materials than in the high temperature ones. The stress did not change with annealing in all cases. Deposition temperature of 150°C was chosen as an optimum value, because it produced films of low enough stress (~100 MPa) and N_D^* (~7×10^{14} cm^{-3}) after annealing. Films deposited at 160°C also showed good values of residual stress and N_D^* on the average, but had large sample-to-sample variation since they are in the middle of the abrupt transition. By combining He-dilution, low temperature deposition, and thermal annealing, a-Si:H layers of 50 μm in thickness were successfully made with low stress and good electrical properties.

Table III. Measured Electron Transport Parameters and Stress

Samples	μ_e ($cm^2/V \cdot s$)	$(\mu\tau)_e$ (cm^2/V)	N_D^* (cm^{-3})	Stress (MPa)
standard a-Si:H (deposited at 250°C)				
	1.2	1.2×10^{-7}	7×10^{14}	350
standard a-Si:H (deposited at 150°C)				
as deposited	0.5	3×10^{-9}	2.5×10^{15}	80
annealed	0.5	7×10^{-9}	1×10^{15}	80
He-diluted(deposited at 250°C)				
	1.2	3×10^{-8}	2.5×10^{14}	320
He-diluted(deposited at 150°C)				
as-deposited	0.8	1×10^{-8}	3×10^{15}	90
annealed	0.8	2×10^{-8}	7×10^{14}	100

The stress of the as-deposited samples from pure silane are similar to those of He-diluted samples, but the N_D^* values are a little higher. For the sample deposited at 150°C, the N_D^* reached only 1.5 x 10^{15} cm^{-3} after annealing. Material properties of the as-deposited and annealed films, deposited at 150°C and 250°C, respectively, are listed in Table III. The μ_e did not change with annealing. The electron mobility-lifetime product, $(\mu\tau)_e$, of standard materials is about a factor of three higher than that of the He-diluted ones for the samples deposited at 250°C, and the trend is reversed for those deposited at 150°C. The $\mu\tau$ increased by a factor of two with annealing, which is thought to be partially due to the decreased deep trap (dangling bond) densities after annealing. The $\mu\tau$ value of 2 x 10^{-8} cm^2/V for the He-diluted, low temperature (150°C) deposited and annealed sample corresponds to a mean free path of 60 μm under an electric field of 30 V/μm, which is a normal bias field for a-Si:H p-i-n detectors, and is sufficient for thick detectors.

It is implied from this result that the low temperature deposition only lowers the internal stress and the He-dilution facilitates the material to restore low defect densities. Infrared absorption measurement indicated the existence of microvoids, which relax the internal stress, in the low-temperature materials both for He-diluted or pure silane. It also showed that there are tiny crystallites of the order of a few tens of atoms in the He-diluted layers. The lower defect density in the He-diluted material than in the normal a-Si:H has been attributed to the high level of hydrogen incorporation and heavily clustered microstructure, which are associated with the high deposition rate. Therefore, the He-diluted films prepared by low-temperature deposition and subsequent annealing are preferred over the standard a-Si:H since they have lower residual stress and faster deposition rate with electrical properties comparable to those of the standard films.

In the past, we demonstrated detection of alpha particles and 1~2 MeV protons in 30 μm thick detectors.[23] Beta particles from Sr-90 source was also detected with a 54 μm thick detector using 0.3 μsec shaping time.[32] These detectors were noticeably curved due to the high stress in the film. However, a 10 cm x 10 cm piece of the 50 μm thick film on a 0.8 mm glass substrate prepared by the new method was quite flat. The electrical properties were similar to those of the previous detectors.

III. PROPERTIES OF P-I-N DIODES

The average number of electron hole pairs, n_{min}, created from the interaction of the incident minimum ionizing radiation in intrinsic a-Si:H layer is given by

$$n_{min} = \frac{(\Delta E)_{min}}{W}$$

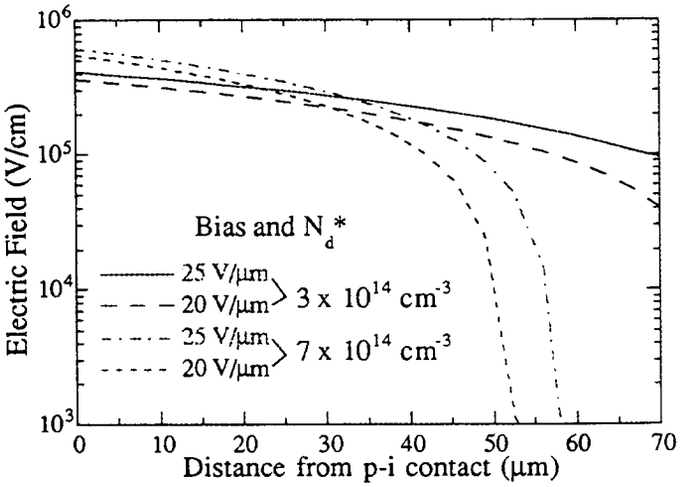

Fig. 5 Electric field in i-layer of a-Si:H n-i-p diode calculated for two different biases and ionized dangling bond densities

where W is the average energy required to produce an electron hole pair and $(\Delta E)_{min}$ is the energy deposited by minimum ionizing particles per unit track length. As $(\Delta E)_{min}$ of protons in silicon is 0.38 KeV/μm and W of a-Si:H is 4.8 eV, the average number of e-h pairs produced from a minimum ionizing proton is 80 per micron.[23] This corresponds to 4000 e-h pairs for a 50 μm-thick layer. In a pixel array configuration with a typical pixel size of ~300 μm or smaller, the detector noise would be fewer than 200 electrons and the generated signal would be about 20 times larger than the noise.

The non-bonding valence electrons, or dangling bonds, in the a-Si:H network lead to deep traps in the band gap and thus degrade the electronic property to a significant extent. As discussed in section I, in order to have a fully depleted detector, a minimum bias is needed which increases proportionately to the density of dangling bonds. The electric field profile inside the i-layer is given by the Poisson equation:

$$\frac{d^2\Phi(x)}{dx^2} = -\rho = -\frac{q N_D^*}{\varepsilon_o \varepsilon_{aSi}}$$

where $\Phi(x)$ is electric potential, ρ is electric charge density, ε_o is the dielectric constant of vacuum and ε_{aSi} is the relative dielectric constant of a-Si:H. The full depletion bias, V_f, is obtained as follows with the boundary conditions of $\Phi(0) = V_f$ and $\Phi(d) = 0$ where d is the i-layer thickness.

$$V_f = \frac{q N_d^* d^2}{2 \varepsilon_o \varepsilon_{aSi}}$$

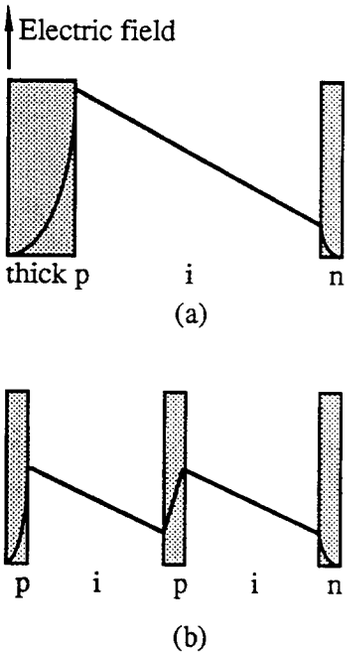

Fig. 6 Full depletion schemes: (a) thick p layer, (b) buried p layer

Therefore, the magnitude of the applied bias necessary for depletion of the i layer varies linearly with the ionized defect density (N_D^*) and is proportional to the square of the i layer thickness. Fig. 5 shows the depletion widths calculated for different values of ionized dangling bond density N_D^* and bias voltages.

For a 50 μm thick diode, with an ionized defect density of $5 \sim 7 \times 10^{14}$ cm^{-3}, full depletion can be achieved at a minimum voltage of 1300 V. In a normal diode with a doped layer thickness of 2-3 nm, application of such a large bias will result in a strong electric field at the p-i interface near the electrode, which in turn will trigger some breakdown mechanism. The peak field in the p-i interfaced can be moved away sufficiently from the contact region by increasing the thickness of the p layer to 20-30 nm as illustrated in Fig.6a. The depletion of the diode can be further promoted by depositing one or more thin p-layers in the middle of the intrinsic layer (see Fig. 6b).[24] This layer will reduce the required depletion voltage approximately by a factor of 2 and allow for the possibility of making 100 μm detectors using the same quality a-Si:H i-layer.

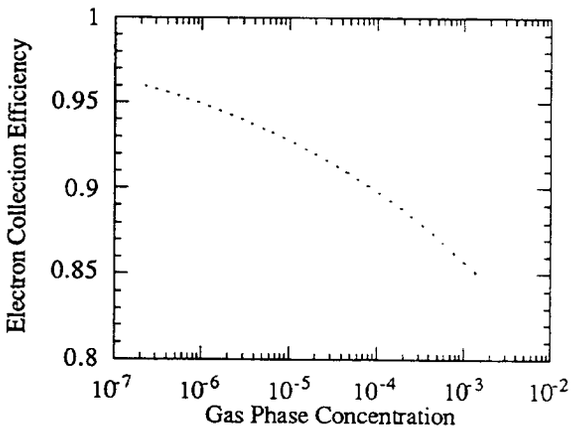

Fig. 7. Calculated electron collection efficiency as a function of the gas phase doping density of the buried p-layer in a 50 μm thick detector at a fixed bias of 1000V.

However, the p layer is expected to act as traps for electrons. In Fig.7, the electron collection efficiency, defined as the ratio of the number of electrons before and after passing the buried p-layer, is calculated for a hypothetical structure of a 50 μm-thick diode having one p-layer in the middle, and is plotted for various gas phase doping densities of the buried layer. As shown in this figure, the electron loss for a gas phase doping density as high as 1000 ppm is less than 15%.

IV. THIN FILM TRANSISTOR READOUT FOR PIXEL ARRAYS

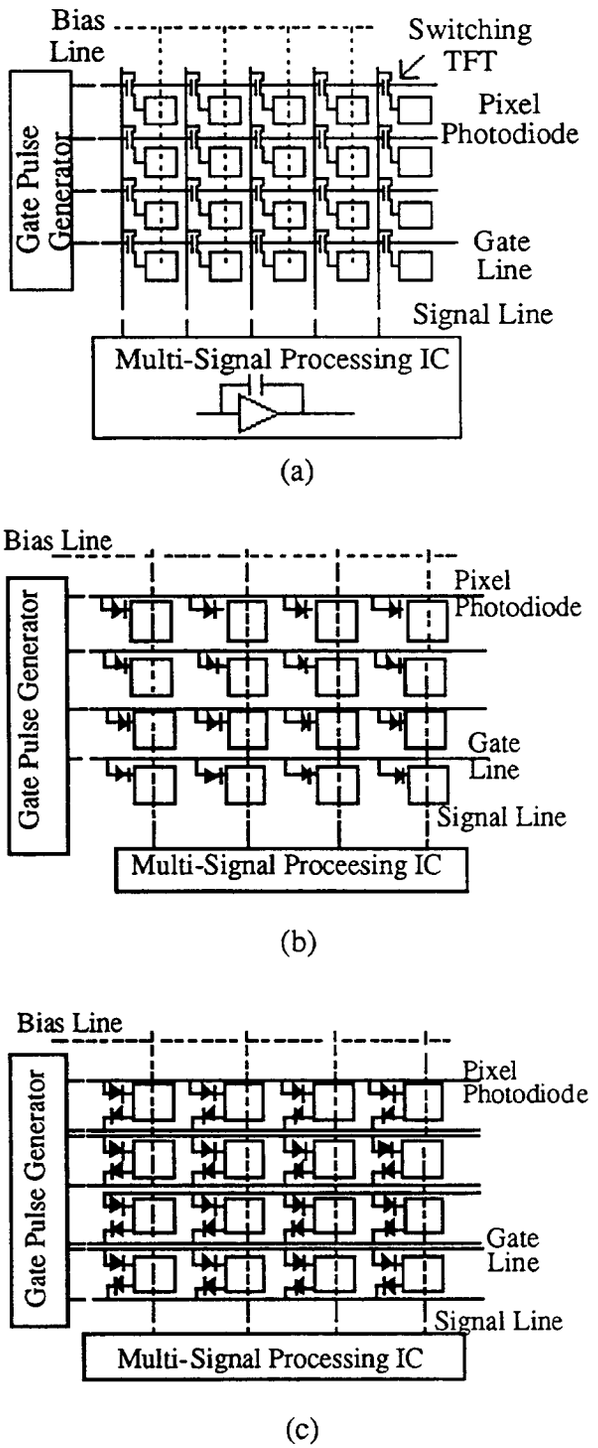

Fig. 8. Diode, TFT readout schemes (a) TFT (b) single diode (c) two diode switches

In many applications, the spatial distribution of the incident radiation is important. For example, a 2-dimensional array of detectors is required in applications such as tracking devices for high energy physics experiment, medical imaging, and synchrotron radiation transmission imaging for non-destructive examination. Hence, we use pixel or strip configurations with appropriately shaped metallic contacts. For other applications such as radiation flux detection, simple routing electronics may be sufficient. These configurations of detector and TFT arrays are shown schematically in Fig. 8. In Fig. 8a, each element is read out line by line by sending out a signal to the a-Si:H switching transistor in that line. The charge in the pixels in the tagged line can be read out by some integrated circuit chip with multiple inputs such as the SVX chip developed at Lawrence Berkeley Laboratory.[25] Alternative readout methods involve a single diode connected to each element (Fig 8b) or two diodes (Fig. 8c). The two diode readout is faster and has a larger dynamic range than the single diode scheme.[26] It also minimizes switching transients. Diode readouts have the following advantage compared to TFT; (a) they require fewer number of production masks, (b) they minimize radiation damage problems as SiO_2 or Si_3N_4 gate insulators are not needed.[26] Fig. 9 shows the structure of a-Si:H TFT, polysilicon TFT and a cross section of the diode readout.

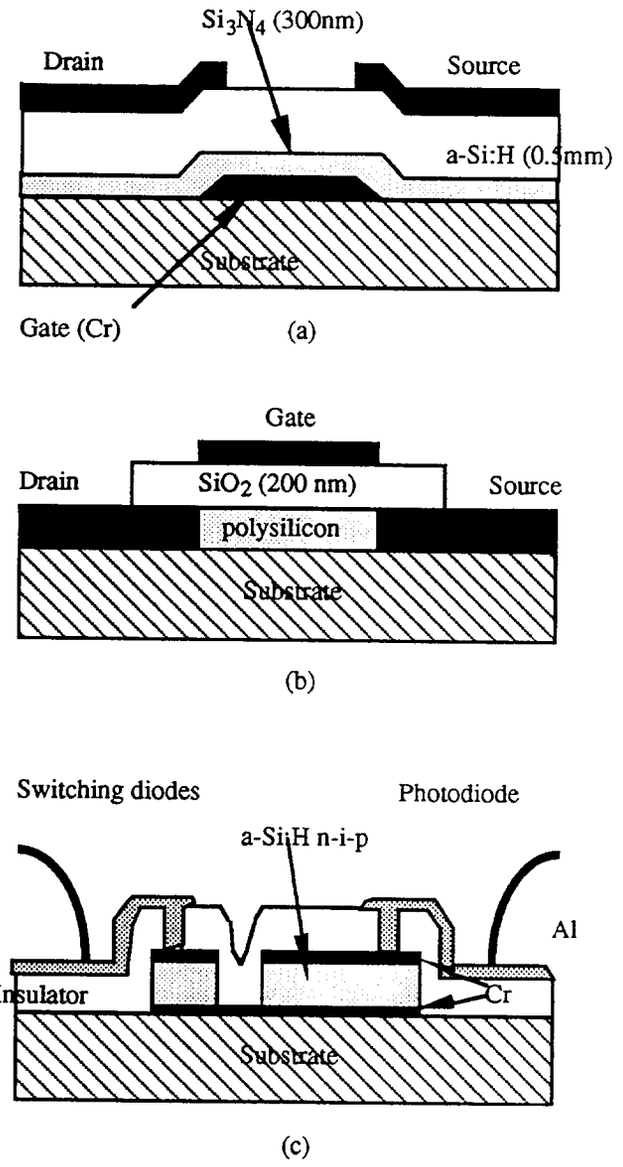

Fig. 9. Structure of TFTs and diode readout (a) a-Si:H TFT, (b) polysilicon TFT, (c) diode readout cross section

Two dimensional arrays of a-Si:H p-i-n diodes are good candidates for β-radio-chromatography applications. A radio-chromatogram consists of a column along which separation of components of a labeled mixture is possible by detecting the position and concentration of a series of spots or bands produced by accumulation of different component. Normally, β-emitters such as ^{3}H ($E_{\beta\ max}$ =18 KeV), ^{14}C ($E_{\beta\ max}$ =150 KeV), and ^{32}P ($E_{\beta\ max}$ =1.7 MeV) are used for labeling the mixtures. In a two dimensional scheme, a number of mixtures can be analyzed simultaneously, by using more columns on a chromatogram. For a real time analysis, a-Si:H pixel arrays have advantage of higher spatial resolution over the alternative systems such as multiwire proportional chambers (MWPC).[27] Thermal neutrons can also be detected by a-Si:H p-i-n diodes interfaced with Gd converters which emit an 80 keV internal conversion line. We have developed such detectors by evaporating ~2 μm thick Gd films on 20-30 μm thick a-Si:H diodes. Using a sandwiched structure with two layers of enriched Gd film in the ^{157}Gd isotope coupled to p-i-n diodes, thermal neutron efficiencies of more than 60% can be obtained.[28] Such detectors in a two dimensional configuration are excellent candidates for applications where high spatial resolution and good thermal neutron sensitivity with gamma rejection are desirable.

There are some applications that require amplification of the collected signal to bring it to a satisfactory level above the system noise. This can be accomplished by introducing a TFT amplifier made of polysilicon underneath each element of the array, and then reading the output by enabling lines as in the diode case. Amorphous silicon TFT can only be used as switching devices because the threshold voltage of the gate bias shifts continuously under dc bias.[29] True CMOS amplifiers can be made using polysilicon TFT since both electron and hole mobilities are

Table IV. Typical properties of a-Si:H and polysilicon TFTs

Property	a-Si:H TFT	Poly-Si TFT
μ_e (cm^2/Vsec)	1	150
μ_h (cm^2/Vsec)	0.005	80
g_m (μA/V)	5	150
Bandwidth (MHz)	5	100
Noise* (e)	500	500

*Equivalent noise charges for a CR-$(RC)^4$ shaping time of 1 μsec.

comparable and much higher than the corresponding ones for a-Si:H TFT. Table IV summarizes electronic characteristics of amorphous and polycrystalline silicon TFTs. Fabrication of polysilicon TFTs with high mobility and uniform microstructure in a low temperature process (<600°C) has been studied by various approaches for applications to LCDs and 2-dimensional image sensors. Recently, a field effect mobility as high as 440 cm^2/Vs, which is only about a half of that in single crystalline silicon, has been accomplished by an excimer laser annealing method.[30]

Using the facilities of the Xerox Palo Alto Research Center, we designed and tested 3-stage CMOS polysilicon amplifiers. The amplifiers consist of a charge sensitive input stage, a voltage gain stage, and a low impedance output stage for driving signals through a pixel array. This prototype amplifier design is shown in Fig. 10. The gain-bandwidth product of the amplifier is ~350 MHz. When the amplifier is connected to a pixel detector with a capacitance of 0.2 pF, it gives a charge-voltage gain of ~0.02 mV/electrons with a pulse rise time less than 100 nsec. An equivalent noise charge of the front-end TFT is ~1000 electrons for a shaping time of 1 μsec.[31]

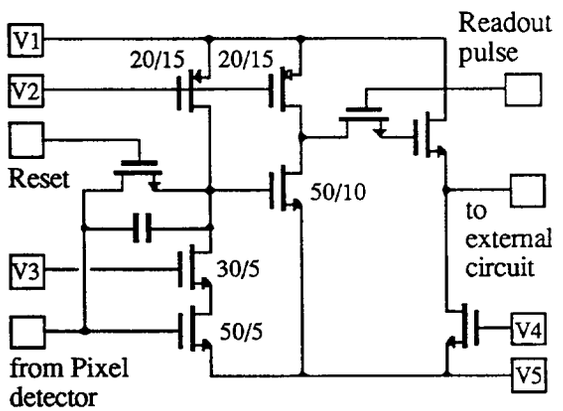

Fig.10 Schematic circuit diagram of the prototype polysilicon TFT charge sensitive pixel amplifier for a-Si:H pixel detectors. Each square with node numbers represents a test pad. N and P stands for n- and p-channel TFTs, respectively, and C for a capacitor.

The noise produced in a reverse biased p-i-n detector together with that of a typical readout amplifier should be small. In Fig. 11, the noise in a 26 μm diode as a function of reverse bias, measured by a charge sensitive amplifier with 2.5 and 0.5 μsec CR-$(RC)^2$ shaping times. The flat portion of the noise graph, at low biases, is the sum of the amplifier

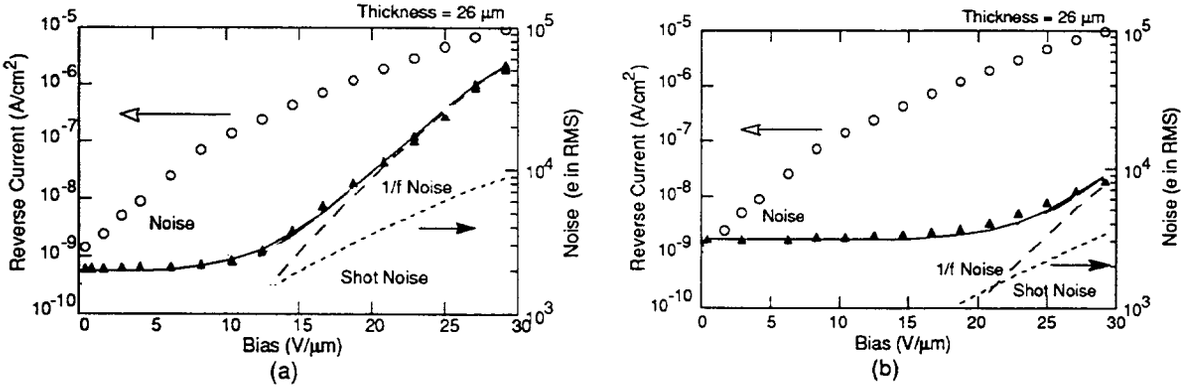

Fig. 11 Resistive, shot and 1/f noise in a-Si:H p-i-n detector diode at a shaping time of (a) 2.5 μsec. and (b) 0.5 μsec.

noise when loaded by the capacity of the detector and a mostly resistive (Nyquist) noise generated by the contact resistance and the p layer resistance. At higher biases when the reverse current increases, the contributing shot noise which has a flat frequency spectrum and is proportional to the current is observed. At still higher biases with larger reverse current, 1/f noise, which has the 1/f spectral response and is proportional to I^2 becomes predominant. All of these noise components are proportional to the area of a pixel detector.

The signal response as a function of shaping time can be calculated from the mobility and the electric field in the i layer at a given bias. Figure 12 shows the signal from electrons and holes for a 50 μm thick diode. The material parameters used in the calculation are μ_e = 1 cm^2/Vs, μ_h = 0.005 cm^2/Vs, $\tau_e = 9 \times 10^{-8}$ sec., $\tau_h = 3 \times 10^{-6}$ sec. Fast timing in less than 10 nanosecond is achieved by collecting the full electron signal only.

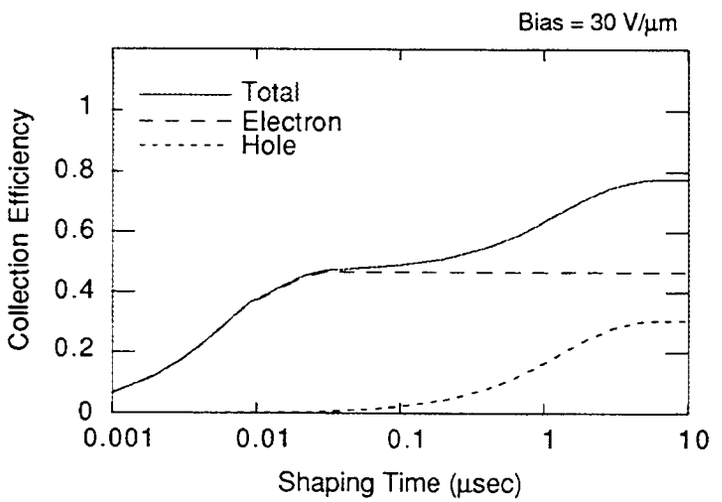

Fig.12 Normalized electron and hole collection efficiency for a p-i-n diode with 50 μm thick i-layer

V. CONCLUSION

We have explored the effects of helium dilution of silane on various material properties of a-Si:H films. Thick a-Si:H films for minimum ionizing particle detection were made with low internal stress by deposition at low temperature in order to minimize substrate bending and delamination. He-dilution of silane and post-deposition heat treatment restored the degraded electronic quality to a satisfactory level. 50 μm-thick films made by this technique showed internal stress of 100 MPa and N_D^* as low as 7×10^{14} cm^{-3} after annealing. The electron mobility and $\mu\tau$ value of the He-diluted and annealed materials were comparable to those of conventional a-Si:H films. On the average, a minimum ionizing proton would produce 4000 electrons in the 50 μm-thick diode and the resulting signal to noise ratio would be 20 when the pixel size is ≤ 300 μm.

He-diluted material is good for thick diodes for direct detection of charged particles due to the high deposition rate and low ionized defect density. Low temperature deposition and subsequent annealing produces films under low stress and of reasonably good electrical properties. In addition, a-Si:H is a suitable material for large area devices, and the 2-D pixel array of a-Si:H integrated with readout circuit is a crucial technology for flat screen displays.

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