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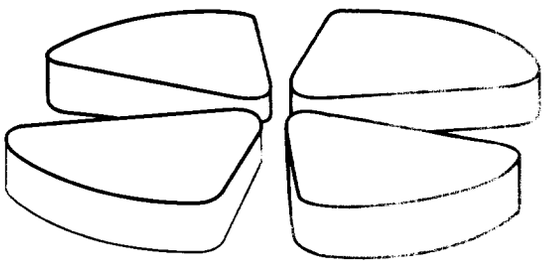

The electronics of the INDRA 4π detection array

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Abstract

INDRA is a 4π detection array designed for the studies of "hot nuclei" at the heavy ion accelerator GANIL. The INDRA multidetector is composed of 96 ionization chambers, 196 silicon detectors, 324 CsI(Tl) scintillators and 12 NE102/NE115 phoswich detectors. This article describes the associated electronics. The signal treatment is performed through specifically designed modules, most of which are in the new VXIbus standard. This standard allows us to considerably reduce the number of modules by regrouping many functions in the same module. For example, all the functions related to 24 CsI(Tl) scintillators are stacked in one D-size module. VXIbus also provides the opportunity to locate all the electronics close to the detector, in the beam cave, with full remote control (VXI-VME buses) including visualization of analogic and logic signals on oscilloscopes. The large dynamic range (4000 to 1) required for the silicon detectors is reached by means of a new method : a low noise amplifier providing a unipolar signal which is charge integrated and converted on two dynamic ranges. The trigger system relies on a new working mode called "asynchronous mode" and performs event selections based on multiplicity functions which are built up from subgroups of detectors. The performances of the data acquisition and the graphical software packages which were developed to set up and control the electronic parameters are also presented.

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1. Introduction

The formation and decay of hot nuclear systems formed in heavy ion collisions at intermediate energies is one of the major research axis at GANIL (Grand Accélérateur National d'Ions Lourds, Caen, France). The ultimate goal is to form highly excited nuclei at the "limit of stability". In the last few years, theoretical approaches predicted new decay modes for these nuclei, especially the possibility of a "sudden multifragmentation" of the nucleus, accompanied or not, by a phase transition. The de-excitation of very hot nuclear systems is characterized by the emission of a large number of "light charged particles" (hydrogen and helium nuclei) and, to a lesser extent, heavier fragments. Experimental studies require an event by event detection of all particles and fragments, with precise measurements of their number, their size (charge, mass), their spatial distribution and their energy. To satisfy these requirements, the community of physicists interested in the multifragmentation process at the GANIL Facility decided in 1989 to undertake the construction of INDRA which is able to detect, in charge, complete or quasi-complete events. In 1993 and 1994, two sets of experiments which lasted two months each were successfully run with INDRA. Argon, nickel, krypton, xenon, gadolinium, tantalum and uranium beams bombarding various targets were used.

A split view of INDRA is shown in Fig. 1. The multidetector array which operates in vacuum, covers about 90% of the space around the target. It can be schematically described as an ensemble of 336 detection cells arranged according to 17 rings centered on the beam axis. In order to compensate the forward peaked angular distributions of emitted particles, the solid angle subtended by each cell increases by a factor of 100 from ring 1 (forward angles) to ring 17 (backward angles). Due to high counting rates expected at very forward angles, the first ring ($2°<\theta<3°$) is made of 12 fast NE102/NE115 phoswich detectors, enabling charge identification up to Z=30 for fragments having an energy greater than 20 A.MeV. For rings 2 to 9 ($3°<\theta<45°$), the charge identification (up to Z = 50) is achieved through the usual $\Delta E/E$ method, by measuring the energy deposited in three detection layers of increasing thickness : a low pressure gas-ionization chamber, a 300 μm thick silicon detector and a CsI(Tl) scintillator thick enough (14 to 10 cm depending on the ring) to stop all particles. In the last 8 rings ($45°<\theta<176°$), the energy range of the fragments is much smaller and only two stages of detection are used : gas ionization chambers and CsI(Tl) crystals of a thickness from 8 to 5 cm. The ionization chamber layer with almost 4π solid angle coverage and high geometrical efficiency is certainly the most original feature of the detector, since it gives charge identification from very low energy thresholds ($\approx$ 1 A.MeV). Identification of H and He isotopes is obtained by using pulse shape discrimination techniques on the CsI(Tl) detector signals. INDRA is therefore composed of 12 phoswich detectors, 96 ionization chambers, 180 silicon detectors and 324 CsI(Tl) scintillators. For energy calibration purposes, rings 10 to 17 ($45°<\theta<176°$),

which do not incorporate silicon detectors were each equiped with a two-element telescope (80 μm and 2 mm thick silicon detectors). The INDRA 4π array, the detectors and the performances obtained are presented in Ref. [1]. The present paper presents the electronics which was not described in this reference.

The INDRA detectors have the intrinsic capacity of satisfying the required specifications concerning nucleus identifications and energy resolutions. However, the energy measurements must be performed on a large dynamic range as, for example, from 1 MeV to 4 GeV for silicon detectors with an energy resolution of a few hundred of keV. Such a performance could not be obtained by using conventional methods and commercially available electronic modules. Furthermore, the complexity of the electronics associated with the large number of channels raises some difficulties related to its tuning, control and overall management. Consequently, a number of complementary requirements were placed on the design of the INDRA electronics and data acquisition : i) a very low noise level and a large dynamic range, ii) a close proximity to the detector, iii) a minimum number of connectors, iv) a full software control of settings, v) a compatibility with the VME based GANIL acquisition [2] and vi) an easy visualization of the relevant signals. To meet these requirements the electronics had to be adapted to the specifications of the detectors and so, most of the electronic modules were designed and constructed by the collaborating laboratories. Among the particular features which contribute to the final performance, the following should be pointed out. An important effort was invested in the design of the reaction chamber, the detectors, the front end electronics and connections, with special care being paid to the ground reference in order to avoid crosstalk and ground loop effects. Requirements i)-ii) imply that the front end electronics (preamplifiers and photomultiplier bases) are located inside the reaction chamber, as close as possible to the detectors. These devices and their associated cable connections which must be fed through the vacuum chamber are presented in section 2. In order to entirely fulfill the requirements i) and ii), it was also decided that all the electronics should be placed in the beam cave. In conjunction with items iv) and v), this had important consequences concerning the choice of a new standard : the VXIbus. The VXIbus [3] has been developed for high quality electronic applications and compatibility with the VME computer bus. It allowed us to considerably reduce the number of modules and connections (item iii) by grouping many functions in the same module. This choice also has the additional advantage of allowing the development of an easy to use and remotely controlled visualization of the signals (item vi) without cable disconnections. The INDRA electronic architecture which is largely based on the VME and VXI buses is discussed in section 3.

In relation to signal processing and encoding, INDRA is composed of two kinds of detectors : i) Scintillators (phoswich and cesium iodide) which need a double signal integration in a "fast gate" and a "slow gate" ; ii) Ionization chamber and silicon detectors for which energy measurements have to be done on a large dynamic range (more than 1000 to 1). This last

performance is obtained by means of a new method which is discussed in section 4. The associated electronic modules are presented in the same section. The signals coming from the CsI(Tl) scintillators are fed to 24 input VXIbus modules containing all the necessary processing functions. This module is presented in section 5. A similar VXIbus module with 16 inputs is used for the phoswich detectors. The new method of triggering called "asynchronous mode" is briefly described in section 3 and their associated electronic modules are presented in section 6. The time measurements (10 ns resolution) necessary to estimate the importance of random coincidences are performed in 96 input VXIbus modules which are briefly described in the same section. Section 7 presents the data acquisition system and its performances as well as the graphical software packages developed for the control of the electronic modules.

2. Electronics inside the vacuum chamber

The 336 photomultiplier bases associated with the scintillators (324 CsI(Tl) and 12 NE102/NE115 detectors) and the 292 charge preamplifiers coupled to the ionization chambers (96 channels), the 300 μm thick silicon detectors (180 channels) and the calibration telescopes (16 channels) must work under vacuum. This section presents these devices and discusses the problems of power consumption. In order to satisfy the requirements of very low crosstalk and noise levels in signal transmissions, a standardized system of connections has been developed. This system, also used for the analog transmission of signals between the electronic modules, is described at the end of this section.

2.1 Low consumption and fast recovery photomultiplier bases

The decay time of CsI (Tl) crystals consists of two components of $\approx$ 0.5 μs and $\approx$ 7 μs. This means that, for a given signal amplitude, the total charge is much higher than that usually given by other scintillators. Therefore, the associated photomultiplier has to deliver high charge output per signal and this demand is equally required of the photomultiplier base. It became rapidly clear that the standard RC chain was inadequate [4]. We turned therefore to a transistorized photomultiplier base. Fig. 2 shows the principle of such a base for a 8 dynode (D_1 to D_8) photomultiplier. The charge supplies to the dynodes are the capacitors C_k to C_8. As these capacitors are discharged by dynodes, one has to replenish them as quickly as possible in order to maintain the stability of the interdynode voltages. It is the bias current, I_b , which replenishes the capacitors C_k to C_8. Since the maximum signal is given at the output stage (the anode), the capacitor C_8 must deliver the maximum charge $Q_8 = Q_a$ and has to be replenished with the whole current, I_b. This is accomplished by opening the switch SW_8 so that the total bias current I_b rushes into the C_8 capacitor, to make up for the lost charge Q_8. As soon as the C_8 capacitor is

recharged, the switch SW_8 closes again, so that $I_b.R_8$ equals the voltage V_{C8}. One practical solution of the SW_8 switch could be obtained by a transistor as shown in the inset of Fig.2. The switches (SW_8, SW_7...) of Fig. 2 are only used where the discharge of the interdynode capacitors is significant. Practically, one only controls 3 to 5 stages by switches. The rest of the chain is of the RC-type. Such a transistorized photomultiplier base works well if it is adapted to the charge of the anode signal and the counting rate.

The bias current is calculated by :

$$I_b \geq 2.7\ \lambda\ Q_a \qquad (1)$$

and the capacitor C_8 is given by :

$$C_8 \geq 10^2\ Q_{a\,max} / V_8 \qquad (2)$$

where λ is the average counting rate, Q_a the average anode charge, $Q_{a\,max}$ the maximum anode charge and V_8 the DC voltage of dynode D_8.

The subsequent capacitor C_7 is calculated by $C_7 \geq C_8 / g_8$, where g_8 is the current gain of the dynode D_8. Similarly, $C_6 \geq C_7 / g_7$. If we want an average anode signal of 2.5 V pulse height (which corresponds to a charge Q_a = 55 nC) with an average counting rate of $\lambda \leq 500$ counts/sec, the expression (1) gives us $I_b \geq 75\ \mu A$. As the transistors Q_8 and Q_7 need a minimum quiescent current of approximately 10 μA, the bias current will be $I_b = 85\ \mu A$.

Fig. 3-a shows the waveforms of the dynode D_8 voltage (V_{D8}) and the cathode K-dynode D_1 voltage ($V_{K\text{-}D1}$) for a transistorized photomultiplier base with $I_b = 85\ \mu A$ and for an anode signal of 2.5 V. The photomultiplier type is the Philips XP2961. One can note that the voltage V_{D8} across C_8 drops to less than 1V and that the capacitor is replenished within 700 μs. The $V_{K\text{-}D1}$ voltage also drops to less than 1V and recovers within the same time as V_{D8}. The curves were obtained by a computer simulation (VALID-AWB), but the measurements performed on a real photomultiplier base gave the same results. The excellent simulation precision is due essentially to the correct photomultiplier modelling. For comparison purposes, one can find in Fig. 3-b, the waveforms in the case of a resistor-only (or RC) photomultiplier base. Note that the bias current is $I_b = 850\ \mu A$, a value which is ten times greater than that for the transistorized base. For this RC-base, the voltage V_{D8} recovers exponentially with a constant of around 15 ms and reaches 90% of its original value in a time greater than 40 ms.

The transistorized photomultiplier base developed for the INDRA detector dissipates 10 times less power and recovers 30 times faster than its resistor-only (or RC) counterpart. The low power consumption of these bases allows one to work under vacuum without cooling. The maximum counting rate fixed at 500 counts/sec is sufficient for the CsI(Tl) detectors of rings 4 to 17. However, in rings 2 and 3 the base current is $I_b = 150\ \mu A$ in order to accept counting rates up to 1000 counts/sec. A similar transistorized base has been developped for the 12 phoswich (NE102/NE115) detectors. Due to the relatively fast decay constant of the scintillators (2.4 ns for the NE102 and 240 ns for the NE115), the maximum counting rate has been

increased to 5000 counts/sec with a base current of 200 μA. A cooling of the photomultiplier bases is still not necessary.

2.2. The charge preamplifiers

The charge preamplifiers are associated with two types of detectors for which the required characteristics are different. Due to the low energy deposit and low current conversion in the ionization chamber, the preamplifier must have a very high sensitivity together with a low noise. Conversely, the main feature of the silicon detector preamplifier is its high dynamic range capability which leads to a low sensitivity and thus to a channel noise figure dominated by the following amplifier (see below, section 4). Therefore, two types of preamplifiers were developed. In order to fulfill the characteristics requirements and to get low overall dimensions, both preamplifiers are constructed with SMT (Surface Mounted Technology) components.

Fig. 4-a shows the circuit diagram of the ionization chamber preamplifier. The input stage is a conventional cascode circuit composed of a field-effect transistor T_1 of transconductance g_m followed by a fast current amplifier A_i of gain G_i. This stage (T_1, A_i) is equivalent to a transistor of $g = g_m \times G_i$ transconductance. Thus, the open-loop voltage gain is increased by the factor G_i and reaches 30 000 in the filter band-pass (100 kHz). The dynamical capacitance is around 6 nF, a value which is greater than the few pF detector capacitance. The preamplifier output stage delivers negative or positive signals with a maximum amplitude for a linear response of 5 V on 100 Ω, i.e. 2.5 V on the 50 Ω impedance of the amplifier input. The very high sensitivity is obtained by a low feedback capacitor C_r of around 0.22 pF. This sensitivity which is equivalent to 200 mV/MeV for silicon detectors leads to pulse amplitudes of 20 mV/MeV for ionization chambers filled with C_3F_8 gas. The capacitor C_r of 0.22 pF is not available as a component and moreover the interference circuit capacitors must be included in this value. In fact, the capacitor C_r is made of two copper lines which are separated by a short distance on the printed circuit board. The value of C_r is adjusted by increasing the distance between the two copper lines. The value is fixed by a bench test measurement where the preamplifier sensitivity is compared to a reference one. This method allowed us to adjust the 96 preamplifier sensitivities to within 1%. The main characteristics of these charge preamplifiers are given in Table 1. They have been controlled for the 96 devices on the test bench constructed for the gain tuning.

Fig. 4-b shows the circuit diagram of the silicon detector preamplifier. The most important feature is the high dynamic range needed and thus one must consider, instead of the noise, the open-loop voltage gain and the rise time characteristics. The input stage is a field-effect transistor T_1 working as an impedance corrector. The high open-loop voltage gain is obtained by a cascode circuit composed of the bipolar transistors T_2 and T_3. This gain is controlled through the variation of the dynamical input impedance of T_2 with the value of the current generator I_1. The open-loop voltage gain, measured in the filter band-pass (100 kHz), is around 100 000. The preamplifier output stage works for the two signal polarities. Nevertheless, a fast signal rise time of 25 ns is only obtained on

the negative excursion for the full dynamic range with a 200 pF detector capacitance. In fact, the preamplifiers were optimized for negative output signals and the capacitances of the INDRA 300 µm thick silicon detectors which vary from 140 pF to 400 pF. The preamplifier output stage delivers negative output signals of up to -10 V on 100 Ω, i.e. -5 V on the 50 Ω impedance of the amplifier input. The 180 devices were checked on a test bench. The sensitivity variations do not exceed ± 1% as expected with the choice of the C_r component (COG in the EIA specification : value within ± 1%, temperature coefficient of 0 ± 30 ppm / °C). The main characteristics of these charge preamplifiers are summarized in Table 4. The 16 silicon detectors which compose the 8 calibration telescopes are equipped with similar charge preamplifiers which provide positive output signals with maximum amplitudes of + 5 V on 100 Ω.

As discussed in Ref [1], the preamplifiers are located as close as possible to the detectors and are mounted in groups of 4 to 6 devices on multilayer printed circuit boards. The large dynamic range needed in the energy measurements led us to develop charge preamplifiers which can deliver high amplitude signals. Even if particular care was taken in the preamplifier designs, the power consumption is too high for working under vacuum conditions [1]. A water based cooling system had to be implemented in order to remove the excess heat. After 10 hours of water circulating at 10 °C, the temperature stabilizes at 20°C on the mechanical supports of the printed circuits boards.

2.3. Analog signal transmission. Cables and connectors

The photomultiplier bases and the preamplifiers are located in the vacuum chamber. These devices must be connected to the electronic modules with a relatively large number of cables : 888 for signal transmissions and 405 for high voltage power supplies. Moreover, due to the large dynamic range in energy measurements, the noise pickup and the cross-talk between channels must be held at very low levels. In order to meet these requirements and to reduce the costs, a specifically designed system of coaxial cable connections has been developed. This technique makes use of standard and low cost 2.54 mm contact pitch connectors, as shown in Fig. 5. Two types of connections have been standardized and implemented on the vacuum chamber flanges. The signals and the moderate high voltage bias (< 600 V) associated with the ionization chambers and the silicon detectors are grouped by 16 channels (S.1 to S.16) on a 53-contact connector (Fig. 5-a, left-hand side). The ground shielding between the channels is ensured by the remaining 37 contacts and the implementation of the coaxial cables as shown in Fig. 5-b. The braids of the coaxial cables are soldered on both sides of a three-layer printed circuit board. The central layer of this circuit is also grounded. The interconnections of analog signals between the electronic modules also rely on the same technique. The coaxial cables are grouped by 8 on a 29-contact connector with a distribution of the 8 signals and ground interconnections corresponding to half (S.1 to S.8) of the 53-contact connector of Fig.5-a. Despite a non-coaxial transmission through the connectors, the short distance involved together with the relatively slow rise time of the signals (> 25 ns) does not introduce significant signal

perturbations. The most important feature is the high performance of this design technique in regard to electro magnetic compatibility (EMC). In particular, a very low cross-talk is obtained and a signal of 5 V in amplitude and 25 ns rise time induces on an adjacent channel an interference signal of less than 1 mV in amplitude. For the scintillator detectors, the high voltage biases of the photomultipliers are set between 1000 V and 1600 V. Another connector was designed for the connections through the vacuum chamber flanges (Fig. 5-a, right-hand side). In order to obtain a safe distance between the high voltage contacts, the grounded contacts surrounding them were removed. We checked that this type of connection gives satisfactory working conditions for high voltages up to 3000 V. For the signal connections we kept the same design with grounded contacts around S1 to S8. Such a technique allows us to connect, on one small-sized device, a set of 8 scintillator detectors. The implementation of the connectors on the vacuum chamber flange is shown in Fig. 6. Ten connectors are soldered onto a printed circuit of 160 mm diameter and 6 mm thickness. All ground contacts are connected to a plane which constitutes a ground reference connected to the flange, and so to the reaction chamber, by a silver-filled epoxy glue (EPO-TEK H20E from Epoxy Technology). The reaction chamber which is electrically insulated from the beam pipe and the floor can then be considered as the main ground reference of the setup. The air-tighness is obtained by the contact soldering on the printed circuit and reinforced by the deposit of an insulated epoxy resin (EPO-TEK H77) on both sides of the printed circuit. In order to respect the two connector designs, two types of printed circuit are used. On the flange associated with the scintillator detectors, one can connect 80 detectors, i.e. 80 signal and 80 high voltage lines. For the other detectors, the number of available coaxial connections is 160.

3. Electronics architecture

The design of electronics with commercially available NIM or CAMAC modules would have led to a large number of them with a numerous connections and several front pannel adjustements of parameters. Moreover, the high dynamic range energy measurements are very difficult to perform following the classical signal processing method provided by these modules. Facing these problems and in order to reduce the costs and increase the quality and the reliability of the system (see section 1), we decided to design and build electronic modules using mainly a new standard, the VXIbus (VME Extension for Instrumentation). Developed by a consortium of test equipement manufacturers, VXIbus [3] is an architecture for modular instruments based on the VME computer bus [5] which was already used for data acquisition at GANIL [2]. This being the main reason for our choice, we can mention other advantages : a good shielding of the modules, a satisfactory Power Distribution Bus (±24V, ±12V, - 5.2V, +5V, -2V), multiple possibilities of connections by different backplane buses (ECL or TTL lines, clock signals). A VXIbus system consists of a central timing module (Slot 0) and up to

12 additional instrument modules in four different sizes with the same width (1.2 in.). We choose the bigger one (D size : 14.4 in. x 13.4 in.) which provides all VXIbus facilities and gives the maximum room for implementation of analog components on daughter boards and so allowing a considerable reduction in the number of modules.

Fig. 7 shows the architecture of the electronics which is, as indicated in section 1, located in the beam cave with no access during the beam periods. The data acquisition system is the standard GANIL one running on VME based CPU and an optical fiber link transmission to a central VAX computer [2]. Using VXIbus does not mean that the totality of the electronic modules must be constructed in this standard. The link between the VME and the CAMAC crates is still available and we used CAMAC modules to implement functions which do not need fast data readout. The high voltage power supply system is composed of 8 CAEN Model SY403 crates [6]. Each crate contains up to 64 independent channels arranged in boards of 16 channels and the system is controlled via the serial link "caenet" from the VME. The scalers are VME modules (16 channels CAEN modules, [6]) and are housed in one VME crate which is linked to the central VME master crate by the VMV bus provided by the CES company [7]. The same solution has been adopted to incorporate the VXIbus. The Slot 0 modules are the STR8032 ones, designed at the Daresbury laboratory [8] and commercially available from the Struck company [9]. The board for this module allows one to accommodate any commercial VME processor and we used the VIC8250 from CES which contains the access through the VMV bus. As a consequence, for data acquisition and parameter software control, the VXIbus system works like the VME one. These Slot 0 modules also provide access to some of the VXIbus backplane lines through front pannel connectors and buffered circuits. This facility allowed us to distribute the trigger signals to the modules by a "trigger bus" simply connected from the trigger VXIbus crate to the Slot 0 modules of the other crates. It also permitted the introduction of standardized remote visualizations of signals. On the VXIbus crate backplane, five lines are assigned to these functions : 2 lines for analog signals, 2 lines for logic ones and 1 line for coincidence adjustments ("gate control"). Under software control, the signals inside the modules can be multiplexed and accessed through 5 coaxial connectors (Lemo 00) on the VXIbus Slot0 front panel and displayed on oscilloscopes. Thus, the connections to the INDRA electronics are reduced to VME-Computer links (Ethernet and data optical fibers) and to a set of 20 coaxial cables (5 per VXIbus crate) for remote visualization of signals.

A new method for the ADCs timing has been introduced. Fig. 8 shows schematically its logic, called "asynchronous mode". The integration gate opens when the corresponding discriminator fires and without any logic condition coming from the trigger. At the end of a delay of around 1 μs, a "validation point" is generated. Each encoding channel cycles on its own (start -> integration gate and validation point -> reset) as long as the event configurations are rejected by the trigger (fig. 8a). Once a configuration is accepted, the trigger issues a "validation gate" to all the encoding modules enabling to proceed and to convert only those

channels which have their "validation point" in coincidence with the trigger gate (Fig. 8b). A "start coding" signal generated by the trigger starts the digital conversion. During this operation, and until a reset is emitted at the end of data acquisition, all the channels are disabled by a general "ADC inhibit" signal. The fact that the validation is delayed by 1 μs gives time to prform complex triggering functions and to wait for slow detectors. However, the most important advantage stands in the individual channel working which avoids the use of cumbersome long delay lines which deteriorate the linear signals.

Table 2 summarizes the INDRA standardized buses, their functions and their implementation in the VXIbus system : external access through the Slot 0 module and distribution on the VXIbus backplane. The "trigger bus" which achieves the connections between the trigger crate and the other ones, is composed of 9 logical lines : two "validation gates" (same function with different timing settings), "start coding", "ADC inhibit", "general reset", "discriminator inhibit" (used to stop all discriminators), "ADC test" (used to fire the test pulse signals directly inside the encoding modules) and two lines used for data acquisition purposes ("ADC coding line" and "ADC reading line"). The parameter settings are provided by VME and digital to analog conversion inside the modules. Results of this conversion can be controlled in the Slot 0 (ADC conversion and VME reading) in sending the analog value on the "voltage measurement" line. In the VXIbus standard, 2 clock signals of 10 MHz and 100 MHz frequencies are generated in the Slot 0 module and distributed in the crate. Both of them have been used in the trigger module and the 10 MHz line for logic sequencing in the other modules. Among the advantages of VXIbus, we can also underline the autoconfiguration of modules. The individual module identification line, MODID, allows one to test for the presence of a module, and to identify each module's location by a slot number. The system automatically identifies each device, its type, model manufacturer, and all the requirements of memory loading. As a consequence, all modules can be directly accessed for initialization or data readout without any modification of the acquisition files, even if a module location has changed.

4. Large dynamic range energy measurements (ionization chambers and silicon detectors)

4.1. Limitations of classical electronics

In association with an ionization chamber or a silicon detector, a charge preamplifier normally preserves the intrinsic high resolution energy capability of these detectors. The energy measurements are usually achieved by a "spectroscopy amplifier" and a peak sensing ADC. However, the dynamic range that can be covered by a standard electronics is generaly limited to 100 to 1. The main reason for this limitation comes from the stretcher of the ADC which cannot

satisfactorily work on low level signals with rise times of a few μs. In order to obtain a higher dynamic range, a second amplifier with a different gain is generally introduced. For example, one amplifier and its associated ADC covers the energy range from 1 MeV to 100 MeV whereas the second chain is adjusted for the 10 MeV to 1 GeV range. This method is not free of difficulties, particularly with regard to the very long recovery times of the high gain amplifier for energies largely exceeding its range. The electronics generally used with a ionization chamber or a silicon detector has been developed for very high resolution and low dynamic range energy measurements. In these spectroscopy amplifiers, one of the most important features is the optimization of the signal to noise ratio. This leads to complex shaping networks such as the approximate semi-Gaussian shaping performed with a network consisting of a CR differentiation followed by four RC integration stages. The large number of channels (292) needed to equip INDRA and the limitations and relative complexity of classical electronics led us to study new methods of energy measurement on a large dynamic range .

4.2. A new method : a low gain amplifier and a double charge encoding

In order to overcome the dynamic range limitation due to the pulse height encoding, one could introduce an acceptance time window centered on the peak of the amplifier pulse. Satisfactory working conditions of the ADC stretcher could be obtained if care has been taken to ensure the timing accuracy of the gate signal. To avoid precision timing considerations, which are basically non necessary in INDRA, we turned to another method based on charge sensitive ADCs. Let us assume that the amplifier output is purely unipolar and that a logic pulse (a gate) with a width larger than the linear signal could be generated (these hypotheses will be discussed below). A charge integration of the amplifier pulse is performed during the gate and thus a voltage proportional to the surface of the linear pulse is obtained. Concerning the dynamic range, there is no limitation due to the noise of the linear pulse. For instance, with a 12-bit A/D converter, one could expect energy measurements from a few channels (≈10) to the maximum (4095) with an intrinsic resolution of 1 or 2 channels. Unfortunately, these characteristics do not satisfy the requirements of the energy measurement resolution for the silicon detectors. If we assume that the maximum energy is 4 GeV, a 12 bit ADC has a 1 MeV per channel resolution which is ten times the resolution required for low energy measurements. In fact, for the silicon detectors, an equivalent dynamic range of a 16-bit ADC is needed. Different techniques could be use to construct these ADCs. We experimentally explored three of them on prototype circuits [10]. The large number of channels imply that several charge integrators must be associated with a common converter through a linear multiplexer. We found that the settling time and the resolution of the available multiplexer circuits were not compatible with 16-bit ADCs. Another technique, largely used in the LEP OPAL detector, is described in Refs [11] and [12]. The outputs of 32 charge integrators are multiplexed and simultaneously fed into two

chains of conversion : a conventional 12-bit ADC and a x8 amplifier followed by another 12-bit ADC. On our prototype we extended the 15-bit dynamic range to a 16-bit one with a x16 amplifier gain. As in the first method, the charge integration must be performed with a high resolution since the noise will also be amplified by a factor 16. In particular, the reference voltage of the integrator must be very stable. On our prototype, we found a resolution of 5 channels (fwhm) for the 16-bit range, a value compatible with the typical pedestal distribution (for a 15-bit range) presented in Ref. [12]. Better results have been obtained with a third method : a dual range conversion based on two charge integrations per channel. Each integrator is associated with a multiplexer followed by a 12-bit ADC. A x16 factor between the two ranges called "high gain" and "low gain" is simply obtained in varying the integrator capacitances by a factor 16. The main advantage over the previous technique is the lower quality required for the charge-integrating front end on the high gain range which is limited to an equivalent 12-bit dynamic range. Intrinsic resolutions of one channel have been obtain for the low gain (32 nC full scale range) as well as for the high gain (2 nC full scale range). For silicon detectors, this technique leads to energy measurements which are performed by two simultaneous 12-bit encoding : a few MeV to 4 GeV with 1 MeV per channel ("low gain") and a few hundred of keV to 250 MeV with 62 keV per channel ("high gain").

We have now to consider the hypotheses introduced, in particular about the possibility to obtain unipolar shaped pulses compatible with the resolution required. A 100 keV resolution seems to be so large that the choice of the shaping amplifier becomes trivial. Unfortunately, in the numerous works on the optimization of the signal to noise ratio, high dynamic range measurements are not considered. The discussions are generally limited to a careful evaluation of the detector and preamplifier noises and the effect of different pulse shaping on these noises [13, 14]. In a spectroscopy chain, the intrinsic noise of the filtering amplifier need not to be considered since the noise is dominated by that of the preamplifier. Conversely, in a high dynamic range chain, the preamplifier and amplifier must be set at such low gains that the energy resolution is dominated by the amplifier noise as shown in Ref. 15. The INDRA preamplifier provides 1 mV pulses on 50 Ω for 1 MeV deposited in the silicon detector. The intrinsic resolution is 14 keV at FWHM and corresponds to a noise of 6 μV (rms) at the amplifier input which has to be compared to the intrinsic amplifier noise. For the spectroscopy amplifier Enertec 7129, the manufacturer gives the equivalent input noise voltage : 3 μV (rms) for a high gain and 80 μV (rms) with the minimum gain limited to 3. With this amplifier, the resolution is 190 keV (fwhm) for the amplifier gain set to 3. Lower gains, necessary to process the 4 V pulse which corresponds to an energy deposit of 4 GeV in the detector, can only be obtained by the introduction of an attenuator between the preamplifier and the amplifier. At an equivalent gain of 1, the resolution will be 670 keV ! Thus, the intrinsic noise of the amplifier must be reduced. A solution was found by a simplification of the filter-amplifier design with which very low noise integrated circuits can be used [16]. The negative amplifier pulse is

obtained through a bipolar shaper (1.5 μs CR-RLC) followed by a clamp circuit. This simple design presents other advantages. A pole zero cancellation of the preamplifier decay time (220 μs time constant) is not necessary since a rejection of $\approx 10^4$ is provided by the bipolar shaping. Due to the zero crossing timing properties, the total pulse width (≈3.1 μs) is practically independent of the amplitude and the integration in the ADC can be performed on the totality of the pulse. This is important as the jitter in the time references (a few tens of ns) does not allow an integration limited to a well defined part of the analog pulse.

Another important feature in energy measurements of heavy ions with silicon detectors is that of the ballistic deficit due to detector collection times which can reach 1 μs [1,15]. In classical chains based on pulse-height ADCs, the ballistic deficit (BD) is the loss of the amplifier signal amplitude due to the interplay between the preamplifier rise time which follows the detector collection times and the amplifier time constants. The relative ballistic deficit (RBD_{amp}) is the ratio of the amplitude loss for a finite collection time to the amplitude obtained for an instantaneous collection time. A relative ballistic deficit RBD_{cha} can be similary defined for charge encoding as the ratio of the results obtained for finite collection times and an instantaneous one. The calculated RBD_{amp} and RBD_{cha} obtained by a simulation of the INDRA amplifier with the PSpice program [16] are presented in Table 3. The preamplifier pulse shape observed with silicon detectors [1] can be approximated by an exponential variation with respect to time : $1 - \exp(-t / \theta)$. A linear rise time is also considered for a comparaison to the RBD_{amp} obtained with the standard CR-$(RC)^4$ shaping, a differentiator followed by four integration stages. These calculations show clearly that the ballistic deficit with the INDRA amplifier is more than five times smaller for charge encoding when compared to pulse height encoding. The low RBD_{cha} can be qualitatively understood as following : when the preamplifier rise time increases, the slight widening of the amplifier pulse width, due to the bipolar CR-RLC filtering, compensates the pulse height decrease. The calculations of the RBD_{amp} for the CR-$(RC)^4$ amplifier were performed with the analytical formula of Loo, Goulding and Gao [17] which relies on the Baldinger and Franzen approach [18]. The relative ballistic deficit is expressed by $RBD_{amp} = (1 / 24.N).(T / \tau)^2$ where N is the filter order, T the total input rise time considered as linear and τ the filter time constant. We considered the fourth order filter (N=4) and two time constants, τ = 1 μs and τ = 0.25 μs. The first one is the standard value used in spectroscopy amplifier, while the second one corresponds to the same 1 μs peaking time of the INDRA amplifier. For the low value of τ, we also performed a simulation as the analytical formula overestimates the RBD_{amp} for the large rise times. The data show that a short time constant which could increase the dynamic range in the associated peak sensing ADC, is not compatible with the relatively large collection times of the silicon detectors. The most important result lies in the comparaison of the RBD_{cha} obtained with the INDRA chain to the RBD_{amp} of the standard CR-$(RC)^4$ amplifier set with τ = 1 μs. Similar ballistic deficits are obtained, but the shape of the amplifier output pulses are very different. The CR-$(RC)^4$ amplifier provides pulses

of 4 μs peaking time and an overall pulse width which exceeds 15 μs. The INDRA amplifier delivers pulses which have quasi constant and short widths : 3.1 μs to 3.7 μs for instantaneous and 1.2 μs rise times respectively. This last feature is very important for charge encoding.

4.3. Consequences on the detector time references

In order to allow quite a large jitter in detector time references, a 330 ns delay line has been placed in the output circuit of the amplifier. Therefore, the most important timing feature is to fire a discriminator on a large dynamic range. If we consider a classical timing system composed of a fast amplifier and a constant fraction discriminator, the dynamic range is usually limited to few hundreds to one. The limitation comes from the discriminator for which the maximum input voltage, generally limited to 5 V, has to be compared to the minimum effective threshold. This depends upon factors such as the input signal rise time, the fraction and the delay line of the discriminator. In order to increase the dynamic range, a specific timing amplifier has been developed. The main features are : a fixed voltage gain of 8, a CR-RC filtering of 50 ns integration and 300 ns differentiation times and a limit of 5 V for the maximum output voltage [16]. If we consider the previous example of a silicon detector preamplifier which gives a signal of 1 mV/MeV at the amplifier input, the 5 V saturation corresponds to an energy of 625 MeV and, for higher energies, a signal with a flat top at 5 V is delivered. This saturation mode allows the discriminator to fire up to the maximum energy of 4 GeV while also preserving a low energy threshold. In fact, the situation is a little bit more complex if we consider the large rise time variations due to the detector. Experimental results with the 300 μm thick silicon detectors have shown that a 100 % efficiency timing reference within 25 ns can be obtained above a threshold of a few MeV. In order to decrease this threshold one can consider the telescopic arrangement of the detectors. On forward angles ($3°<\theta<45°$), the 300 μm thick silicon detectors are followed by CsI(Tl) scintillators and a low energy loss in the first ones generally corresponds to a high energy loss in the second ones. By starting the charge integration gate of the ADC on a logical OR built on the two time references of the corresponding silicon and CsI(Tl) detectors, one obtains a very low threshold for the particles which cross the silicon detector. As protons can lose less than 1 MeV and as the electronics are set to collect up to 4 GeV, a dynamic range of more than 4000 to 1 is achieved. This method is also applied to the ionization chamber electronics for which the OR circuit is built on the time references provided by the ionization chamber discriminator and the four discriminators corresponding to the four pads of the associated silicon detector. At backwards angles ($45°<\theta<176°$), where there is no silicon detector, the OR circuit makes use of the CsI(Tl) discriminators instead of those of the silicon detectors. As shown in Ref. [1], the energy threshold thus obtained is low enough to detect He nucleus with the ionization chambers. This

corresponds to energy measurements as low as a 100 keV with a chain set up to a maximum energy of 200 MeV.

4.4. Description of the electronic modules

Fig. 9 presents a general view of the electronics associated with the 96 ionization chambers and the 196 silicon detectors. The preamplifier signal is sent to slow and fast amplifiers which are housed in the same 8 input CAMAC module. The energy measurement is achieved by double charge encoding in ADCs implemented in a 32 input VXIbus module. The fast output of the amplifier is fed to a constant fraction discriminator (48 input VXIbus module) which delivers a time reference signal to the "Trigger and Time-marker" system. As explained previously, the individual opening of the charge integrators in the ADC modules is a logical combination (performed in the trigger system) of different detector time references. For the total number of 292 channels, we need 37 amplifier modules, 7 discriminator modules and 10 ADC modules. The VXIbus spare channels and another amplifier module are used in the electronic chains of the PIN diodes which control the stability of the laser system associated with the scintillators [1]. In order to control the stability of the electronics, 8 output CAMAC pulse generators were also developed. There is one generator output for each ionization chamber, calibration telescope and PIN diodes, i.e. 120 generator channels in total. Each 300 μm silicon wafer shares the same generator signal, thus leading to 48 generator channels. Therefore, the total number of CAMAC generator modules is 21. The electronics is very concentrated ; only 3 CAMAC crates and one and a half VXIbus crates are necessary to house it. For the high voltage bias of the detectors, we use two SY403 crates of CAEN [6] equipped with the following boards : five negative 600 V boards for the 48 silicon wafers of 300 μm thickness and the 5 ionization chamber arrays, one positive 60 V board for the 8 silicon detectors of 80 μm thickness and one positive 600 V board for the 8 Si(Li) detectors. Fig. 9 shows, for one detector channel, the connections which are implemented on the module front pannels. All the other connections are made through the Slot 0 modules and the backplanes of the VXIbus crates.

Let us now present the four electronic modules which constitute the ionization chamber and silicon detector chain.

4.4.1. The octal CAMAC pulse generator

Fig. 10 shows a block diagram of the programmable pulse generator packaged in a #1 CAMAC module. The NIM input "Synchro." signal which triggers the generator is shaped to a width of 6 μs and limited to a maximum frequency of 100 Hz. The DC reference voltage is set to a value V_0 between - 5 V and + 5 V by a 16-bit DAC. When a synchronisation signal

occurs, V_0 is switched during 6 μs on the capacitance C_0 = 820 pF and so a pulse of amplitude V_0 is generated. The rise time given by the switch-on resistance of the commutator coupled to C_0 is around 50 ns. The decay time constant is ≈1 ms corresponding to the discharge of C_0 in the resistor R_0 = 1.2 MΩ. When the analog switch goes off, a slight signal (< 10 mV) appears. The 6 μs duration was chosen as it is larger than the charge integration gate (4 μs) of the ADC and smaller than the dead time of the discriminator fixed at 8 μs. Under CAMAC control, the rise time can be increased to 200 ns or 800 ns by the selection of the capacitances C_1 or C_2 of the integrator A_1. The pulse is distributed to the 8 outputs through amplifiers of gain 2 and buffered circuits. Eight relays allow a CAMAC software inhibit of each channel. The pulse amplitude is the same to within 1% on the 8 low impedance outputs and can be adjusted from - 10 V to + 10 V by steps of 0.3 mV. The integral non-linearity is better than 10 mV on 10 V. In the fabrication, particular care has been taken in the implementation of the capacitance and relay components. The fast, high linearity and high input FET impedance integrated circuits AD843 from Analog Devices are used for the DC reference voltage output and the amplifiers A_0 and A_1. They are also used for the amplifier A_S, in conjunction with the LH0043C buffered circuit.

4.4.2. The octal CAMAC amplifier

This #1 CAMAC module contains 8 channels of "fast" amplification for timing and 8 channels of "slow" amplification for energy measurements with charge ADCs. A detailed description with noise calculations is presented in Ref. [16] and we give here an overview of the main characteristics. Fig. 11 shows a block diagram of the energy channel filter-amplifier. The shaping network configuration, CR-RLC with time constants of 1.5 μs, is obtained through a passive input high pass filter (C_0 = 1.5 nF and R_0 = 1kΩ) followed by an $R_fL_fC_f$ band pass filter (R_f = 287 Ω, L_f = 220 μH, C_f = 10 nF) which gives a bipolar pulse. This filtering configuration has the main advantage of requiring only one operational amplifier A_1 for which a very low voltage noise integrated circuit, such as the AD844 from Analog Devices, can be chosen. For a unitary gain, the filter attenuation is 0.45 and that corresponds to a maximum amplitude of ≈2.25 V for an input amplitude of 5 V. Under CAMAC control, the true voltage gain can take 8 different values from 0.45 to 4.7 by multiplicative steps of 1.4. This function is obtained by the commutation of relays associated with the resistors R_{a1}, R_{a2} and R_{a3}. The amplifier A2 and the transistors T1 and T2 constitute a clamp circuit which limits the output pulse to the negative part and gives a current output signal. A 330 ns delay line is added at the output in order to encompass the totality of the linear pulse within the charge integration gate. The maximum output current is 60 mA and must not exceed 40 mA for a linear response. With the pulse shape provided by the amplifier (1.5 μs rise time and 3.1 μs total width), this corresponds to a maximum charge for a linear response of ≈80 nC. The silicon detector

preamplifier provides pulses of 1mV/MeV amplitude on the 50 Ω amplifier input impedance. Under these conditions, the amplifier's intrinsic resolution is 70 keV (fwhm) at the 0.45 minimum gain with a 4 μs charge encoding gate [16]. During the experiments and depending on the detectors, a resolution of 100 keV to 200 keV was obtained. The degradation of the resolution can be attributed to background noise of a very low level which cannot be seen on an oscilloscope as a 100 keV variation corresponds to a voltage step of less than 20 μV during the 4 μs opening of the ADC gate.

The main characteristics of the fast amplifier channel have been underlined in section 4.3 and are detailed in Ref. [16]. One of the difficulties in the electronic design came from the saturation mode chosen to ensure a timing with a high dynamic range. The solution was found in a fast biased line restorer which gives restitution times not exceeding 20 μs after saturation. Moreover, the polarity of the output signal is always negative whatever the polarity of the input signal is, and so multiple firing of the discriminator is avoided.

4.4.3. The 48-channel VXIbus discriminator

A photograph of this module is shown in Fig. 12. It represents a typical example of the VXIbus modules produced for the INDRA project. On the printed circuit motherboard two parts can be distinguished. On the forward part, the analog circuitry for each channel is implemented on a daughter board which is vertically plugged in the motherboard and can be easily changed. These daughter boards are multilayer PCB with SMT (Surface Mounted Technology) components on both sides. A high density analog circuit implementation is thus achieved with a very good separation between channels. A very low cross-talk can be preserved if attention is paid in the manufacture of the PC motherboard. As for example, in this 48-channel discriminator module, a 12 layer design of the PCB allows one to work with 40 ns rise time signals at 2mV thresholds without firing on a 5 V amplitude signal sent on an adjacent channel. The second part of the module, close to the three VXIbus connectors, is dedicated to the logic functions. In order to achieve a high density and versatility in the realisation of these functions, we used CMOS field-programmable gate arrays provided by the Xilinx Company [19] such as the XC 3042 and XC 3064 Logical Cell Arrays (LCA). The LCA structure consists of a perimeter of programmable Input Output Blocks (IOB), a core of configurable Logic Blocks (CLB) and their interconnection resources. Table 4 summarizes the main features of two LCA circuits. The CLB and IOB functions and their interconnections are controlled by a configuration program which is loaded automatically, on the power-up, from a serial PROM. In all the INDRA modules, the VXIbus interface is made by an XC 3064 which runs the same functions. A variable number of other LCAs (one XC3042 and one XC3064 in the discriminator module) are dedicated to the command of specific functions .

Fig. 13 shows a block diagram of the VXIbus discriminator module. Each of the 48 daughter boards contains a complete constant fraction discriminator (CFD) circuit and a delay and gate generator. The CFD shaping delay is 55 ns and an auto walk adjustement cancels the DC offsets and low frequency noise. An internal 8 μs dead time avoids multiple firing within the amplifier restitution times. The delay and the width of the output logic pulse are determined by two voltage comparators working on a linear ramp fired by the CFD. The following characteristics are remote controlled :

- thresholds, individually, from 0 to 255 mV in 1 mV steps
- output delays (non including the shaping times), individually, from 15 to 270 ns in 1 ns steps
- output widths, in groups of 8 channels, from 10 to 265 ns in 1 ns steps
- channel enabling and disabling, individually

On each channel, the analog input can be sent on any one of the 2 analog visualization lines through remote controlled analog multiplexers. Logic multiplexers ensure the same function for the logic output which can be sent on the 2 logic visualisation lines. This allows to check and compare the signals on an oscilloscope without dismounting the connector cables as discussed in section 3. All the analog values generated by the DACs, as well as the power voltages inside the module, can be controlled by the VME through the "voltage measurement" line and the associated ADC in the Slot 0 module.

4.4.4. The 32-channel VXIbus charge ADC

Fig 14 presents a block diagram of this 32-channel module which is described in detail in Ref. [10]. As discussed in section 4.2, the analog to digital conversion is achieved by a double encoding : two charge integrators with gains in the ratio 1:16 and two multiplexed 12 bits convertors. The "low gain" data are obtained on the full dynamic range and the "high gain" ones are provided for low energies only (corresponding to 1/16 of the full dynamic range). The two charge integrators for each channel are implemented on one SMT daughter board. The pulse from the amplifier is split into two equal currents which are integrated over capacities of 8700 pF and 540 pF. These values correspond respectively to dynamic ranges of ≈32 nC for the low gain and ≈2 nC for the high gain. Due to the 0.5 pC resolution needed on the high gain, particular care has been taken in the design of the ground and DC references. For example, the voltage drift of the input virtual ground is held below a value equivalent to 0.1pC/°C by a low frequency closed loop circuit [10]. Each dual integrator is associated with a logic gate SMT daughter board which includes the individual firing and validation of channels required by the "asynchronous mode" of the INDRA working logic. On this logic daughter board, the individual gate (T_i), validation point (VP_i) and reset (R_i) signals are generated. They can be adjusted by software commands through VXIbus and DACs. The standard settings used are

4 μs for T_i and 1 μs for VP_i. When an event is accepted by the trigger, only the channels having their VP_i in the trigger "validation gate" are processed in the two parallel chains of AD conversion. Each chain comprises four parallel connected 8 input analog multiplexers (MX818 from Datel) and one analog to digital converter of a 12 bit resolution and a 350ns conversion time (ADC530 from Datel). The multiplexers have a 800 ns settling time down to 10^{-4}. The ADC has an intrinsic 80% differential non linearity and is used in conjunction with a sliding scale circuit which reduces the differential linearity error to 1%. In order to avoid perturbations during the analog to digital conversion, the two conversions are made sequentially in the ADCs. This leads to a total conversion time of 2 μs for the two ranges of one input channel validated by the trigger through the "validation gate" and "start coding" signals. The data are stored in a R.A.M. memory working in the same way as a F.I.F.O : the 12-bit data and their corresponding 14-bit labels are read following the D32 mode of the VME until there is nothing more to be read in the module. The module logic is mainly constructed of LCA circuits which can be grouped into two functions : the VME interface (one XC3064 and one XC3042) and the control and sequence block (four XC3042s) which assumes the logic functions specifically related to this module. However, in order to avoid important time dispersions, the interface with the VXIbus timing signals, such as the "trigger bus", uses ECL technology. Some functions which are important in controlling the operation of the module are not presented in Fig 14. The pedestal of the channels can be adjusted by sending a DC current to the integrators. A local test mode makes use of a current generator which is fired when the "ADC test" signal is generated by the trigger. The following characteristics of the module are remote controlled :

- channel enabling and disabling, individually
- gate widths, from 1 μs to 11 μs, defined on 12 bits
- delays of the validation point, from 0.3 μs to 1.7 μs, defined on 12 bits
- pedestals, negative or positive, defined on 12 bits
- amplitudes of the test generators, defined on 12 bits

The main logical signals of each channel (integration gate, validation point, coding cycle...) can be sent on the two logic lines of the visualization bus. On the "gate control" line of this bus, one can see the validation point added to the validation gate sent by the trigger. As this corresponds to what occurs inside the module for each channel, this allows a precise adjustment of the coincidence functions. In fact, controls during the experiments show that the same value of the validation point delay can be used for the same family of detectors. This is due to the good reproductibility of the electronics and to the attention paid in the design of the timing circuits.

5. Compact modules for scintillator signal processing

The 324 CsI(Tl) detectors constitute the outer layer of the INDRA detector and no fast or individual logic information from the other detectors has to be considered. It was therefore decided that a VXIbus module containing a maximum number of channels with all the electronic functions should be designed [20]. The connections are thus reduced to one analog input and one logic output per channel. The other connections are general ones (VME bus, trigger bus, visualization bus, etc) and come through the VXIbus backplane. Fig. 15 shows a photograph of the "CsI module" in which the complete electronics for 24 channels has been implemented. As for the other VXIbus modules, the logic functions are assumed by LCA circuits located close to the bus connectors. The analog circuitry for each channel is implemented on 4 daughter boards, each having a surface of 40 x 18 mm^2. Such a high density is obtained mainly through the use of SMT components on both sides of the daughter boards. Fig. 16 presents for one channel, a block diagram of this circuitry. The CsI(Tl) signal processing needs the generation of a fast time reference which is sent to the trigger and two integrations, one in a fast gate (400 ns) and the other in a delayed slow gate (1.5 μs width and 1.6 μs delay). The photomultiplier signal arrives in the first daughter board (DB 1) where it is split into two channels. On one channel the signal is delayed by 55 ns and sent to the DB 2 daughter board which contains the two integrators. On the other channel, the signal is amplified by a factor of 3 and sent to the discriminator (DB 3 daughter board). The last daughter board (DB 4) contains the gate and delay generators which are fired by the discriminator and provide the fast and slow gates as well as the validation point of the channel triggering logic. The DB 1 daughter board also incorporates a test pulse generator which delivers particle-like signals to the input of the circuit. The inset in Fig. 16 shows a block diagram of the dual integrator. Due to the specifics of the fast and slow gates, which do not overlap, it was possible to simplify the electronic design. The common base input configuration (transistor T_0 and resistor R_0) ensures a well defined input impedance which is necessary for matching with the 50 Ω impedance of the DB 1 delay line. Depending on the logic signals (FG fast gate, SG slow gate or "no gate"), the input current signal flows into only one of the transistors T_1, T_2 or T_3. Thereafter, the current is integrated in the C_1 capacitor during the fast gate and in the C_2 capacitor during the slow gate, while it flows into the T_3 transistor when the two gates are inactive. A pedestal current of 50 μA is added to the signal in the input circuit in order to obtain a good linearity for low amplitude signals. The analog to digital conversions of the 24 channels are performed by two multiplexed ADCs implemented on the motherboard, one for the fast signal component and the other for the slow one. As for the other detectors, the CsI module follows the asynchronous mode of triggering and only the channels having their validation point in coincidence with the validation gate are converted. In order to save place on the motherboard, small-size audio converters (Crystal CS5101) without sliding scale corrections are used. Only 12 bits of these 16-bit converters are kept and a satisfactory differential nonlinearity of 3% is thus obtained. The coding time

takes about 10 μs. The main electronic characteristics of this module are given in Ref. [20]. The following parameters are remote controlled :

- channel enabling and disabling, individually
- discriminator thresholds, individually, from 0 to 128 mV in 0.5 mV steps
- discriminator output delays (non including the shaping times), in groups of 8 channels, from 15 to 270 ns in 1 ns steps
- discriminator output widths, common , from 10 to 265 ns in 1 ns steps
- fast gate widths, common, from 50 ns to 1.1 μs, defined on 8 bits
- slow gates : the start and the stop of the gate signals are adjustable from 100 ns to 3.8 μs, values are common to all channels and defined on 8 bits
  (the fast gate and the slow gate must not overlap)
- delays of the validation point, common, from 15 ns to 1.1 μs, defined on 8 bits
- test generator : channel enabling and disabling, individually
- amplitudes of the test generators, defined on 12 bits

As the module contains all the functions, it is important to be able to visualize the internal analog and logic signals. This is assumed by multiplexers which, under software control, send the signals to the crate backplane and then, through the Slot 0 module, to one of the five lines of the INDRA visualization bus. The signals which can be visualized are : the analog inputs, the fast integrator analog outputs, the discriminator outputs, the fast gates, the slow gates and the validation points added to the validation gate.

The CsI module was adapted to the characteristics of the CsI(Tl) and cannot be used for the NE102/NE115 phoswich detectors. The main reason is due to faster rise and decay times of the NE102 plastic scintillator, so that the integrations must be performed in a different way. In this case a short gate (30 ns) is required, during which the fast plastic light is measured, and a larger gate (800 ns) for the integration of the entire signal. The modifications needed led us to design a specific 16-channel module which is presented in Ref. [21]. In what concerns the parameter setup and the signal visualizations, this module works like the CsI module and the operating software system is quite similar for the two modules.

6. The trigger and time references for detectors

The trigger system selects the events, delivers the logic signals to the ADC modules and assumes the conversation with the data acquisition system. The large number of detectors rule out the possibility of event selections in which all the discriminators would be considered individually. The requirements of physics and the axial symmetry of INDRA led us to consider event selections based on ring dependent multiplicity levels. The ionization chamber logic signals are not actually used and thus INDRA can be considered as an arrangement of 336 detection cells within 17 rings [1]. Each

detection cell delivers a 0.3 mA signal per hit which are added to form 17 multiplicity current signals as shown in Fig. 17. For ring 1, it is simply a 12 input circuit receiving the discriminator signals associated with the 12 phoswich detectors. Due to the arrangement of detectors in telescopes, the situation is more complex for the other rings. In the forward rings (2 to 9), the introduction of OR circuits allows the creation of only one individual multiplicity current when the particle hits one or two detectors of the same Silicon-CsI(Tl) telescope. In the backward rings (10 to 17), only the CsI(Tl) detectors are considered, except for the cells (one per ring) which comprise the calibration telescopes for which OR circuits are also needed. In each ring, three identical multiplicity currents are available on three LEMO 00 connectors. These multiplicity and OR functions do not need software access and they are implemented in NIM modules which belong to a system called the "grouper". Not only does the grouper system reduces the number of signals to consider in the event selection, but it also assumes other logic functions. As shown in Fig. 17, the OR circuits deliver signals which fire the ADC gate of the silicon detectors (see section 4.3). Similarly OR functions ensure the firing of the ADC gates of the ionization chambers. For each ionization chamber cell, a logic OR is built between the ionization chamber discriminator and the discriminators of the detectors placed just behind, these are silicon detectors for rings 2 to 9 and CsI(Tl) for rings 10 to 17. The grouper also aids in reducing the number of channels which are controlled by the scalers. For example, one scaler is used for the four channels coming from the same silicon wafer. Therefore, only 16 VME scaler modules of 16 channels each are needed, whilst an individual control of each detector discriminator would have led to more than 40 scaler modules. The grouper is actually composed of 30 NIM modules of four different kinds. The functions performed can be varied or other functions added simply by changing the connections between the modules. For instance, multiplicity currents could be generated from the ionization chamber discriminators and used to select events for which a high energy deposit is required in the first layer of gaseous detectors.

In order to have the option of easily changing the trigger configuration, the event selection itself is performed in a VXIbus module called the "selector". Fig. 18 presents a simplified block diagram of the triggering inputs which can be selected under software commands. Two modes can be distinguished : the "physics mode" in which the system is triggered by one of the A to H inputs and the "test mode" which ensures the generation of the synchronization signals for the laser system associated with the scintillator detectors [1], the CAMAC pulse generators and the test generators of the ADC modules. During an experiment, the three synchronization signals which are denoted L.T. for the laser, C.T. for the CAMAC generators and A.T. for the ADC generators, are regularly generated by the selector following the time sharing of the beams delivered by GANIL, i.e., in a typical arrangement, during 10% of the time cycle when the beam is directed to another experimental area. Under software command, one can choose different test configurations which are automatically and successively selected at each beam cycle. Four test configurations are available : L.T. alone, C.T. alone, A.T. alone and L.T. and C.T. simultaneously. The frequencies (Fr) of the C.T. and A.T. signals can be selected from 40 Hz to ≈0.005 Hz on 14 values : Fr (in Hz) = $160 / 2^n$ with n = 2 to

15. In order to obtain the best stability on the laser system, its working frequency must be fixed at 10 Hz [1] and instead of a frequency, one can select the L.T. signal every few cycles, more precisely L.T. is generated during only 1 per N cycles with N = 1 to 15. Thus, the "test mode" allows to check the stability of the electronics during the experiments with a selected number of events and without beam on the target .

The triggering in the "physics mode" relies on the inputs A to H. The first three (A to C) run the same functions and perform a multiplicity selection of the events. Fig. 19 presents a block diagram of one of these inputs. In order to obtain fast responses, the multiplicity logic works in the current mode. The current signals of 0.3 mA per hit generated by the grouper NIM modules arrive on 8 inputs A1 to A8. The common base configuration of these inputs ensures a fast response together with a well-defined input impedance of 50 Ω. After crossing the analog switches S1 to S8, which allow to open or close the corresponding channels, the input currents are added on the common line Li. The current mirror, composed of transistors T_9 and T_{10}, transfers this total pulse current (It) to the line Ld where it is added to a current Id generated by a DAC. The current Id determines the multiplicity threshold. When "It" is greater than "Id", the discriminator fires and a logical signal is created. Therefore, whatever the chosen multiplicity is, the discriminator always works at the same low level threshold. However, it is important to carefully adjust the current Id. This is carried out by the logic selection block in the following way. When a configuration and a multiplicity value are selected, the selector module generates a "discriminator inhibit" signal which disables all the detector discriminators. Then, through a counter progression and a comparison with the comparator circuit response, the logic block searches for the true zero level. The corresponding numerical value is added to the selected multiplicity value to create, via the DAC, the current Id. This method ensures that the multiplicity levels do not depend of the residual current which could vary with the number of NIM grouper modules considered. The standard INDRA triggering configuration makes use of the A selector input. The 17 individual multiplicity currents generated in the grouper modules are added to form 8 independent signals corresponding to rings 1 alone, 2 and 3, 4 and 5, 6 and 7, 8 and 9, 10 and 11, 12 and 13 and finally 14 to 17. The addition is simply performed by connecting on the same coaxial cable the corresponding grouper module outputs. We have checked that despite the relatively high number of primary logic channels, this multiplicity selection is very clean regardless of the detector hit. The two selector inputs, B and C, which are not actually used, will allow the incorporation of future triggering configurations such as, for example, multiplicity selections based on the ionization chamber discriminators. The D and E inputs are devoted to calibrations at backward angles. On the inputs D_1 to D_8, it is possible to select the 8 calibration telescopes placed in the rings 10 to 17, whilst on the inputs E_1 to E_8, all the detectors except the ionization chambers of the corresponding ring can be selected. The last three inputs can receive NIM logic signals and are thus open to future developments in which other detectors could be added to the INDRA ones. The logic signals (L_A to L_H) corresponding to the eight inputs (A to H) are then individually allowed, or not, to trigger the system. A coincidence function can also be performed between these 8 inputs but for

simplicity it has not been shown in Fig. 18. The first signal to arrive fires a coincidence gate of duration T during which the 8 input signals, delayed by a value T/2, are memorized. A set of configurations can be pre-selected amongst the 255 possibilities given by the 8 memorized signals. All the settings of the selector module are under software control. The triggering configurations are selected by switches and level multiplicity adjustments. The timing (delays, gate and signal widths) is performed through numerical counters working on the VXIbus 100 MHz clock. Therefore, all the time settings rely on binary registers and can be adjusted in steps of 10 ns.

The trigger must also ensure the conversation with the data acquisition system and the VXIbus encoding modules. These functions are implemented in a specific VXIbus module called the "correlator". The splitting into two modules preserves future evolutions of the data acquisition system in which only the correlator module would be changed.

In INDRA, the identification of particles is based only on energy losses and so precise timing measurements are not necessary. However, in order to evaluate random coincidences, we need an estimation of the detectors' timing. Typical times between beam pulses at GANIL range from 80 ns to 120 ns. A 10 ns time resolution was therefore considered sufficient. The time measurement is performed by "time marker" VXIbus modules which make use of the 100 MHz clock available in the VXIbus standard. A time marker is a 96 channel module which uses the principles of the "asynchronous mode". Each channel is associated with a counter which is started by the output of the corresponding discriminator and which will stop and clear itself on reaching the end of the counter scale. This allows one to follow the activity of each detector on software definable time scales of 1.25, 2.5, 5 or 10 μs. Once a valid event has triggered the "selector", all counting scalers are stopped by the "validation gate" signal, inhibited and presented for readout. The time markers allow not only an evaluation of random coincidences but also of the instantaneous efficiency of the multidetector since the measurements could be made on a longer timescale before the trigger validation. We use seven time marker modules in order to get individual time measurements of the 628 detectors which compose INDRA. The selector, the correlator and the 7 time-marker modules are housed in the same VXIbus crate and composed together with the 30 grouper NIM modules in an ensemble called "the INDRA trigger".

7. Data acquisition and software controls

The INDRA data acquisition is based on the standard GANIL acquisition system [2]. However, some facilities such as the implementation of VXIbus or the full remote control of the electronics had to be added to satisfy the INDRA requirements. The standard GANIL acquisition system is implemented within a distributed computing environment, based on a cluster of four VAX 6000 working under VMS. In each experimental area, a front end multiprocessor VME crate is dedicated to real-time data acquisition, to event building and

filtering. The VME front end is a modular system which is easily configurable for a variety of experimental needs. It can be used either in stand-alone mode for electronic debugging or connected to a VAX for data storage and control. The experiment configuration is described in text files on the VAX which are compiled to generate object files loaded in the VME crate. Graphical visualization is performed on VAX workstations (VS4000/60 or /90) distributed on the local area network using a locally developped software based on XWindow/MOTIF. During experiments, four VAX stations are dedicated to the INDRA data acquisition and controls.

7.1. The VME front-end

The configuration of the INDRA VME front end is shown in Fig. 20. The CAMAC interface consists of a CBD8110 board from the CES company connected to a VME processor called "READ" through the VSB bus. The access to the VXIbus crates is achieved by the VMV bus (see section 3 and Fig. 7). The interface is the VIC8250 board from CES connected to the "READ" CPU via VSB. The same CPU is used for CAMAC and VXIbus in order to have the possibility of reading CAMAC modules in data acquisition. Even if presently, there is no data coming from CAMAC modules during INDRA acquisition, future developments including commercially available CAMAC modules are still possible. Thus, data are read, via the VMV bus, by the dedicated acquisition processor ("READ") seen as a VXIbus interface by the FP boards (filtering processors). Events are queued in the double port memory of the processor. The same VMV bus is also used to access CAEN V260 scaler modules installed in a separate VME crate. In the standard GANIL acquisition, one to seven FP CPUs processing in parallel perform data collection from different interfaces, event building and filtering before sending event buffers to the VAX for storage and control via the optical data link. Each FP processor runs the same application program. At the present time, two FP processors are used in the INDRA configuration. The optical data link interface consists of a CPU board FIC8230 coupled with an optical data link board ODL8142 from CES, which is seen as a "black box" by the application programs. It is used only for event buffer transfers to the VAX. The "SURV" CPU, equipped with Ethernet interface, runs a TCP/IP server which acts as a gateway for all CPU boards in the crate. All commands from VAX are sent through Ethernet. The "CC" CPU has been added to command and control high voltages through the V288 CAEN module (VME interface to the serial CAENET bus) [6] and to get, through a JBUS connexion, informations on the experimental conditions : pressures in the reaction chamber and gaseous detectors, surrounding temperatures, target's high voltage bias, etc. All CPU boards, with the exception of the FIC8230, are MC68030 manufactured by the FORCE Computer Company. They have shared memory with the VME bus and they run PDOS or VMEPROM real time operating systems.

In order to satisfy INDRA requirements, new software packages had to be created. To perform remote controls, five dedicated servers (CAMAC, VXIbus, Scalers, High voltage, JBUS) were developed in the VME. They can reside in any CPU in the crate and receive orders from local or remote applications through the TCP/IP server running in the "SURV" processor. Except for the high voltage server, ASCII commands are directly interpreted by the servers. Thus, a common utility allows to send interactive commands to any of them. A VXIbus register based resource manager (RM) has been developed and runs in the VME crate. It initializes VXIbus configurations and creates a local data base. It uses a VXIbus board library which consists of text files containing board identifications and register descriptions (name, access rights, significant bits, initialization values, etc). The VXIbus server allows remote applications in order to access registers by name and to get any information on the current configuration. In addition, a subroutine library allows VME applications to access VXIbus modules. A surveyor running on the "CC" processor controls the high voltage status. An alarm process can display a status panel on a local terminal or information can be sent to a remote user application through the high voltage server. Due to the setup complexity and the large number of channels, exchanges with the server are in a binary format. The GANIL acquisition program running in the VME processor has been upgraded to accept VXIbus modules. Some interactive options allow the user to run the acquisition with several debugging levels. This has been very useful for the tuning of the electronic modules. The FP processors generate two kinds of buffers. In the standard GANIL acquisition, one of them dedicated to magnetic support storage contains variable length events and the other one, intended for the VAX control program, contains events of a fixed size equal to the total number of parameters of the experiment. For INDRA, a variable format has been implemented for control events and thus the control buffers contain only significant parameters.

7.2 The command and control software

All the electronics is located in the beam cave and is only accessible through software commands on VAX workstations. Four graphical software packages have been developed. Three of them are dedicated to the set up and to the control of parameter values and one to the selection of the signals to be visualized. The setting softwares have been separated into three interfaces corresponding to the "high voltage" (SY403 CAEN system), the "trigger" (VXIbus selector module) and the "electronics" ie. all the modules in CAMAC or VXIbus standards except for the selector.

Table 5 summarizes all the parameters which are controlled by the "electronics" software. The different values accessible have been presented together with the description of the modules in sections 4 and 5. Fig. 21 shows the graphical interface associated with this software package. It looks like a big array in which each cell represents a detection module. For example,

the cell located at the fifth column in the third line stands for the third detection module of ring number 5. The kind of detector (scintillator, ionization chamber, silicon detector) is selected by using the upper menu bar and the function (threshold, gain, delay, etc) is chosen in the corresponding pulldown menu. The values are given in commonly used units : mV for thresholds, ns for time settings. When a writing or reading order is given, by clicking on one of the four bottom pushbuttons, the program finds the relevant electronic module and channel. It converts the given value to the proper integer value and builds the basic order which will be sent through the ethernet network to the CPU located in the VME crate. The order is then executed and an acknowledge message is sent back to the command program which decodes it and alerts the user if something is going wrong. The user can save a configuration on a disk or read it from a disk. The graphical interface for high voltages was built following the same principles as well as the command of the signals to be visualized. The "trigger" interface is different from the other three. It shows a picture close to a simplified electronic block diagram of the selector module. Each register is represented by an editable text field (times, multiplicities) or by toggle buttons (channel connections). In order to simplify the usage, some registers are bound in specific windows without any reference to a real picture of the internal logic connections. As for example, in the case of the generators for which the user needs only to know the types of generators sent and their occurence. All the interfaces run on VAX workstations under VMS. The graphical standard used is XMOTIF. They are written in FORTRAN VMS language. The connections between the electronic modules and the physical channels are hidden to the user. They are described in a text file which can be easily modified by advanced users. This allows to modify links between the electronics and the detectors without modifying the command program. In the same way, all the functions and conversion factors of the electronic modules are described in editable text files.

7.3 The VAX acquisition

Due to the large number of spectra to be treated, one of the three VAX6310s has been upgraded to a VAX6510 with 128 Mbytes of memory. This large central memory allows the storage of all the control spectra which consist of 1800 one-dimensional (512 channels each) and 1400 two-dimensional (128 x 128 channels) histogramms. A new package of treatment routines has been developed in order to integrate the variable format of the control buffers provided by the VME front-end. The control spectra are displayed with the GANIL visualization program on VAX workstations [22]. However, the standard interface of this program would lead to many operations to display all the stored spectra. The possibility of customizing the application through a package of routines allowed us to build a graphical XMOTIF interface corresponding to the INDRA arrangement of detectors. The users only have to choose the ring and the kind of spectrum they are interested in by using pulldown menus.

The INDRA display program generates proper orders and sends them to the GANIL visualization program. This allows spectra to be displayed in a few clicks and it is thus possible to check all the spectra in roughly two hours.

7.4 Performances of the data acquisition

In order to estimate the performances required for the data acquisition rate, typical experiments were analysed. A very important constraint is the minimization of random coincidences. In relation to the ion accelerated and its energy, the beam pulses at GANIL are separated by 80 to 120 ns which leads to a mean of 10^7 beam bursts per second. If a maximum proportion of 10^{-4} random coincidences is accepted, the number of nuclear reactions must not exceed 1000 per second. Depending on the trigger considered, the number of events to be registered stretches from 100 to 500 counts per second, respectively for high and low multiplicity events. With a 20% dead time, the time of data acquisition must range between 400 µs and 2 ms for a low and a large number of registered parameters respectively.

The cycle time of data conversion and readout consists of :

1) Analog integration in parallel in all the ADCs and multiplexed A/D conversion in the VXIbus modules. The time of this operation is limited by the A/D conversion in the VXIbus board associated with the CsI(Tl) detectors and is equal to $10 + p \times 10$ (in µs) where p is the maximum number of hit detectors corresponding to the same 24 input VXIbus module.

2) VXI interrupt acknowledgment : 20 µs on average. The pull down time cycle is 40 µs.

3) Trigger (selector module) readout : 70 µs. In fact, this function contains also the connections to CAMAC data reading which are not actually used. An optimization of this part could lead to a reduction of 35 µs on this time.

4) Scanning of the 31 VXIbus boards : 90 µs.

5) Readout of the parameters : $n \times 2$ µs where n is the number of parameters.

6) Data acquisition end loop. At the end of the last parameter read out, all the electronic modules are liberated by the "general reset" signal. However, in order to prepare the system for the next event read out, a loop of 60 µs duration is generated. For an evaluation of the counting rate, the added average dead time is : $(5 - p) \times 10$ µs for $p < 5$ and 0 µs for $p \geq 5$, since the A/D conversion can operate when an event occurs during the 60 µs end loop.

Thus, the total time (triggering, conversion and readout) for an event can be expressed by :

$$T_{acq} \text{ (in µs)} = 190 + p \times 10 + n \times 2 + [(5 - p) \times 10 \text{ , for } p < 5]$$

This time is the overall acquisition one since the read events do not need an additionnal software treatment to eliminate parameters. A virtual pattern filtering is already made by the asynchronous mode in the ADCs. The data acquisition rate depends on the events considered.

For instance, a registered multiplicity of 20 particles leads to an average of 40 hit detectors for which 3 parameters (two energies, one time) have to be read and so, n = 120. Due to the repartition of the particles, p = 2, on average. Thus, for this typical example, T_{acq} = 480 μs and the acquisition rate is 415 events per second with a dead time of 20 %. With the same dead time and taking p equal to 12, a rate of 100 events per second could be reached for events of 845 parameters, i.e. a number of hit detectors which is greater than the maximum encountered with INDRA as it corresponds to 45% of the total number of detectors. Therefore, one can say that the acquisition rate is compatible with the type of events produced in INDRA. Moreover, this rate in the VME is not limited by the tracking in the data acquisition system. A parameter needs 4 bytes (16 bits of data and 16 bits of identification). The optical connection between VAX and VME is limited at 700 Kbytes/sec, that is about 730 events of 120 parameters per second, due to the two types of buffers (storage and control) to be sent to the VAX. The data from the storage buffer are recorded on IBM 3480 cartridges for which the storage speed is 1 Mbyte per second. Concerning the control, about 150 events per second can be treated by the control task in the VAX computer, which represents 35% of typical counting rates.

8. Summary and conclusion

The characteristics of the INDRA 4π detector led us to develop a specially dedicated electronics system which is entirely located in the beam cave. The 292 charge preamplifiers and the 336 low power consumption photomultiplier bases are implemented in the vacuum chamber. With the exception of the high voltage power supply system (8 CAEN model SY 403 crates), the scalers (16 modules CAEN V260), the VME processors and drivers and the 4 VXIbus controllers, all the other electronic modules were designed and constructed by the laboratories of the INDRA collaboration. The standards were chosen in relation to software access : NIM (3 crates, no access), CAMAC (3 crates, command only), VXIbus (4 D-size crates, commands and acquisition readout). All the electronics software accesses (commands and controls, data readout and buffer packaging) are centralized in a master VME crate. The NIM crates house the 30 modules which compose the grouper system which performs current multiplicity generations and non-programmable logic functions of the trigger. The CAMAC modules are the octal pulse generator (21 modules) and the octal amplifier (38 modules) associated with the ionization chambers, the silicon detectors and the PIN diodes which control the laser system. A VXIbus crate is dedicated to the trigger system and houses three different types of modules : the selector which assumes the event selection, the correlator for the link with the data acquisition and 7 time markers (96 channels each) which perform low resolution (±10 ns) timing measurements on all the detectors. The 3 other VXIbus crates contain the compact modules for scintillator signal processing (14 modules of 24 channels each for the CsI(Tl) and 1 module for the 12 phoswich detectors), the 7 constant fraction discriminator modules (48 channels

each) and the 10 charge ADC modules (32 channels, dual range per channel) which are associated with the ionization chambers, the silicon detectors and the PIN diodes. Numerous test runs were performed with the GANIL beam in 1992 during the last year of construction and detector assembly. They allowed us to progressively check all the electronic features in the experimental configuration. First experiments were performed in the spring of 1993 without any important problems in the functioning of the electronics.

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Figure captions.

Fig.1 Split view of the INDRA 4π detection array.

Fig.2 Principle of the transistorized photomultiplier base. The photomultiplier is represented on the right-hand side. The cathode current, I_k, is amplified from dynode D_1 until dynode D_8. The capacitors C_k to C_8 of the base serve as charge supplies. The capacitors C_6 to C_8 are replenished with the full bias current by means of switches SW_6 to SW_8. The inset shows a practical solution of the SW_7 and SW_8 switches (transistors T_7 and T_8).

Fig.3 Comparison between transistorized and RC photomultiplier bases. These computer simulations show the variation of the last dynode voltage (V_{D8}) and of the cathode-first dynode voltage ($V_{K\text{-}D1}$). In a transistorized photomultiplier base, the bias current I_b is used to fully replenish the capacitors C_6 to C_8. On the contrary, in a resistor-only (RC) base, the capacitors C_k to C_8 are replenished with only a fraction of the bias current I_b. The consequence is a lower counting rate with a higher current I_b in the second type of base.

Fig.4 Schematic diagram of the charge preamplifiers associated with (a) the ionization chambers and (b) the silicon detectors. The variations in preamplifier sensitivities are within $\pm$ 1%. In the former case the sensitivity is tuned by adjusting the printed circuit made capacitor C_r. In the latter case the precision is given by the choice of the C_r component.

Fig.5 (a) Schematic diagram of the connectors used on the vacuum chamber flange for the cable connections. On the left-hand side, the connector associated with the ionization chambers and the silicon detectors is presented. The right-hand side connector is used for the scintillators. (b) Technique used for the coaxial cable assembly on the connectors.

Fig.6 The INDRA vacuum chamber flange. Ten multipoint connectors (following the designs presented in Fig. 5) are implemented on a 160 mm diameter printed circuit. A silver filled epoxy glue ensures the ground connection for all the cable ground references to the reaction chamber.

Fig.7 Outlines of the electronic architecture. The data acquisition front end is a VME crate. The connection to other crates is achieved by driver cards and associated CPU. The distribution of the trigger signals is assumed by a "Trigger bus" connected to the control module (Slot 0) of the VXIbus crates. Remote visualizations of signals inside the VXIbus modules are available on the Slot 0 front pannels ("Visu.").

Fig.8 Principles of the "asynchronous mode" of triggering (see text).

Fig.9 General view of the electronics associated with the ionization chamber and silicon detectors.

Fig.10 Schematic diagram of the 8 output CAMAC pulse generator.

Fig.11 Schematic diagram of the slow amplifier used for energy measurements with the ionization chambers and silicon detectors. The bipolar shaping amplifier (C_0R_0-$R_fL_fC_f$) is followed by a clamp circuit which limits the output pulse to the negative part.

Fig.12 Photograph of the 48-channel VXIbus discriminator. The analog circuitry of each channel is implemented on a SMT daughter board plugged in the PC motherboard. In the backward part of the PCB, the logic functions and VXIbus interfaces are implemented.

Fig.13 Block diagram of the 48-channel VXIbus discriminator. The main connections to the VXIbus backplane and Slot 0 module are shown.

Fig.14 Block diagram of the 32-channel VXIbus charge ADC. The two integrators of one channel are implemented on one SMT daughter board. Another SMT daughter board ensures the local logic functions (gate, validation point and reset). Two multiplexed ADCs are used for the low and high gain conversions. The main general logic functions and the connections to the VXIbus backplane and Slot 0 module are shown.

Fig.15 Photograph of the CsI VXIbus module (D-size) which houses 24 channels. A total of 96 daughter boards of 4 different types are plugged into the motherboard and 6 LCA circuits ensure the logic functions and VXIbus interface.

Fig.16 Block diagram of the 4 daughter boards which compose the analog circuitry of one channel of the CsI VXIbus module. The inset shows the principle of the dual integrator (DB 2 daughter board) which works on the two non-overlaping fast (FG) and slow (SG) gates.

Fig.17 Principles of the multiplicity current generation in the NIM modules which compose the grouper system of the trigger.

Fig.18 Schematic diagram of the triggering principles in the selector module. Two modes can be distinguished and are automatically activated by the beam cycle signal. See text for a detailed description.

Fig.19 Schematic diagram of the multiplicity triggering channel of the selector module.

Fig.20 The VME front end crate of the data acquisition system.

Fig.21 View of one of the four graphical interfaces used to command and control INDRA. This interface is devoted to the parameter settings of all the CAMAC and VXIbus modules except for the trigger "selector". The accessible parameters are summarized in Table 5.

Table captions.

Table 1 Main characteristics of the charge preamplifiers associated with the ionization chambers and the 300 μm thick silicon detectors.

Table 2 VXIbus specifications and their application to INDRA (see text).

Table 3 Calculations of the relative ballistic deficit (RBD) for peak sensing (RBD_{amp}) and charge encoding (RBD_{cha}) with the INDRA amplifier for different input pulse rise times. Two preamplifier pulse shapes are considered at the input of the amplifier : (i) an exponential time variation of constant θ and (ii) a linear time variation. For comparison, the RBD_{amp} of a standard CR-$(RC)^4$ amplifier, calculated as in ref. [17], is given for the two filtering time constants τ = 1 μs and τ = 0.25 μs. The values in brackets are the results of a simulation.

Table 4 Main specifications of two LCA (Logic Cell Array) circuits from Xilinx [19].

Table 5 Parameters of the electronic modules which are software controlled through the interface presented in Fig. 21.

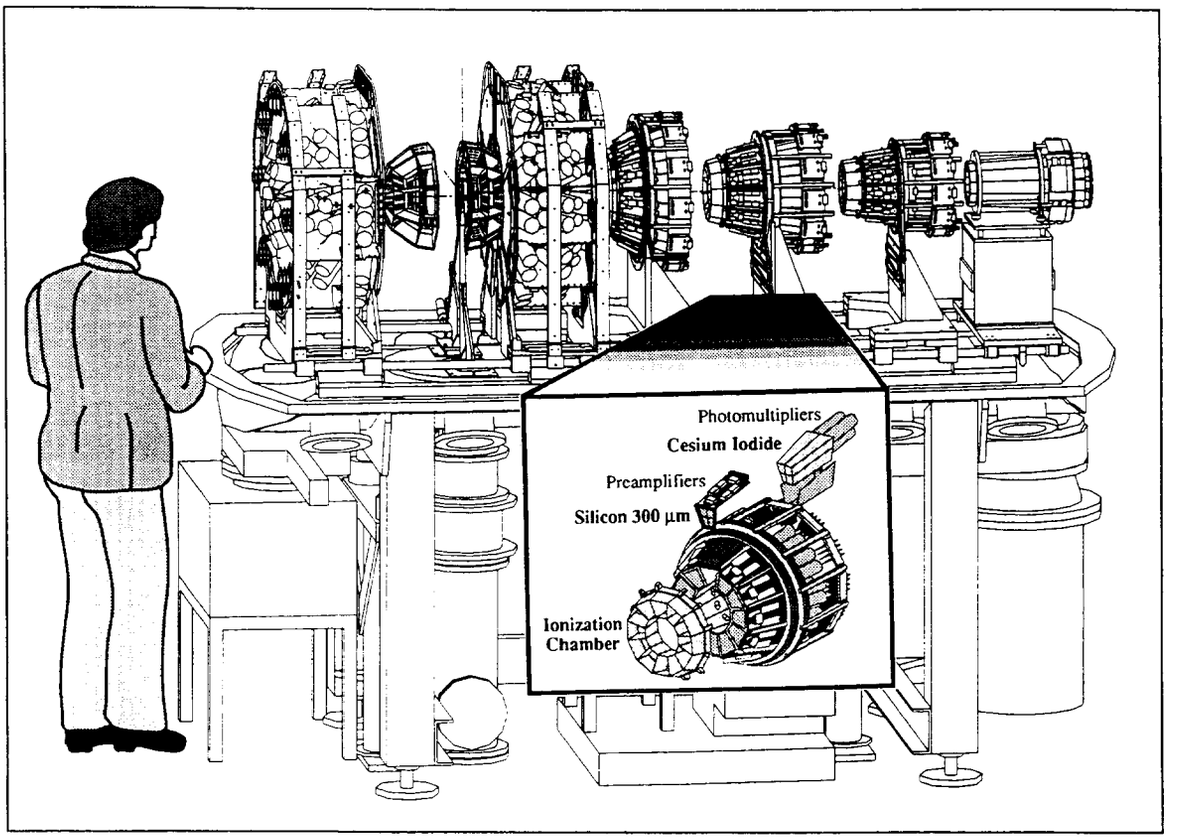

Photomultipliers
Cesium Iodide
Preamplifiers
Silicon 300 µm
Ionization Chamber

Figure 1

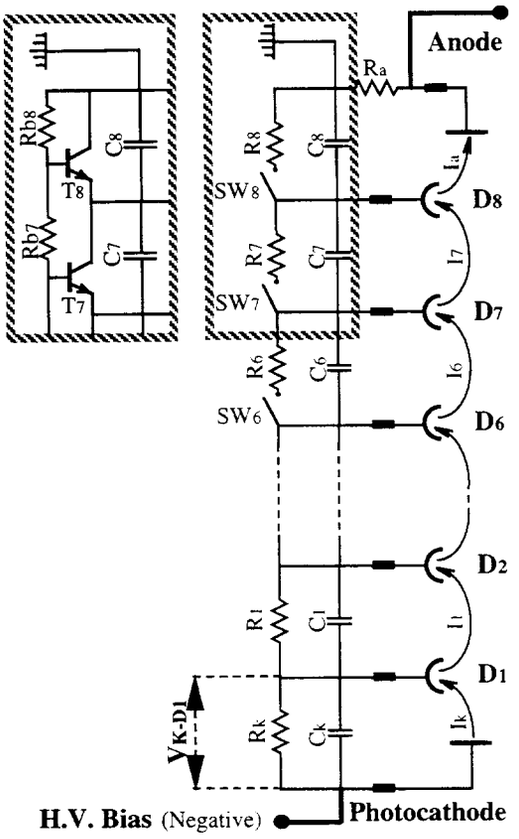


Figure 2

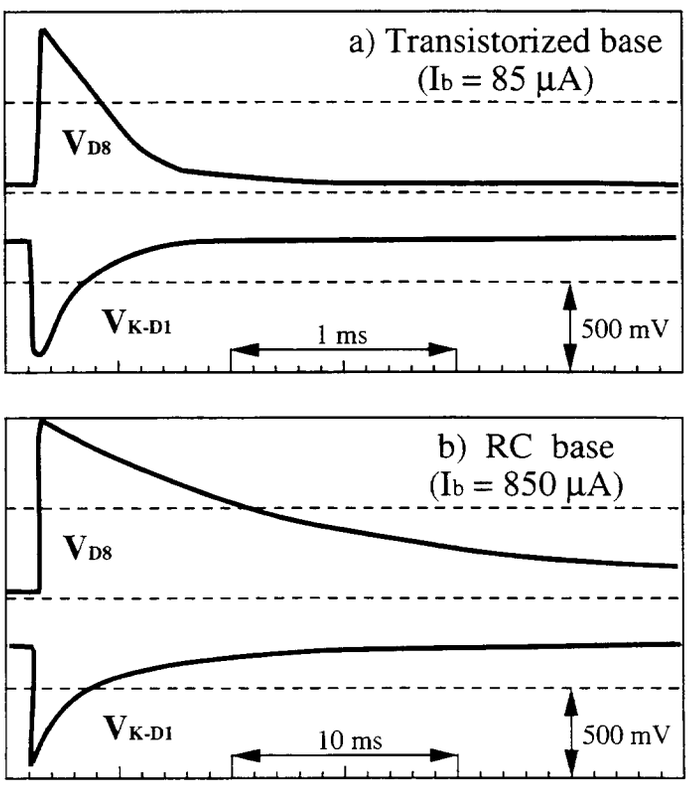
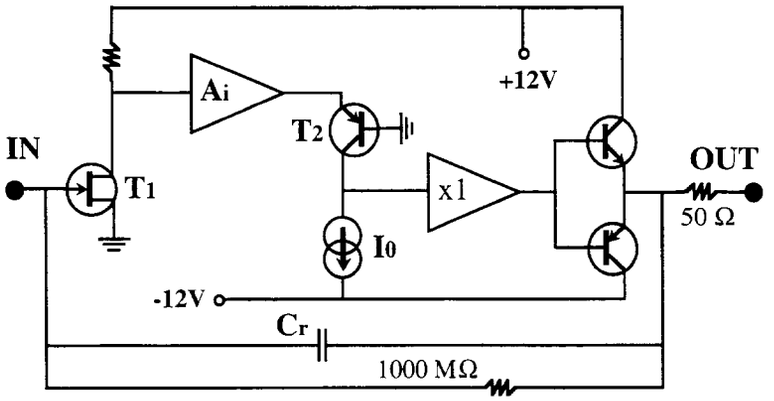


Figure 3

a) Ionization chamber



b) Silicon detector

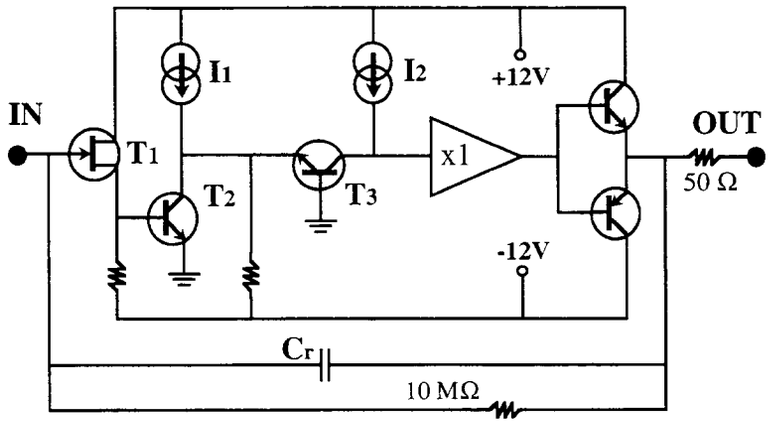


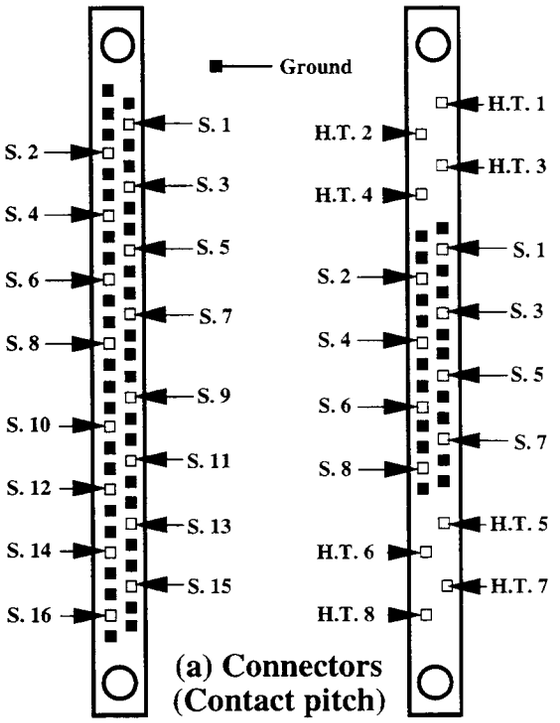
Figure 4

Characteristics	Ionization chamber preamplifier	Silicon detector (300 µm) preamplifier
Charge sensitivity (*)	4500 mV / pC	45 mV / pC
Energy sensitivity (*)	20 mV / MeV (for C3F8 gas)	2 mV / MeV
Maximum output amplitude (*) (linear response)	± 5 V	- 10 V
Decay time constant	220 µs	220 µs
Open-loop voltage gain (at 100 kHz frequency)	30 000	100 000
Equivalent noise charge (**) (r. m. s.)	260 e + 4.7 e/pF	470 e + 6 e/pF
Rise time	15 ns (without detector)	25 ns (with 200 pF detector)
Power consumption (at rest)	Maximum : 300 mW	Maximum : 300 mW

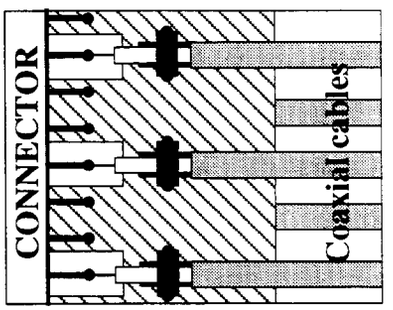
(*) on a 100 Ω output resistor. As the preamplifier output include a 50 Ω resistor, the values are divided by a factor 2 at the amplifier input (50 Ω impedance).

(**) for a standard filtering : CR-$(RC)^4$ amplifier of 1 µs time constants.

Table 1



(a) Connectors (Contact pitch)



(b) Cable connections

Figure 5

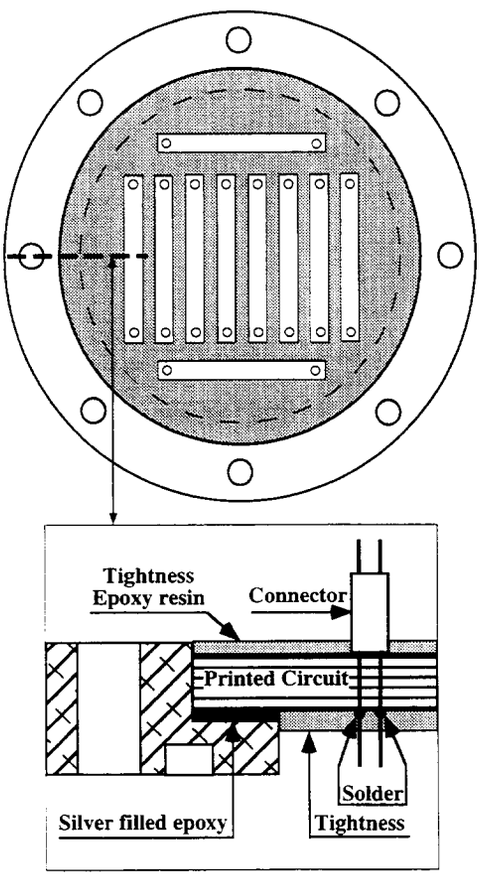


Figure 6

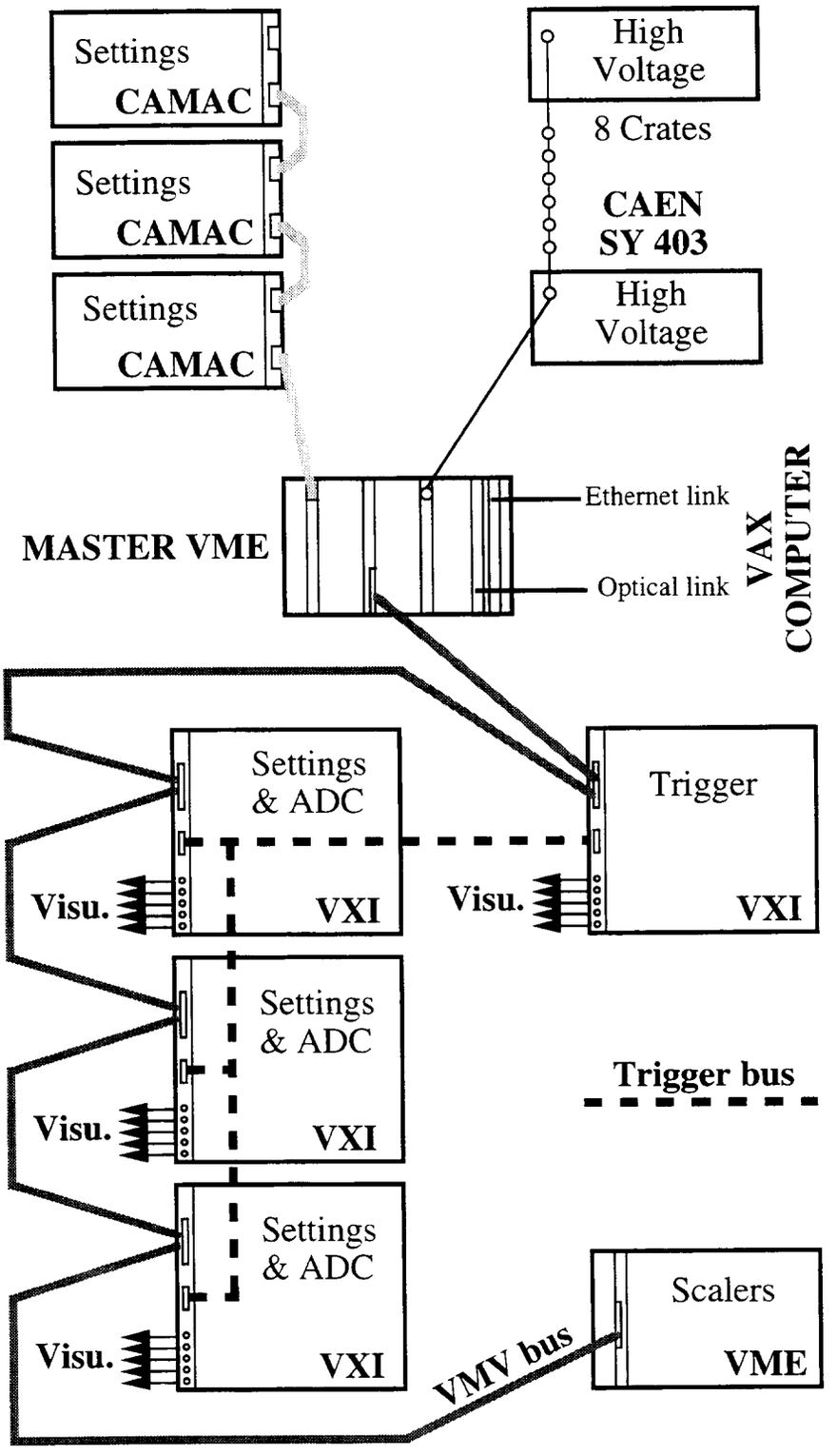

Settings
CAMAC
Settings
CAMAC
Settings
CAMAC
High
Voltage
8 Crates
CAEN
SY 403
High
Voltage
MASTER VME
Ethernet link
Optical link
VAX
COMPUTER
Settings
& ADC
VXI
Visu.
Trigger
VXI
Visu.
Settings
& ADC
VXI
Visu.
Trigger bus
Settings
& ADC
VXI
Visu.
Scalers
VME
VMV bus

Figure 7

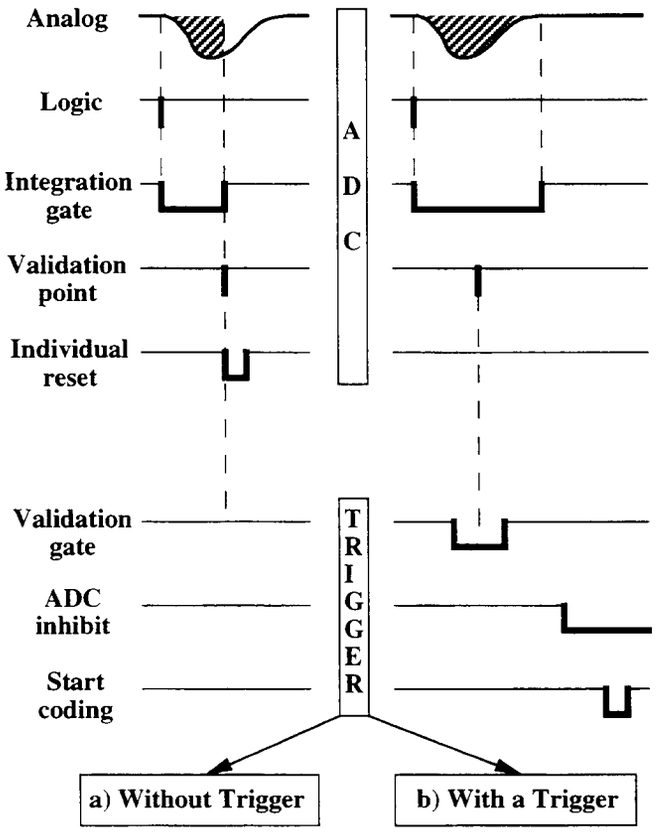


Figure 8

Buses	Functions	External access (Slot0)		Backplane distribution	
		Standard	Connector	VXIbus name	Connector
VME bus	Settings. Controls. Data acquisition	VMV bus	VMV bus connectors	VME bus	P1 and central row of P2
Visualization bus	Analog 1	NIM	Lemo 00	LBUSA/C02	P2 a/c8
	Analog 2	NIM	Lemo 00	LBUSA/C03	P2 a/c9
	Logic 1	NIM	Lemo 00	ECLTRIG3	P3 a3
	Logic 2	NIM	Lemo 00	ECLTRIG4	P3 a5
	Gate control	NIM	Lemo 00	LBUSA/C05	P2 a/c12
Trigger bus	Validation gate 0	NIM	Lemo 00	STARX+/-	P3 a28/29
	Validation gate 1	ECL diff. (+/-)	2 multipoints connectors (IN and OUT) in ECL differential standard	ECLTRG0	P2 a1
	Discriminator inhibit	ECL diff. (+/-)		TTLTRG4	P2 a26
	ADC inhibit	ECL diff. (+/-)		TTLTRG7	P2 c27
	Start coding	ECL diff. (+/-)		TTLTRG6	P2 a27
	General reset	ECL diff. (+/-)		TTLTRG5	P2 c26
	ADC coding line	ECL diff. (+/-)		TTLTRG0	P2 a23
	ADC reading line	ECL diff. (+/-)		TTLTRG1	P2 c23
	ADC test	ECL diff. (+/-)		ECLTRG1	P2 a3
Voltage meas.	Analog setting controls	Inside the Slot0 (VMEbus Access)		LBUSA/C06	P2 a/c14
Clock signals	10 MHz clock	No external access (available from Slot 0 to modules)		CLK10 +/-	P2 c1/2
	100 MHz clock			CLK100 +/-	P3 a31/32
MODID	Module identification	VME/VXIbus access		12 individual lines : Slot0 -> P2a30	

Table 2

Input pulse : exponential rise time variation								
Rise time (10% - 90%) (ns)			200	400	600	800	1000	1200
Time constant (ns)			91	182	273	364	455	546
INDRA Amplifier	RBD_{cha}	(%)	< 0.1	0.3	0.9	1.7	2.5	3.7
	RBD_{amp}	(%)	0.8	3.1	6.4	10.2	13.9	17.5

Input pulse : linear rise time variation								
Rise time (10% - 90%) (ns)			200	400	600	800	1000	1200
Total rise time (ns)			250	500	750	1000	1250	1500
INDRA Amplifier	RBD_{cha}	(%)	< 0.1	0.3	0.7	1.0	1.6	2.2
	RBD_{amp}	(%)	0.9	1.5	3.5	6.2	9.4	13.2
$CR-(RC)^4$ Amplifier	RBD_{amp} $\tau = 1\ \mu s$	(%)	0.06	0.25	0.8	1.0	1.6	2.3
	RBD_{amp} $\tau = 0.25\ \mu s$	(%)	1.0 (0.9)	4.1 (4)	9.4 (8.6)	16.7 (14)	26 (20)	37 (27)

Table 3

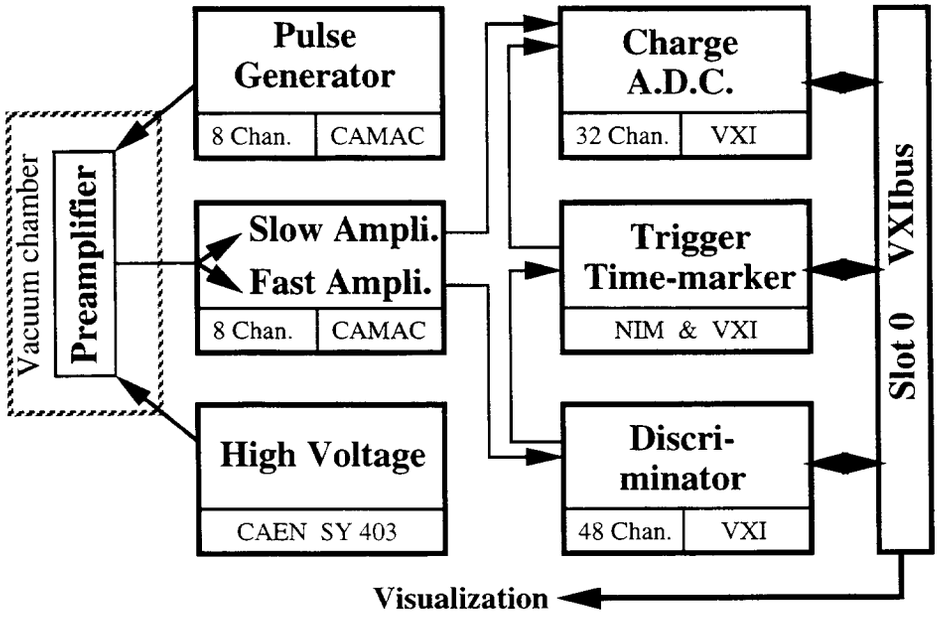


Figure 9

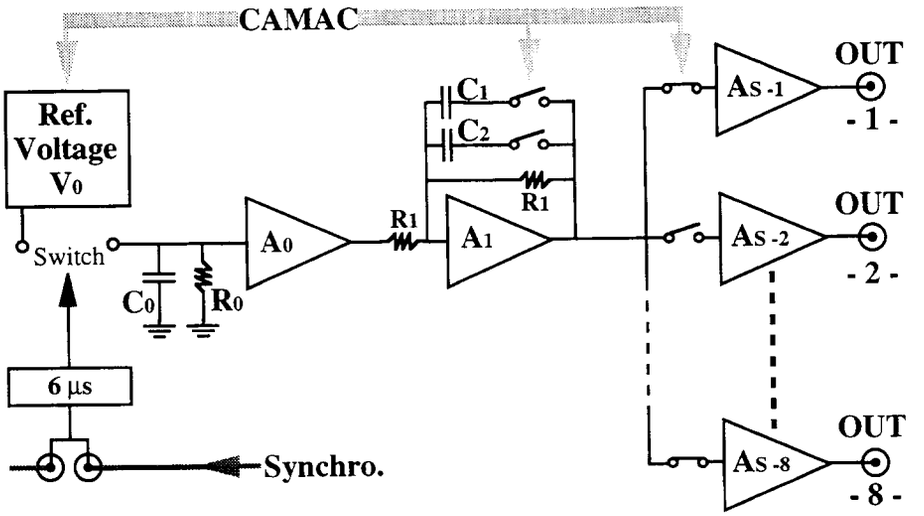


Figure 10

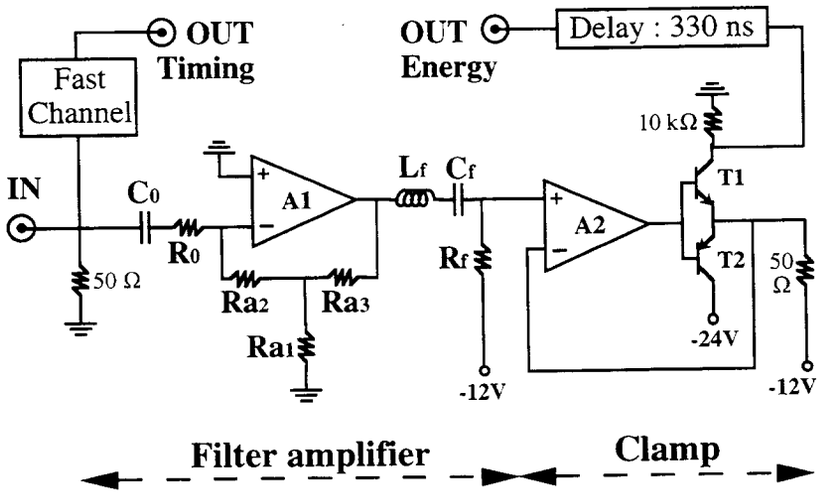


Figure 11

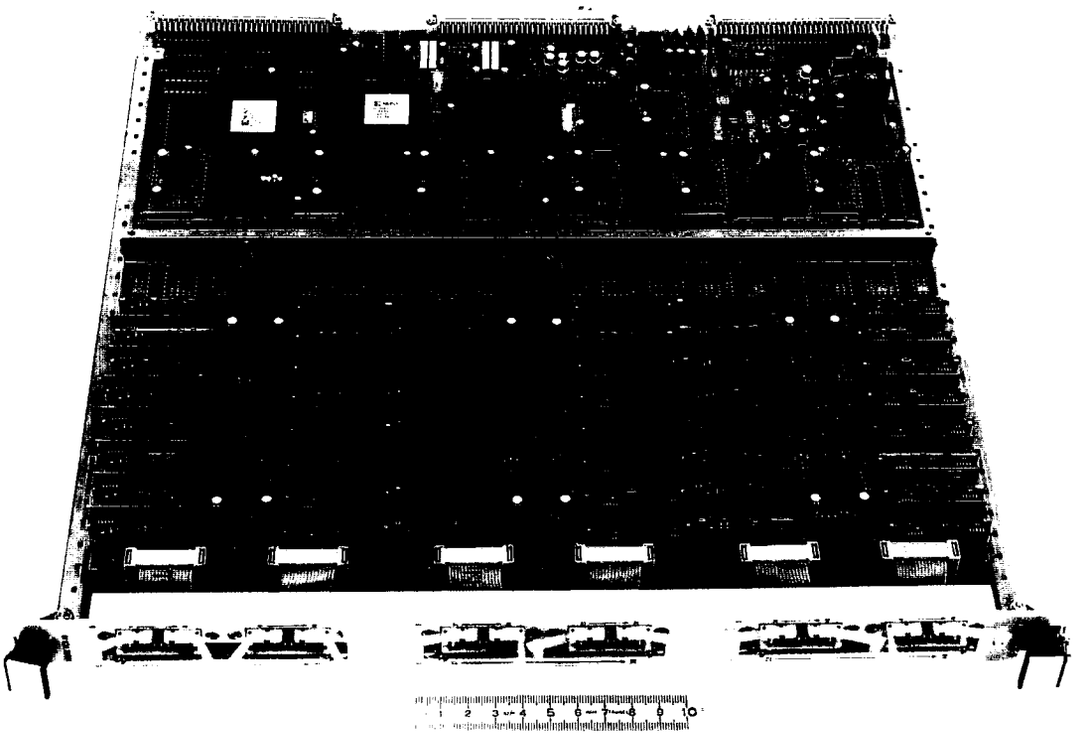


Figure 12

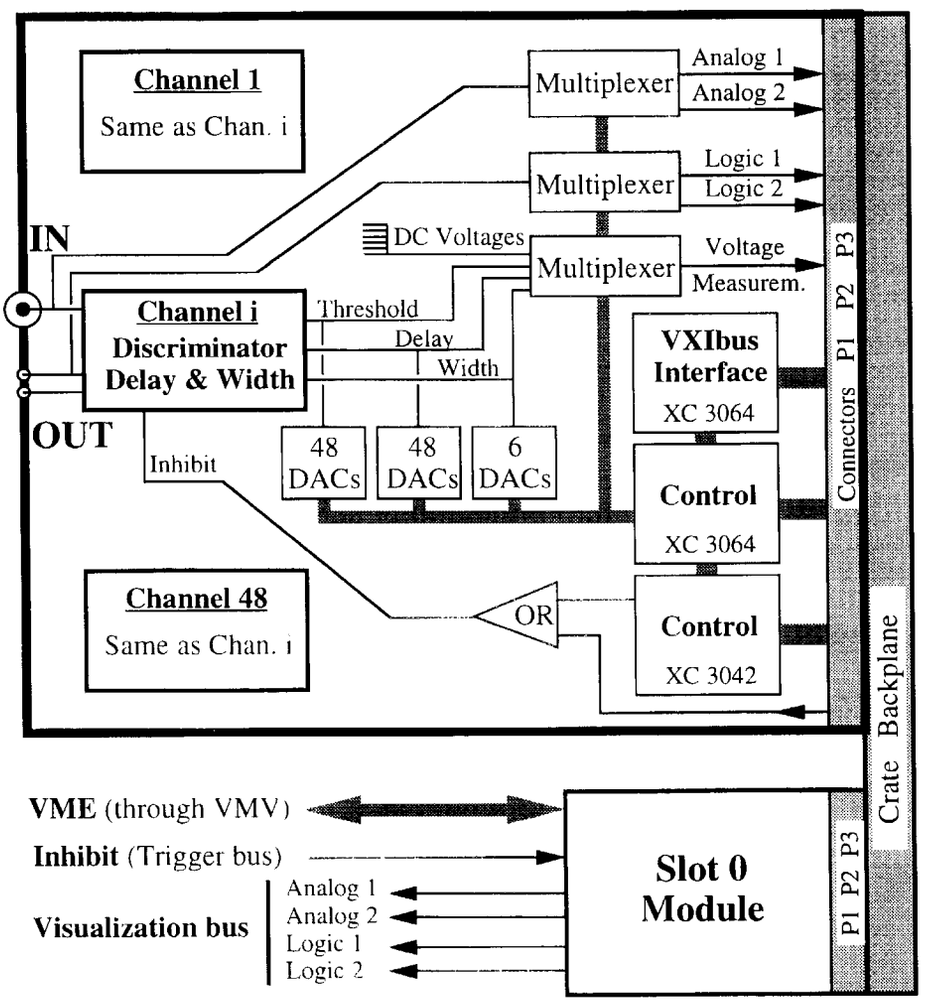


Figure 13

L C A	XC 3042	XC 3064
Equivalent Gates	4200	6400
Configurable Logic Blocks	144	224
Combinatorial Logic Functions	288	448
Latches and Flip-Flops	480	688
Inputs / Outputs	96	120

Table 4

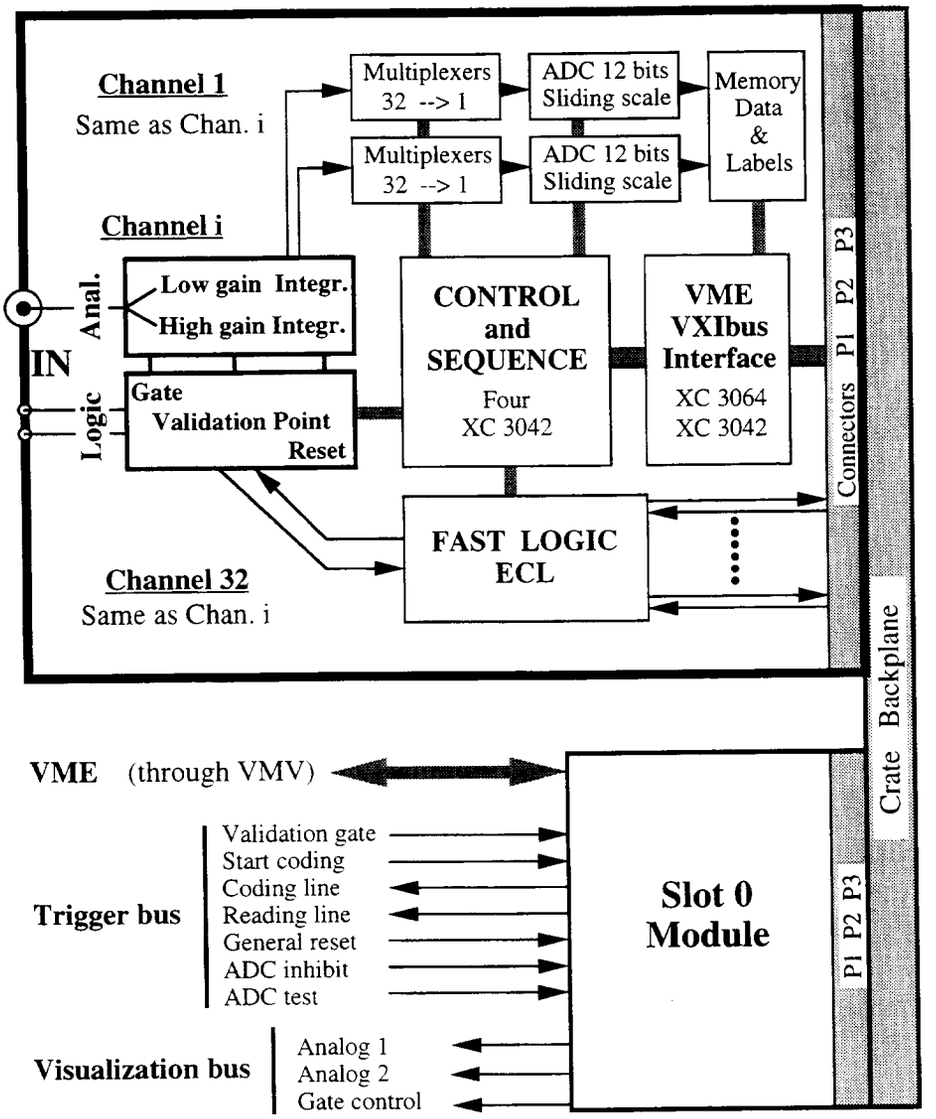


Figure 14

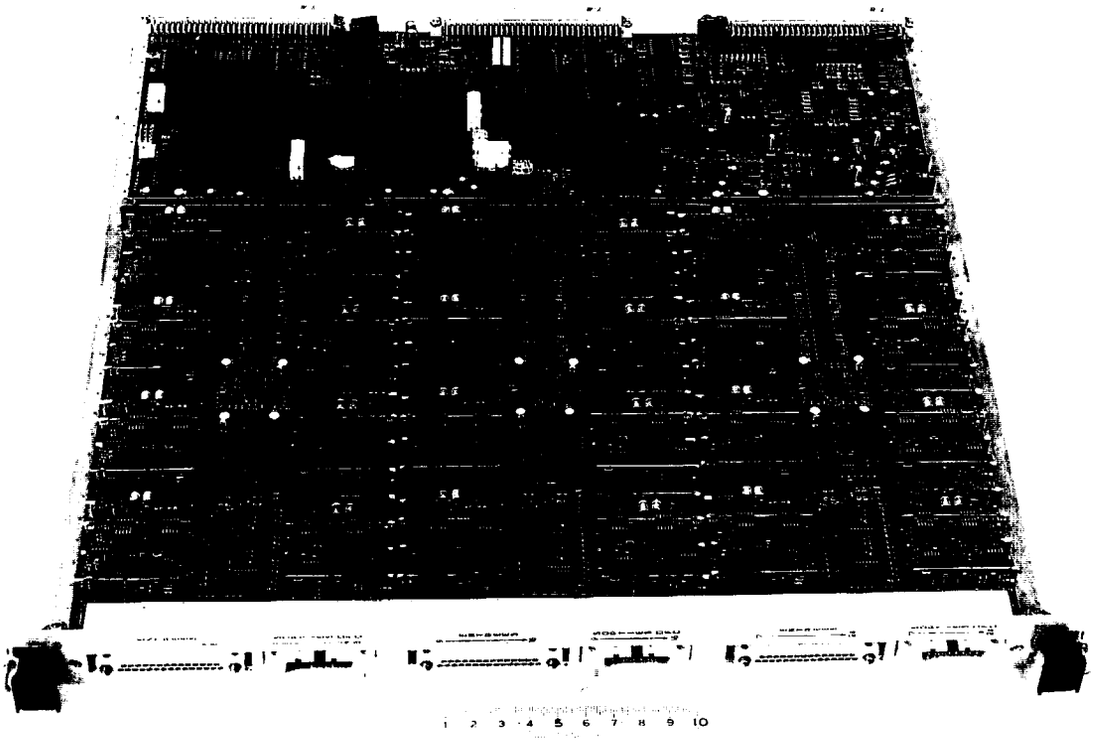


Figure 15

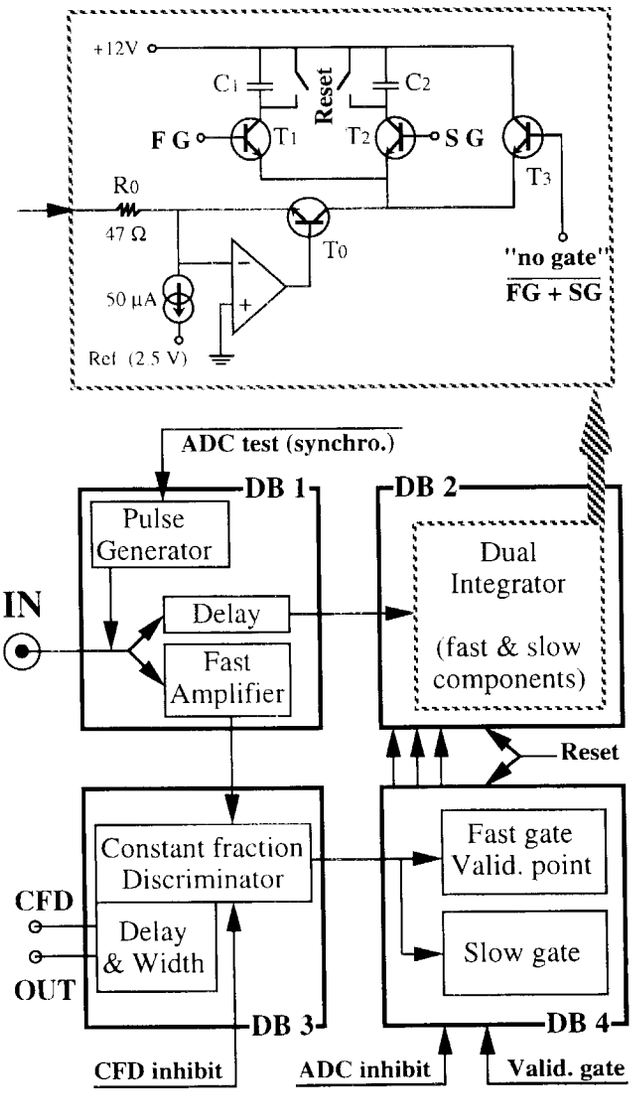


Figure 16

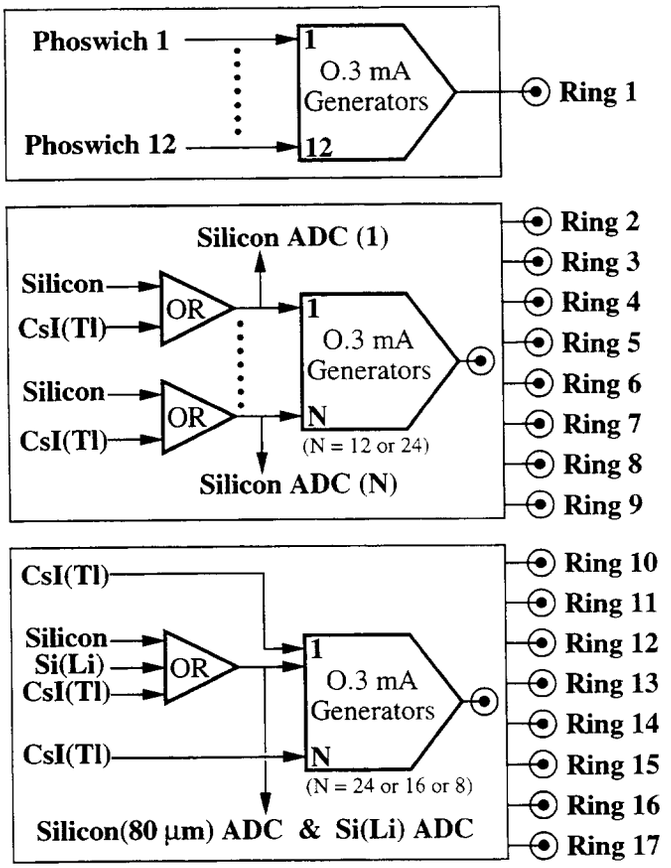


Figure 17

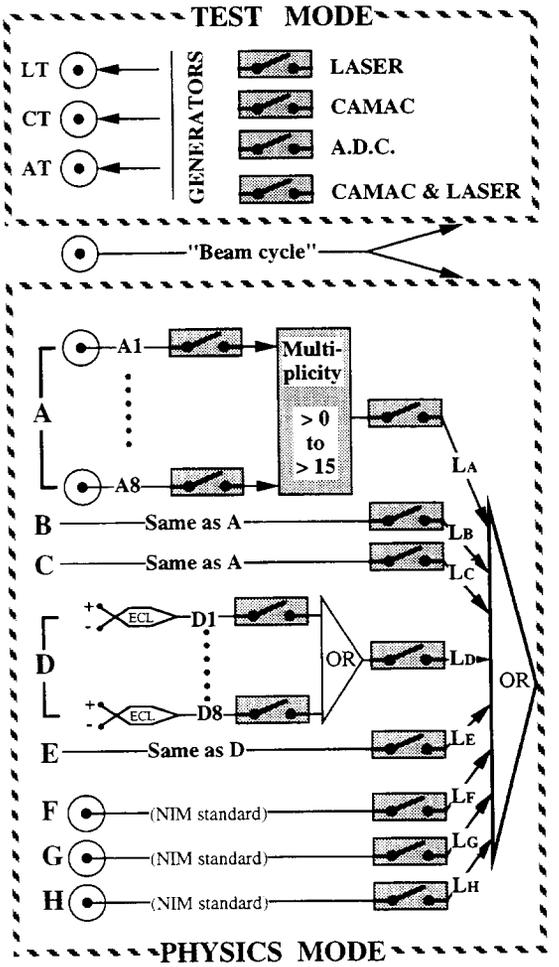


Figure 18

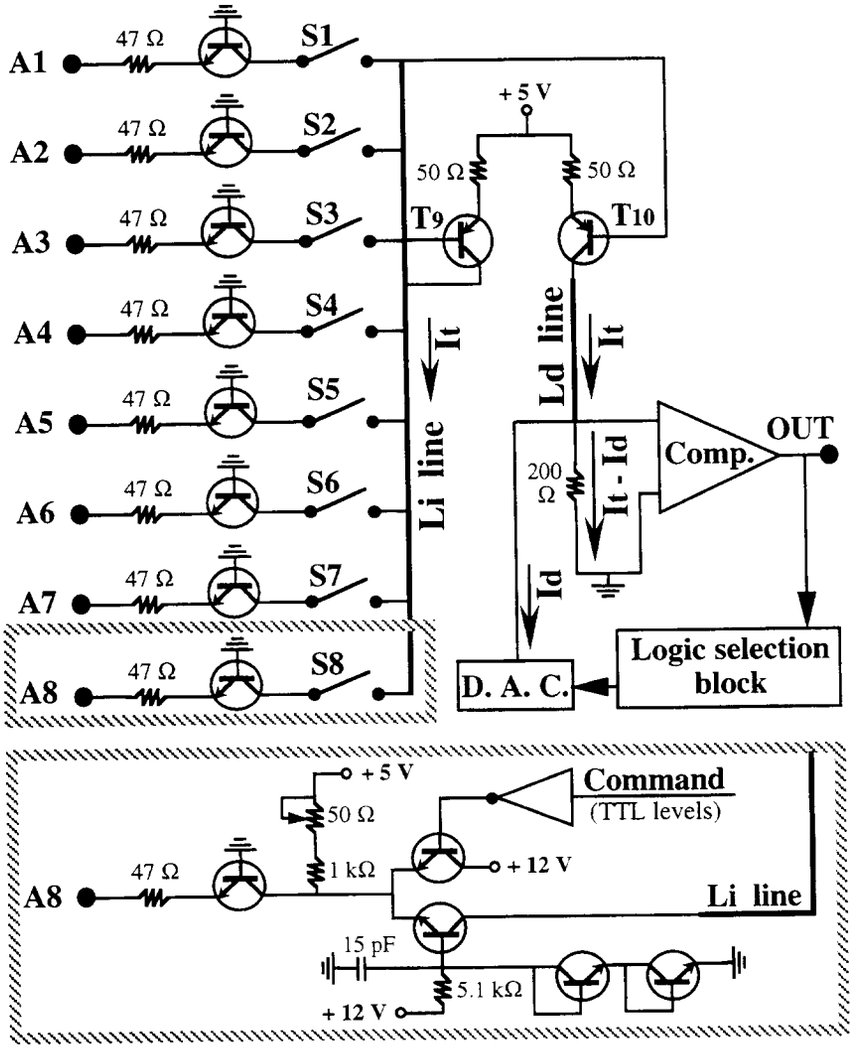


Figure 19

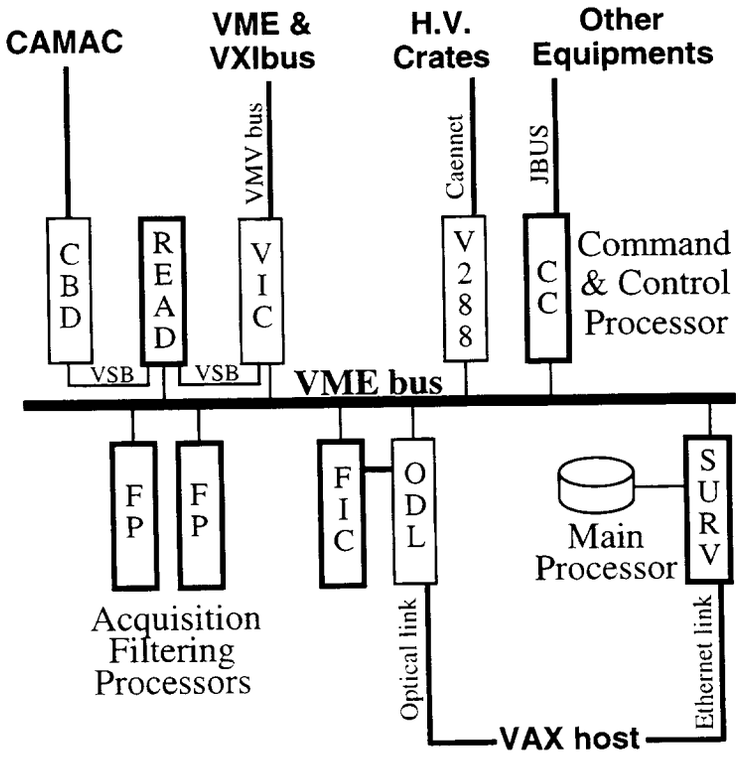


Figure 20

Detector	Module	Standard	Function
Ionization chamber & 300 µm silicon & Calibration telescope (80 µm & 2 mm silicon)	**Charge A.D.C.**	VXIbus (32 channels)	Channel enable
			Gate width
			Validation point
			Offset
			Test amplitude
	Discriminator	VXIbus (48 channels)	Channel enable
			Threshold
			Signal delay
			Signal width
	Time marker	VXIbus (96 channels)	Range
	Amplifier	CAMAC (8 channels)	Gain
	Generator	CAMAC (8 channels)	Amplitude
			Rise time
			Channel enable
Phoswich & CsI(Tl)	**Scintillator modules (all the functions)**	VXIbus (Phoswich : 16 channels) (CsI(Tl) : 24 channels)	Channel enable (Discri.)
			Threshold (Discri.)
			Signal delay (Discri.)
			Signal width (Discri.)
			Fast gate width
			Slow gate delay
			Slow gate width
			Validation point
			Channel enable (Test)
			Test amplitude
	Time marker	VXIbus (96 channels)	Range

Table 5

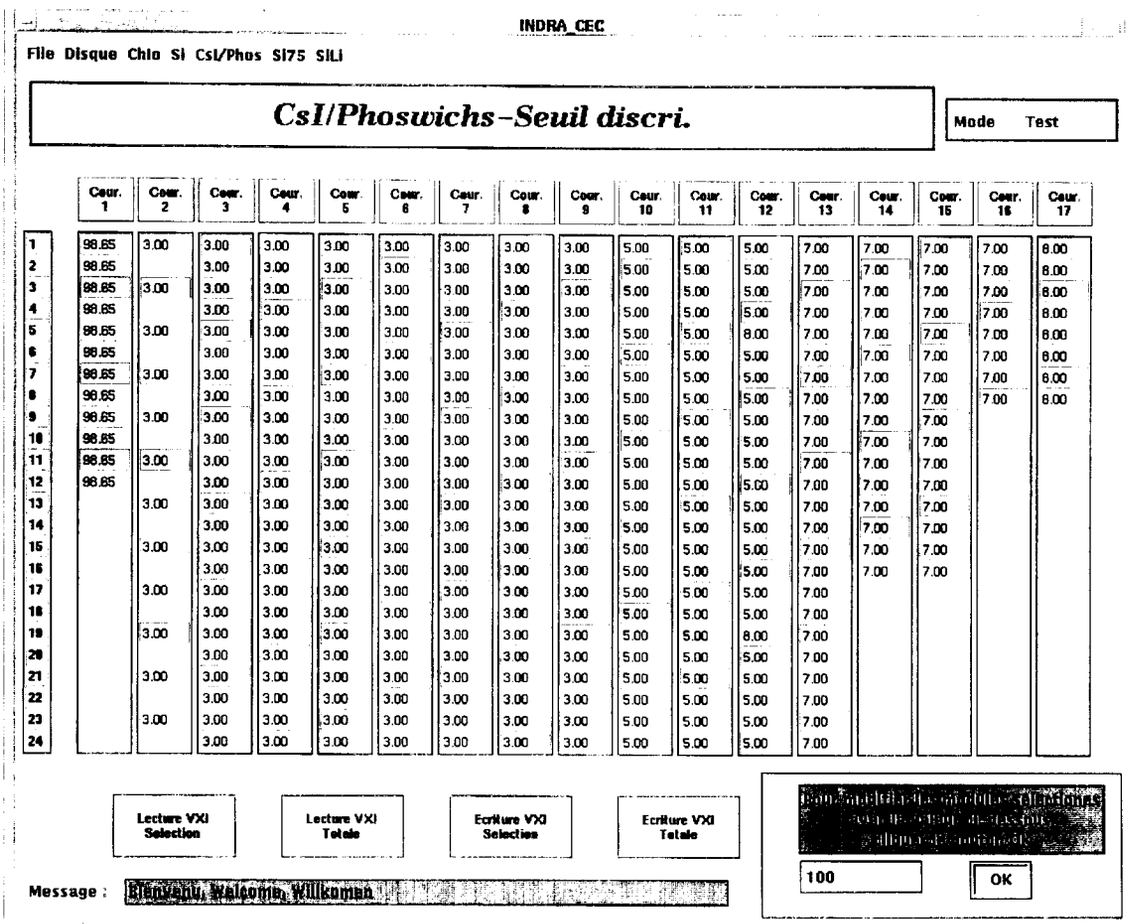


Figure 21