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Quality Control Testing of the HCC ASIC for the HL-LHC ATLAS ITk Strip Detector

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Abstract: The high-luminosity upgrade to the LHC requires a new silicon-strip charged-particle tracking detector for ATLAS. The HCC (Hybrid Controller Chip) is one of three new radiation-tolerant ASICs for this silicon-strip detector. As the interface to multiple binary readout ASICs, the HCC is responsible for buffering and forwarding control signals and readout requests to them as well as serializing their readout data into a 640 Mbps output. All HCCs undergo a suite of tests to verify their analog and digital functionality. The yield for the HCC exceeds the 90% target for production.

Keywords: Particle tracking detectors; Radiation-hard electronics; Digital electronic circuits

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1 Introduction

The high-luminosity upgrade to the Large Hadron Collider (HL-LHC) introduces new challenges for the ATLAS detector [1], related to the planned luminosity increase of up to 7.5 times the nominal rate of proton collisions per second [2]. ATLAS detector subsystems will be upgraded to handle higher radiation levels, stricter timing requirements, and faster readout rates, and they will provide finer detector granularity. Part of this upgrade is a new silicon-strip charged-particle detector for the inner tracker subsystem (ITk Strip) [3]. The HCC (Hybrid Controller Chip) is one of three new radiation-hard ITk Strip ASICs (application-specific integrated circuits) that will be installed in the strip detector modules. The HCC is the interface to the detector analog front-end ASIC, the ABC (ATLAS Binary Chip).

The ITk Strip upgrade will require approximately 25,500 HCCs. Pre-production and production ASICs are manufactured on multi-project silicon wafers containing 557 HCC ASICs. After yield considerations, at least 62 wafers must be probed and diced for production. Using a wafer probing station and a custom designed probe card, contact can be made with all input and output pads of an individual HCC die on a wafer and their digital and analog functionality can be tested. The wafers are diced and the die are then sorted based on the results of the probe tests. Passing die are distributed for detector assembly. A 90% yield of die is targeted for production.

2 The ITk Strip Detector and HCC

The ITk Strip detector is composed of "modules", consisting of the silicon strip sensors, one or two "hybrid" PCBs containing readout ASICs, and a power board providing point-of-load power supply. The layout of an ITk Strip detector module can be seen in figure 1. The silicon strips are read out by the detector analog front-end ASIC, the 256 channel ABC. The HCC is the interface to all the ABCs on a hybrid. In order to meet the technical specifications for readout rate, the final design of these ASICs needs to have dedicated connections between the HCC and each ABC, with up to 11 ABCs per HCC. This "star network" inspired the names for the final design, HCCStar and

ABCStar [3]. (This paper uses "HCC" and "ABC" when there is no confusion.) The HCC forwards clock and control signals to the ABCs, including triggers to request physics data readout, register read and write commands, calibration commands, and resets. The HCC reads out physics data and register read data for each ABC at 160 Mbps. The HCC combines physics data for the same event from up to 11 connected ABCs and sends out this combined data at 640 Mbps. The top-level block diagram for the HCCStar can be seen in figure 2.

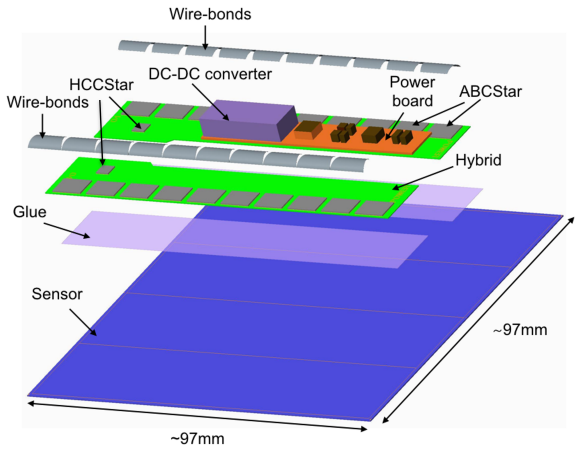

Figure 1. The layout of an ITk Strip detector module with all relevant components. The module electronics consist of a power board and one or two hybrids, with one HCC and a variable number of ABCs on each hybrid. Module design varies in different regions of the detector but features the same component groups; this is a "short-strip barrel module" with two hybrids. (Figure from ref. [3])

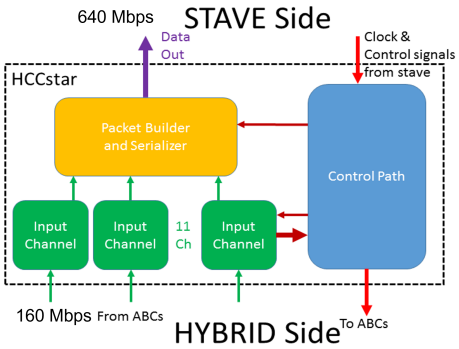

Figure 2. Top-level block diagram for the HCCStar. The HCC serializes data input from up to 11 ABCs on a hybrid at 160 Mbps into a 640 Mbps output stream of packets, and distributes clock and control signals to the ABCs. Physically, these connections to the ABC are within the hybrid ("HYBRID side"), while the output is transmitted on a bus tape over a distance no more than 1.4 m to a device known as the End-of-Substructure card ("STAVE side", referring in actuality to either the "stave" or "petal" substructure design).

The HCCStar is designed for the high-radiation environment inside the ATLAS detector cavern. Radiation testing of the prototype version of the HCCStar, HCCStarV0, revealed vulnerabilities to "single-event effects" in the chip logic, where radiation causes a bit to flip or a transient in a transmission line [4]. The production version, HCCStarV1, triplicates almost all of the logic

with triplicated voters and clock signals to provide triple modular redundancy of vital logic and programmable register settings; additionally, deglitch circuits have been added to input and output pads. The inputs, outputs, and physics data memories are untriplicated. This design has been validated both in simulation and with radiation testing [5–8].

3 HCC Wafer Probing

The pre-production and production HCCs are produced on wafers containing HCCs and other ASICs. Wafers are tested on a FormFactor™ Summit probe station [9] in a cleanroom at the University of Pennsylvania. Contact with an individual die is established using a probe card[1], with needles that have the same spacing as the ring of pads on the HCC. Custom software is used to communicate with the probe station, an Aim-TTi low-voltage power supply [10], and a Nexys FPGA board [11, 12]. This FPGA board runs custom firmware that simulates both the ABCs and the off-module communication. The interface between the FPGA board and the probe card is provided by an FPGA Mezzanine Card (FMC)[2] [13], which has an ADC used by the FPGA board to cross-check analog measurements made by the HCC's internal ADC and to measure communication line levels and currents. Probe tests are sent from the software to the FPGA to be executed and the results are interpreted in software.

The probe testing procedure consists of cleaning probe needles, manually establishing alignment and physical contact with the wafer, then running an automated procedure that steps over each die on the wafer and runs a suite of probe tests. A limited number of recontacts per die are used in the case of poor communication, with an additional probe needle cleaning before in the case of a string of failures.

3.1 HCC Probe Tests

Probe tests are used for quality control of all individual HCC ASICs. These are acceptance tests, used to sort the HCCs into categories based on their analog and digital performance.

Analog functionality tests include ensuring that the internal voltage regulator can be adjusted in a range around the nominal voltage of 1.2 V and calibrating the internal ADC. The power test uses both the HCC's internal ADC and the FMC's ADC to ensure that voltages and currents are within expected ranges, and checks HCC and FMC measurements against each other. Communication tests include setting and reading registers and memory on the HCC and on simulated ABCs, checking their default values after resets, and ensuring that malformed commands are ignored. The trigger test checks that the HCC receives and distributes trigger requests correctly; checks that simulated data is correctly received, processed, and serialized by the HCC; and checks that the HCC correctly receives and identifies errors that are simulated in the ABC response. The memory test checks for stuck bits in all memories. The passthrough test checks that the HCC correctly interprets and reformats control messages to send to individual ABCs. The triplicated clocks test disables one of the triplicated clock trees at a time to ensure each of the individual paths of the triplicated logic functions properly.

[1] designed at the University of Pennsylvania and manufactured by Rucker Kolls, Inc.

[2] specifically the FMC-1701 rev3, designed at Rutherford Appleton Laboratory, UKRI STFC

An HCC that passes all probe tests is considered Category A, and can be used in the ITk Strip detector. HCCs that do not pass only a specific subset of non-critical tests are considered Category B and can be used for system tests such as wire bonding or bench tests. HCCs that experience any failure outside this subset are considered Category X and can not be used in the detector.

3.2 Probe Testing Results

An engineering run of 12 wafers with HCCStarV1 ASICs was tested at the University of Pennsylvania, consisting of a single test wafer, 3 pre-production wafers, and 8 production priming wafers. The test and pre-production wafers are used to develop and finalize the probe-testing procedure, and their ASICs are distributed for testing all steps of the production process as well as various testing purposes. Those purposes include functional testing of single chips, module and system tests, and radiation hardness tests. Production priming wafers are suitable for production.

The probe tests for the HCC were developed on a prototype version, HCCStarV0, and were updated for the production version, HCCStarV1, using data from the test wafer and 3 pre-production wafers. The test wafer was processed rapidly with fewer tests for quicker distribution to module-building sites. The 8 production priming wafers were tested using the final version of the probe tests. The final version of the probe tests runs in 83.5 seconds per die on average, processing a wafer in approximately 13 hours.

The total yield of Category A plus Category B HCCs was 96.7% for the engineering run of 12 wafers, and 96.6% for the final 8 production priming wafers. The total yield of each quality for the production priming wafers is 96.0% Category A, 0.6% Category B, and 3.4% Category X. Figure 3 shows a histogram of yields for the individual wafers. A range of yields between 93% and 99% is observed. Variation in wafer yields for the production priming wafers is due to manufacturing differences; for example, some wafers have significantly more Category B and X die along the edges than others. Figure 4 is a histogram of Category A die at each location over the 12 engineering run wafers; failures are concentrated near the edge of the wafer.

4 Conclusion

The HCC ASIC is a key component of the ATLAS ITk Strip detector, and the radiation-hardness and high readout rate of this ASIC are necessary to withstand the conditions of the HL-LHC. A production-ready system for probe testing the HCC ASIC has been demonstrated, with a suite of tests for analog and digital performance. Yields of HCC ASICs from testing exceed the 90% targeted for production.

Acknowledgments

Many thanks to Dr. Bruce Gallop[3], Dr. Peter Phillips[3], and Matt Warren[4] for their work developing the probing firmware and hardware, their collaboration on the probing software, and lending their expertise and assistance with the probing process.

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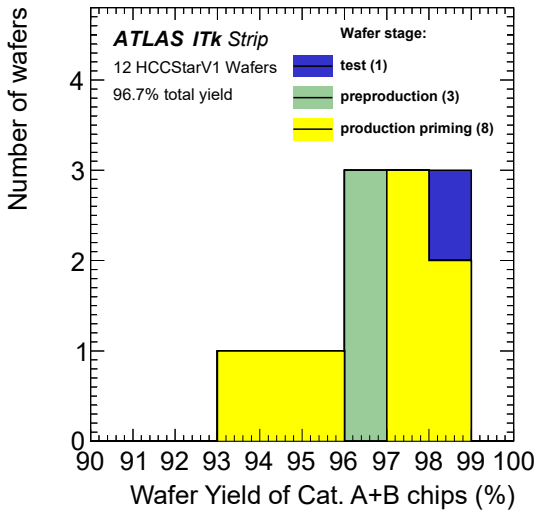

Figure 3. Percent yield of Category A+B HCCStarV1 ASICs from 12 engineering-run wafers. The distribution is split into the first test wafer (blue), three subsequent pre-production wafers (green), and final eight production priming wafers (yellow). The total yield is 96.7% over all 12 wafers, and 96.6% for the 8 production priming wafers. For the production priming wafers, variation in yields is due to manufacturing differences.

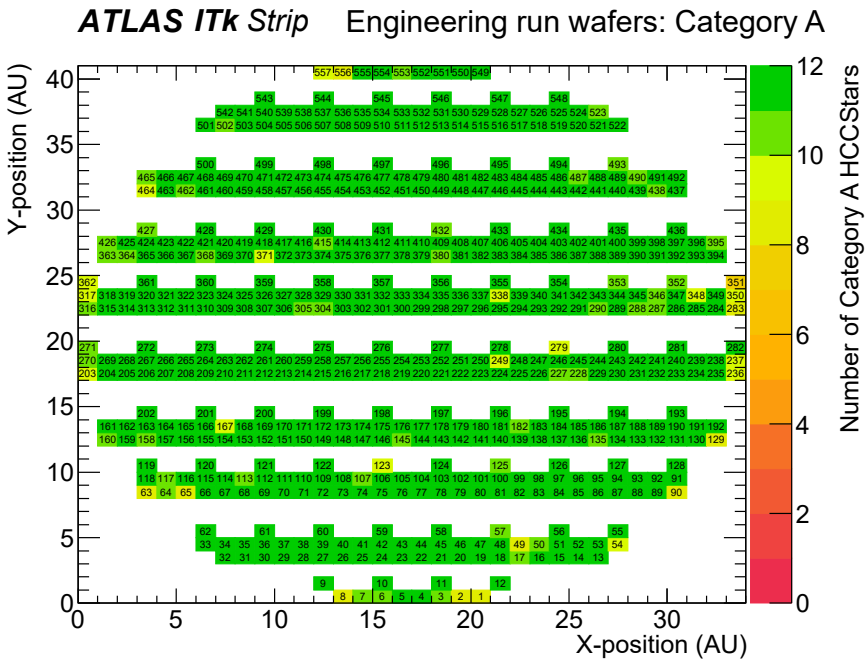

Figure 4. Quantity of Category A HCCStarV1 ASICs as a function of x–y position across 12 engineering-run wafers. Category A ASICs must pass various digital, memory, and analog probe station tests. For the final 8 production priming wafers 4277 of 4456 die passed all probe tests, with the remainder failing one or more tests (Category B or X) due to manufacturing differences.

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