Prepared for submission to JINST

Prototyping Serial Powering for the ATLAS ITk Pixel Detector

Thomas Senger for the ATLAS-ITk collaboration

E-mail: thomas.senger@uni-bonn.de

Abstract: The high luminosity upgrade for the LHC at CERN requires a complete overhaul of the current inner detectors of ATLAS and CMS. A serial powering scheme has been chosen to cope with the constraints of the new pixel detectors. A prototype stave consisting of up to 8 quad modules, based on the new readout chips developed by the RD53 collaboration in 65 nm CMOS technology, RD53A and ITkPixV1, has been set up in Bonn. This contribution covers the results obtained with RD53A modules and presents first measurements with a full ITkPixV1.1 serial powering chain.

ATL-ITK-PROC-2022-027
19 October 2022

Contents

1 Introduction

To overcome the challenges of the High-Luminosity LHC [EB08], the inner tracking detector of ATLAS [ea08] will be replaced by an all-silicon inner tracking system called the ITk [ATL17]. The new detector will consist of 4 layers of strip detectors and 5 layers of pixel detectors. Compared to the current ATLAS Pixel Detector the area of the pixel detector will increase from 2 m^2 to 13 m^2 [ATL17], with more than 8000 pixel modules. To minimize the material budget and power losses on the cables, a serial powering [STF+04, SFH+03, GAB+10] scheme will be used for the ITk pixel detector.

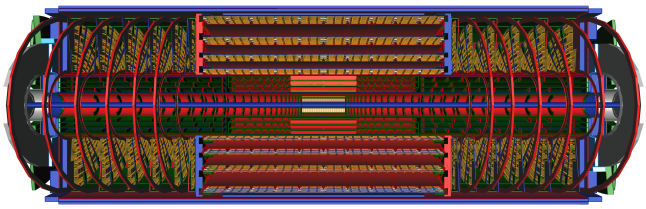


Figure 1: Schematic layout of the Inner tracker detector, consisting of strip detectors and pixel detectors [ftbotAC].

In this scheme n modules are connected in series, where each of these modules consists of m ROC[1], connected in parallel. This chain of modules is powered by one single constant current source, while the supply voltage for the readout chips is generated by the SLDO[2] regulator. Since the current source is one of the crucial building blocks in a serially powered detector, it is important to review the LV PSU specifications. This includes ramp requirements, noise levels, and the ability to react to fast load changes in the chain. As the concept of a serial powering chain has not been used in a detector before, the requirementes for a suitable current source need to be carefully evaluated.

[1] Readout Chip
[2] Shunt Low Dropout

2 ITk Pixel Serial Powering Prototype

A serial powering prototype has been used to evaluate the powering behavior of a SP chain using current generation pixel modules [Hin20], which can be seen in Fig. 2. Up to eight quad-chip modules can be mounted on a mechanical support structure compatible with the RD53A [GS17] and ITkPixV1.1 [GSLC19] quad-chip modules. The services used in this setup are dedicated developments for this prototype with easily accessible test points for debugging purposes.

The EoS[3]-card provides the interface to the power supplies and provides communication between the DAQ system and the quad modules. Through two switches on the EoS-card, the up and downlinks are routed to the modules. The module readout and the EoS-card configuration are done with the DAQ system BDAQ53 [M. 21], developed in Bonn.

Configurable jumpers on the stave flex allow bypassing modules in the serial chain. The LV return line can be decoupled from system GND to connect several staves to build serial powering chains with more than 8 modules in length. In the ATLAS detector, the longest chain will consist of 14 quad modules. Since every quad module dissipates $\mathcal{O}(10\,\mathrm{W})$ of power, the chain needs to be actively cooled. For this purpose, the local support structure is cooled through an ethanol-water mixture.

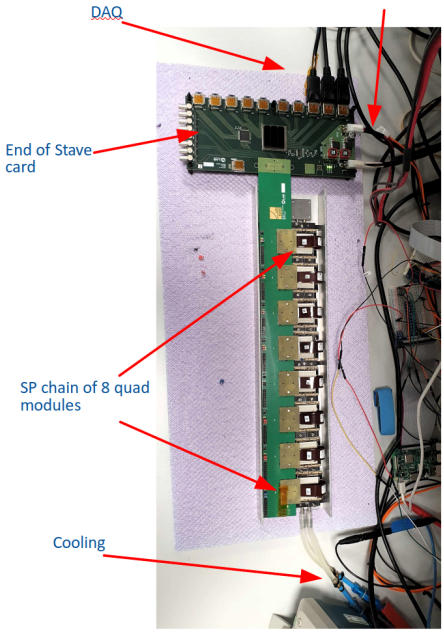


Figure 2: Serial Powering Prototype consisting of 8 quad modules on a local support structure, which is connected to the End of Stave card. These serve the interface of the LV & HV and to the readout, done with BDAQ53.

3 Startup measurements with ITkPixV1.1 digital modules

A current source prototype with an adjustable ramp rate from $1\,\mathrm{A\,s^{-1}}$ to $10\,000\,\mathrm{A\,s^{-1}}$, and a serial powering chain of up to 13 digital ITkPixV1.1 quad modules are used to support the ITk Pixel LV PSU specifications review.

Since start-up issues with RD53A quad modules for low current ramp rates were known, the dependency between the ramp rate and a proper startup of the ITkPixV1.1 quad module chain was investigated. The SLDO of ITkPixV1.1 is in general much more reliable compared to RD53A, such that no issues were expected. However, with low ramp speeds in the range of $<10\,\mathrm{A\,s^{-1}}$ the ITkPix quad module does not start up properly[4]. This behavior can be seen in Fig. 3. If the module starts up properly, as shown in the top part of the figure, the input voltage reaches $\approx$1.7 V and the VDDA of all chips goes up to $\approx$1.2 V, afterward, communication with the chips is possible. On the other hand, if a module does not start up properly, the input voltage remains at $\approx$1.2 V after supplying an input current 1 A or more. Another observation is the oscillation on one of the VDDA channels, which indicates improper startup of the corresponding SLDO. Any communication between the DAQ system

[3] End of Stave

[4] $10\,\mathrm{A\,s^{-1}}$ is out of SLDO specifications

and a module is then not possible. The startup was measured for chain lengths varying between 1 and 8 modules,

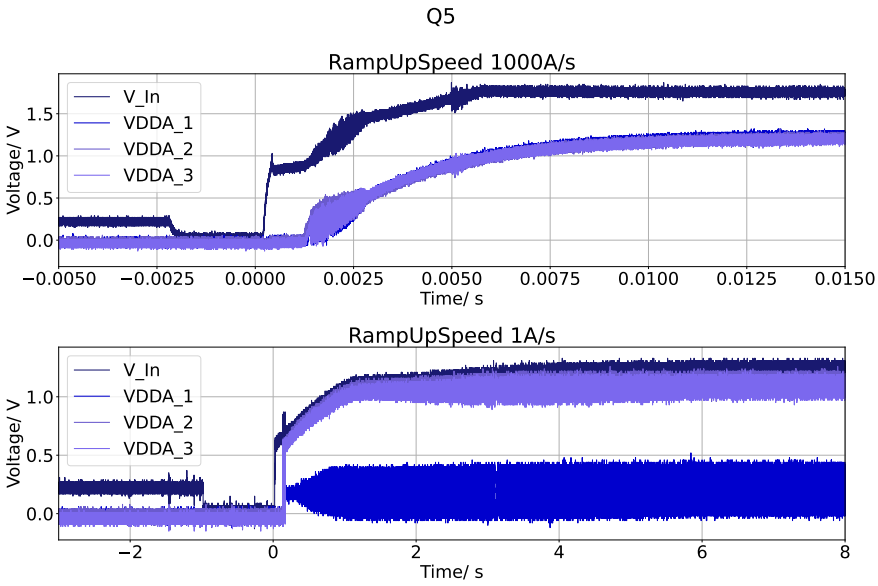


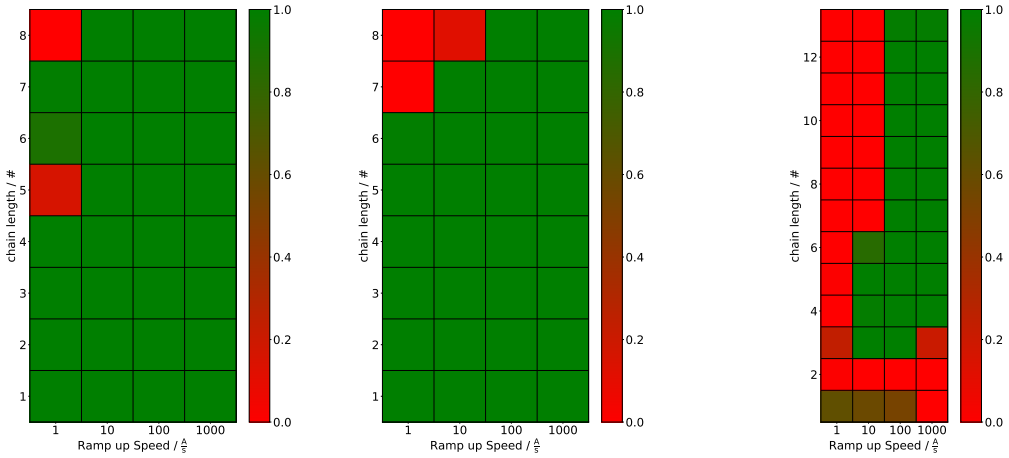
Figure 3: The upper part of the figure shows a successful startup of a digital ITkPixV1.1 quad module. The input voltage reaches 1.7 V and the VDDAs saturate at 1.2 V. The lower figure shows a not properly starting module. The input voltage goes up to 1.2 V and one of the VDDAs shows an oscillating behavior.

for ramp speeds between 1 A s^{-1} up to 1000 A s^{-1} at room temperature, at −20 °C and at −40 °C, which is the coldest detector temperature expected in operation. The corresponding dependency maps can be seen in Fig. 4. At room temperature and −20 °C, more failed start-ups of the serial chain can be observed for longer chain lengths. In addition, unsuccessful start-ups occur for short chain lengths and high ramp speeds at −40 °C. The observed behavior at low ramp speeds is compatible with the SLDO bandgap reference circuit not starting up properly. This is not expected to be an issue during ITk operation, since the LV PSU specifications will require >1000 A s^{-1} and the bandgap issue was fixed after this discovery.

At −40 °C at low ramp rates and longer chains the modules do not start up properly, which can be understood as the bandgap issue, however, the observed behavior at ramp rates >>10 A s^{-1} and small chain lengths up to three quad modules, is understood to be caused by the current source. A small leakage current in the range of a few µA was observed on the current source, while the output was switched off. Due to the steep input IV characteristic of the SLDO at low input currents and the implementation of a high-impedance off-mode in the power supply unit, this leakage is sufficient to generate a voltage drop of ≈ 200 mV over the SLDO.

Moreover, while switching on the current source the voltage drops to zero for a short time before the current is ramped up and no leakage current flows through the chain. This behavior can be seen in Fig. 5a, where the voltage drops to zero for a time Δt. Another measurement showed a positive correlation between the time at zero and the reciprocal value of the ramp rate.

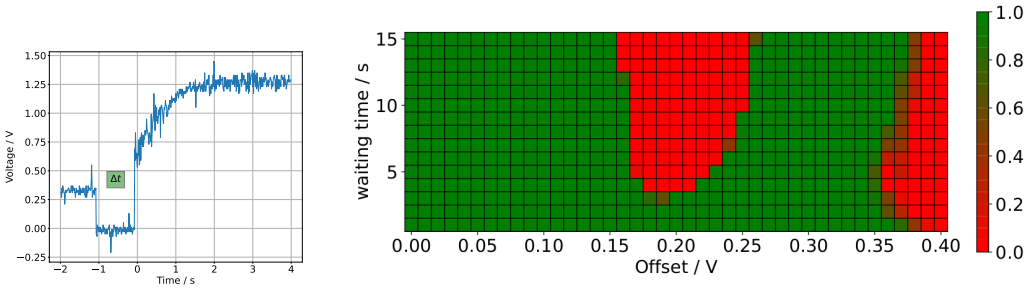
It is suspected that the SLDO is prevented from starting properly by the offset. With a standard bench power supply, it was possible to reproduce the issue, by setting an offset of 250 mV before the start-up. It has been noticed that a certain waiting time on the offset was needed to reproduce the issue. The dependency of the successful startup on the offset and waiting time for a single quad module can be seen in Fig. 5b. This problem can be solved by changing the PSU specifications. A possible solution would be a crowbar in the current source



(a) At room temperature (b) At −20 °C (c) At −40 °C

Figure 4: successful start of a module as a function of the ramp rate, the chain length, and the temperature

or a limitation in leakage current. Since the issue was only visible for fast ramp speeds and thus for short times at a voltage of zero after switching on, a fixed time at zero volts before the ramp-up would be another possible solution.



(a) Start-up behavior of a module. One can notice the time at zero and the offset before startup.

(b) Reproduction of the start-up issue with a power supply. The dependency of the issue on the offset and the waiting time on the offset before the module start-up is shown.

Figure 5: Investigation of the start-up issue at −40 °C

4 Fast load changes

It is important to prevent transients on the input voltage, as this can potentially damage the modules or negatively impact the performance of the readout chips in the SP chain. Therefore, the current source must be able to react quickly to possible load changes e.g. from module failures, which could impact other modules in the serial

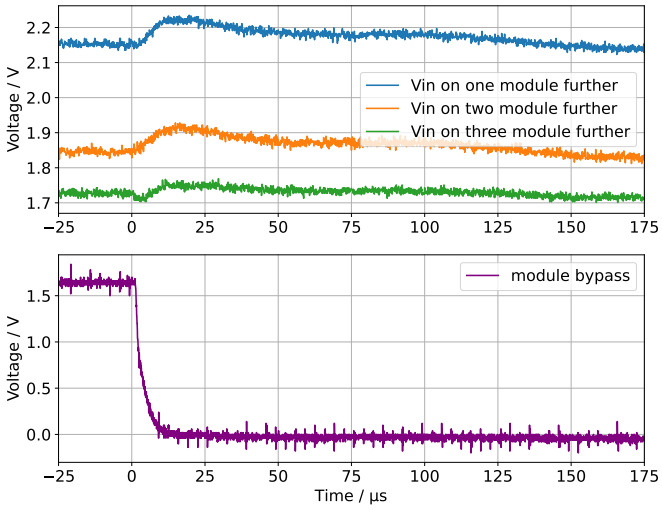


Figure 6: Serial Powering Prototype consisting of 8 quad modules on a local support structure, which is connected to the EoS-card. These serve the interface of the LV & HV and to the readout, done with BDAQ53.

chain. There are two possible tests for a sudden load change with the serial powering prototype. The first option is to reconfigure one module from a low to a high power mode, by enabling all core columns and changing the DAC registers from minimum to maximum value, and then monitoring possible changes in the input voltage of the neighboring quad modules. By an overload of the SLDO the voltage of the reconfigured module dropped by ≈500 mV in 100 µs, while transients on the neighboring modules could not be seen.
Alternatively, the module can be shorted on the stave flex, which causes a more significant load change for the current source. By means of this method, the input voltage of a given module drops from ≈1.7 V to 0 V in less than <10 µs. The results of this measurement are shown in Fig. 6. The lower part of the figure shows the bypass on the module input, while the upper part shows the input voltage of the next three quad modules. As expected, the voltage transient is lowest at the next-to-next-to-next module and highest at the directly neighboring module. The transient amplitude is in the order of 100 mV with a return to baseline within 200 µs. This is a good result and confirms the LV PSU specifications, which provided a current source reaction of minimum 10 µs. Since this measurement was carried out without any configuration of the modules, it would show the worst case in the detector.

5 Summary and Conclusion

To develop the LV PSU specifications for the ATLAS ITk Pixel Detector, a serial powering chain of up to 13 digital ITkPixV1.1 quad modules was set up. Unexpected startup issues were encountered, which are for long chains and low ramp rates likely caused by the bandgap reference of the SLDO. This will be fixed for the next design iteration. The issues for small chains and high ramp rates are likely caused by the PSU and need to be investigated further. They can be circumvented by updating the PSU specifications to include a low impedance off-mode, a limited leakage current, or a fixed time at zero volts before the start-up.

There are first promising measurements of the fast load changes, which confirm that the current specifications for the reaction of the LV PSU in the case of a fast load change are adequate for the operation .

References

[ATL17] ATLAS Collaboration. Technical Design Report for the ATLAS Inner Tracker Pixel Detector. Technical report, CERN, Geneva, 9 2017.

[ea08] The ATLAS Collaboration et al. The ATLAS experiment at the CERN large hadron collider. *Journal of Instrumentation*, 3(08):S08003–S08003, 8 2008.

[EB08] Lyndon Evans and Philip Bryant. LHC machine. *Journal of Instrumentation*, 3(08):S08001–S08001, 8 2008.

[ftbotAC] CERN for the benefit of the ATLAS Collaboration. Expected tracking and related performance with the updated atlas inner tracker layout at the high-luminosity lhc. Last accessed on 2022.09.30 at 05:20 pm. URL=https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PUBNOTES/ATL-PHYS-PUB-2021-024/;.

[GAB+10] L Gonella, D Arutinov, M Barbero, A Eyring, F Hügging, M Karagounis, H Krüger, and N Wermes. A serial powering scheme for the ATLAS pixel detector at sLHC. *Journal of Instrumentation*, 5(12), 2010.

[GS17] Maurice Garcia-Sciveres. The RD53A Integrated Circuit. Technical report, CERN, Geneva, 2017.

[GSLC19] Maurice Garcia-Sciveres, Flavio Loddo, and Jorgen Christiansen. RD53B Manual. Technical report, CERN, Geneva, 2019.

[Hin20] Florian Hinterkeuser. Development and evaluation of prototypes for the ATLAS ITk pixel detector. Technical report, CERN, Geneva, 11 2020.

[M. 21] M. Daas et al. Bdaq53, a versatile pixel detector readout and test system for the atlas and cms hl-lhc upgrades. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 986:164721, 2021.

[SFH+03] Tobias Stockmanns, Peter Fischer, Fabian Hügging, Ivan Peric, Ögmundur Runolfsson, and Norbert Wermes. Serial powering of pixel modules. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 511(1):174–179, 2003. Proceedings of the 11th International Workshop on Vertex Detectors.

[STF+04] Tobias Stockmanns, Duc Bao Ta, P Fischer, Fabian Georg Hügging, Ivan Peric, Ogmundur Runólfsson, and Norbert Wermes. Realisation of serial powering of ATLAS pixel modules. 2004.