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Irradiation testing of ASICs for the HL-LHC ATLAS ITk Strip Detector

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Abstract: For the high-luminosity upgrade to the LHC, the ATLAS Inner Detector will be replaced by an all-silicon tracker (ITk) consisting of two systems: pixels and strips. HCC and AMAC are ITk Strip ASICs vital for performing the system readout, monitoring, and control. To ensure these ASICs will successfully operate in the high-radiation environment of the HL-LHC, they need to be tested for radiation tolerance, and tests have been performed using both heavy ions and protons. The ASIC designs were shown to protect against single-event effects due to radiation.

Keywords: Radiation-hard electronics; Radiation damage to electronic components; Radiation-hard detectors

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1 Introduction

In preparation for the high-luminosity upgrade to the LHC, ATLAS [1] is replacing the Inner Detector with the all-silicon Inner Tracker (ITk), consisting of innermost Pixels and outermost Strips. The ITk is designed to be more radiation hard and to have faster readout than the current Inner Detector, both of which are necessary for the higher luminosity. Each ITk Strip module contains three kinds of ASICs: the ATLAS Binary Chip (ABC), the Hybrid Control Chip (HCC), and the Autonomous Monitoring and Control Chip (AMAC). ABCStar has already been thoroughly tested for radiation effects [2], so this paper will focus on the irradiation test results of the production versions of HCCStarV1 and AMACStar, which are responsible for readout, monitoring, and control. HCC reads out ABC data and sends clock and control signals to the ABCs. AMAC monitors voltages, currents, and temperatures and can control functions on the ITk Strip modules. In the worst-case location, these ASICs are expected to receive a maximum total dose of up to 50 MRad [3]. To confirm HCC and AMAC will function properly in the high radiation environment of the HL-LHC (High Luminosity LHC), performing sufficient testing is critical. HCC and AMAC have also been thoroughly tested for functionality [4, 5] and radiation tolerance using gamma irradiation [6].

Single event effects (SEEs) occur when high energy particles ionize materials as they pass through. HCC and AMAC are sensitive to two types of SEEs: single event upsets (SEUs) and single event transients (SETs). SEUs occur when an ionizing particle causes a change of state. SETs occur when a voltage pulse causes a signal inversion. SEUs affect flip flops, and SETs affect logic gates. The SEE protections implemented by the ASIC designs need to be thoroughly tested. This is accomplished by placing the ASICs in testbeams at laboratory facilities and monitoring their performance. While the beam is being delivered, SEEs are expected to occur and to be corrected by the ASIC designs. Differentiating between SEUs and SETs is not possible in the beam tests, but simulations show that the ASIC designs protect against both [7].

The ASIC designs protect HCC and AMAC through triplication and majority voting. Most of the logic in both chips is triplicated. Due to space constraints, HCC has some components that are not triplicated, including inputs, outputs, and the large memories related to physics data. For

triplicated logic, three identical copies are compared and vote to decide the correct value. The voters are also triplicated. Deglitchers on digital input pads offer additional protection from SETs. Triplication relies on two of the three copies being correct, which means a double SEE would flip the triplicated logic state and would result in the wrong value being saved. Double SEEs are extremely unlikely and are not expected to occur at the HL-LHC. Additionally, the flip flops have been arranged to have a minimum spacing of 15 µm to reduce the chance that a single particle could flip multiple cells. The goal of the beam tests is to determine if the ASICs are well enough protected from SEEs.

Testing details and results from heavy ion irradiation tests and proton tests will be presented and discussed in Section 2 and Section 3, respectively. Conclusions and HL-LHC expectations can be found in Section 4.

2 Heavy ion irradiation

Tests were performed using UCLouvain's heavy ion irradiation facility in February 2022. Single-chip board test setups containing one ASIC and the relevant electronics were used. HCC and AMAC single-chip boards were mounted to a cold plate and placed inside a vacuum chamber. The beam is aligned with one chip at a time, and a continuous software loop runs to count how many SEEs occur and are corrected. Various types of heavy ions are available for testing, and each is primarily defined by its linear energy transfer (LET), which is the energy per unit length a particle loses as it passes through a material. Ions with higher LETs cause bit flips to occur more frequently. The eventual goal is to apply a fit to the heavy ion data collected and extrapolate to the LETs expected at the HL-LHC. Consequently, collecting sufficient data for a range of LETs was essential. Eight ions were tested for HCC and AMAC with LETs of 1.4–62.5 MeV $\cdot$ cm^2/mg and an average fluence of $5.5 \cdot 10^7$ ions/cm^2.

HCC and AMAC performed well operationally during the heavy ion tests. As expected, single SEEs occurred and were automatically corrected by the triplication protections, and the corrected SEE rate increased with LET. No double SEEs were observed. Triplication protections were turned off by disabling one of the three identical clock trees, and uncorrected SEEs were then observed, which confirms triplication was working as expected. HCC and AMAC occasionally became non-responsive and needed resets during the highest two LET runs, which require further investigation.

2.1 Results

The SEE counts were turned into cross sections for each LET value using:

$$\sigma^{\text{corr}}_{\text{SEEs}} = \frac{n^{\text{corr}}_{\text{SEEs}}}{\text{fluence} \cdot \text{bits monitored}} \tag{2.1}$$

where $n^{\text{corr}}_{\text{SEEs}}$ is the number of logic flips detected and corrected by the triplication protections and $\sigma^{\text{corr}}_{\text{SEEs}}$ is the cross section of corrected SEEs. Normalizing for bits monitored allowed for easier comparison between HCC (512 bits monitored) and AMAC (1984 bits monitored). The Weibull distribution is commonly used to model failures of electronic components and predict the reliability

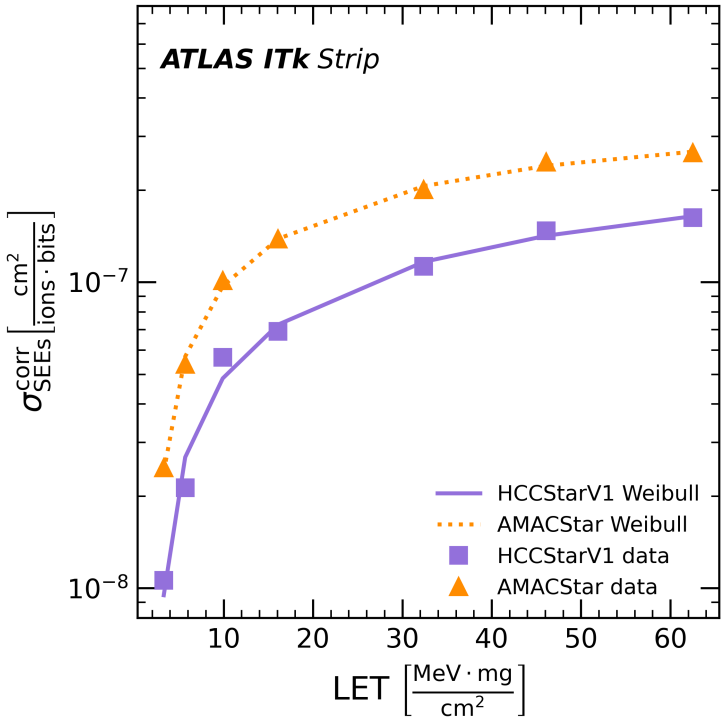

Figure 1: The cross section of corrected SEEs measured at the Louvain heavy ion testbeam as a function of ion LET for HCCStarV1 (purple square) and AMACStar (orange triangle). The results are parameterized by the Weibull distribution for HCCStarV1 (solid purple line) and AMACStar (dotted orange line).

and survivability of a component [8]. As seen in figure 1, the Weibull distribution was used to parameterize the cross-section data. The distribution relies on four parameters and is described by:

$$\sigma(E) = \sigma_0 \left\{ 1 - \exp\left[\left(\frac{E - E_0}{W} \right)^S \right] \right\} \tag{2.2}$$

where σ_0 is the saturated cross-section of a radiation effect, E_0 is a threshold related to minimum LET necessary to cause the effect, W is the width, and S is a shape modification. The Weibull parameters calculated for the ASICs are shown in Table 1.

By convolving the Weibull distribution from experimental testbeam results with the LET distribution the ASICs are expected to be subjected to at the HL-LHC, SEE rates at the HL-LHC can be estimated [8]. Based on the Weibull parameters, the projected HL-LHC SEE cross-section is $1.2 \cdot 10^{-13}$ cm^2/ion per AMAC bit and $5.2 \cdot 10^{-14}$ cm^2/ion per HCC bit. Multiplying these projected cross sections by the maximum 1 MeV equivalent neutron fluence of $8.1 \cdot 10^{14}$ cm^{-2} expected in the highest radiation region of the detector Endcap, one expects to see 100 corrected bit flips per bit in AMAC and 40 corrected bit flips per bit in HCC in the HL-LHC lifetime. Since these projections are based on heavy ion data, they should be taken with a safety factor of 5, as recommended by an internal ATLAS task force on radiation effects.

Table 1: Weibull parameters based on Louvain heavy ion data.

	$\sigma_0 \left[\frac{\text{cm}^2}{\text{ion}}\right]$	$E_0 \left[\frac{\text{MeV}\cdot\text{cm}^2}{\text{mg}}\right]$	$W \left[\frac{\text{MeV}\cdot\text{cm}^2}{\text{mg}}\right]$	S
AMAC	$(2.5 \pm 0.4) \cdot 10^{-7}$	2.5 ± 0.3	56 ± 19	0.8 ± 0.1
HCC	$(3.3 \pm 0.6) \cdot 10^{-7}$	2.3 ± 0.7	31 ± 13	0.7 ± 0.1

The distribution of SEEs across registers and time was used to validate the model of a single time-independent cross-section per bit applicable to all bits in the chip. Based on the heavy ion data, bit flips in the non-triplicated HCC data are expected to occur at a rate of about 10 orders of magnitude lower than that of electronic noise at the HL-LHC.

The resets that occurred at the two highest LET values require further investigation. They are likely due to higher LET ions causing more disruptive issues than just a single bit flip because they deposit more energy across the chip surface. These effects will be much rarer at the HL-LHC, and LETs above 32.4 $\text{MeV}\cdot\text{cm}^2/\text{mg}$ are not expected to occur with significant frequency. For Rh and Xe (LETs of 46.1 and 62.5 $\text{MeV}\cdot\text{cm}^2/\text{mg}$, respectively), HCC needed infrequent register resets, with a conservative maximum extrapolated HL-LHC rate of 9 register resets needed per HCC per year. However, HCC register resets take on the order of a millisecond to identify and to correct. AMAC had communication issues for the two highest LET ions, which were solved with hard resets.

3 Proton irradiation

Tests were performed using the Proton Irradiation Facility at TRIUMF in Vancouver in May 2022. Two HCCs and two AMACs were tested simultaneously. The ASICs received a total fluence roughly equivalent to 8% of the HL-LHC lifetime over 40 hours of beam time. HCC and AMAC both performed well operationally throughout the beam period. Similar to what was observed in Louvain, HCC needed infrequent register resets, and AMAC needed to be power cycled due to SEEs seen by the test electronics. These issues have been observed at high LETs in Louvain and less frequently in testbench without beam and are not considered issues with chip functionality.

3.1 Results

The TRIUMF cross-section calculations were performed in a similar manner as Louvain, but a fluence correction factor was applied to account for relative beam alignment and uncertainties in the beam profile. The cumulative cross-section for each chip is shown in table 2, and the average cross sections are then used to calculate the lifetime projections.

Based on the TRIUMF data, 180 correctable bit flips per bit in HCC and 240 correctable bit flips per bit in AMAC are expected in the HL-LHC lifetime. Considering the safety factor on the heavy ion data, the proton test results confirm the Louvain results.

Table 2: Cumulative corrected bit flip (CBF) cross sections from TRIUMF proton data.

	Cumulative CBF cross-section
HCC 1	$1.5 \cdot 10^{-13}$
HCC 2	$2.1 \cdot 10^{-13}$
AMAC 1	$2.2 \cdot 10^{-13}$
AMAC 2	$2.6 \cdot 10^{-13}$

4 Conclusion

Based on the irradiation test results, the triplication implemented by the ASIC designs of HCC and AMAC is effective in mitigating SEEs. Extrapolations from the test results suggest both HCC and AMAC will perform well in the HL-LHC, each seeing $O(10)$ correctable bit flips per bit per year. The heavy ion tests showed that neither HCC or AMAC are expected to need hard resets for the LET values expected at the HL-LHC. Based on the proton tests, the register resets observed for HCC may be needed at the HL-LHC, but they are not expected to occur with significant frequency and are quick to identify and correct. The power cycles AMAC needed at TRIUMF were due to a test setup issue and not a functionality issue with AMAC itself. Based on these results, both ASICs have passed internal reviews and are ready for production.

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