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Quality Control Testing of the AMAC ASIC for the HL-LHC ATLAS ITk Strip Detector

T.C. Gosart,[1][a] L.F. Gutierrez Zagazeta,[a] P.T. Keener,[a] J. Kroll,[a] S. Lu,[a] G. Mayers[a] F.M. Newcomer,[a] A. Nikolica,[a] M.B. Reilly[a] E. Thomson[a]

[a] *Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, PA, USA 19104*

E-mail: tgosart3@sas.upenn.edu

Abstract: The ATLAS detector requires an all new inner detector, the Inner Tracker (ITk), due to the high-luminosity upgrade to the LHC (HL-LHC). The AMACStar is one of three radiation hard ASICs that will be installed on the ITk Strip subdetector modules. The ASIC operates autonomously and its function is to monitor and control the temperatures, voltages, and currents in the module components, preventing these quantities from reaching dangerous levels. A total of 18000 AMACStars are needed for the ITk Strip subsystem. Wafers of these chips are probed at the University of Pennsylvania. Comprehensive probe-station testing software and procedures have been developed in order to verify the digital and analog functionality of every AMACStar. A detailed grading scheme is applied to determine which chips should be installed on the modules. The results from probing the first 11 wafers with the final design satisfy the required 90% yield needed for production goals. Probing of production AMACStar wafers will begin in 2023.

Keywords: Analogue electronic circuits; Digital electronic circuits; Radiation-hard electronics; Particle detectors

[1]Corresponding author.

1 ATLAS ITk Strip Detector

In light of the high-luminosity LHC (HL-LHC), the existing ATLAS detector requires upgrades in order to satisfy new radiation, granularity, and timing requirements [1, 2]. The ATLAS Inner Tracker detector (ITk) will replace the existing ATLAS tracker system [3]. This detector will contain two subdetectors: outer Strip and inner Pixel. The Strip subdetector consists of four double-sided layers in the detector barrel and six double-sided disks in the two detector end-caps. Both the barrel and end-cap detectors are made of carbon composite structures that contain modules. **Figure 1** shows a schematic of a barrel detector module. These modules contain silicon sensors and readout electronics, including three application specific integrated circuits (ASICs): the ABC (ATLAS Binary Chip), HCC (Hybrid Controller Chip), and AMAC (Autonomous Monitor And Control). The AMAC is located on the module powerboard, an image of which is shown in **Figure 2** [4].

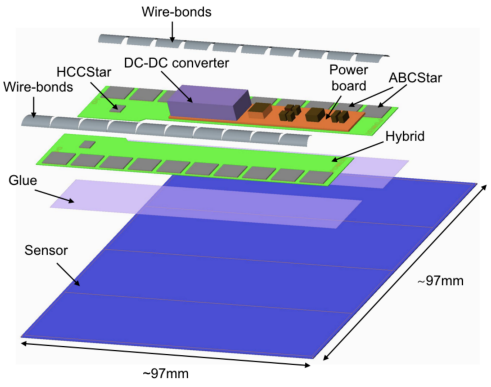

Figure 1: Schematic of an ITk Strip barrel module, with various components labeled. The ABCStar and HCCStar ASICs are located on the green printed circuit board (PCB) hybrids [3].

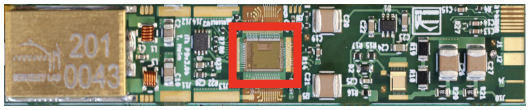

Figure 2: Image of the module powerboard. The red box shows the location of the AMAC.

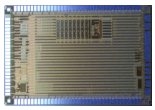

Figure 3: A microscope image of an AMACStar chip, with the pad ring visible.

2 The AMACStar ASIC

AMACStar is the final design version of the AMAC [5]. It performs critical monitoring and protective interruption functionalities in the operation of the module. The chip autonomously monitors the voltages, currents, and temperatures of components on the hybrids and powerboard and controls the power state of DC/DC regulators (which power the ASICs) and HV bias switches. Using a 16 channel ADC and interlock mechanism, the chip can raise flags if any vital quantities fall outside their expected operating ranges and disable the necessary voltages. Further, the AMACStar can set the HCC and ABC chips into special low power states, mostly disabling them, if these components are problematic [6]. An image of an AMACStar is shown in **Figure 3**. The first batch

of AMACStars were produced in a fabrication lot of 12 wafers. Four of these wafers were used for the pre-production stage (three were probed), during which the design, functionality, and radiation hardness of the chip have been heavily tested and meet the necessary requirements [7, 8].

3 Testing the AMACStars

An extensive testing software has been developed in order to ensure that every single AMACStar that will be installed in a module meets the quality and performance requirements of the detector. The software is designed to test each aspect of the chip's digital and analog functionality. Individual tests were developed and refined using an AMACStar on a single chip board (SCB) testing setup. The SCB is also used to debug unexpected problems occurring during probing or other functionality testing. The final testing suite, which was applied for production priming[1] and is being used in production, contains a total of 60 analog and digital tests and takes approximately 3 minutes to run per chip. A discussion of each individual test is beyond the scope of this note, but four tests are presented as examples, with descriptions and plots shown in **Figure 4**.

4 Penn Probe Station

A clean room set-up at the University of Pennsylvania contains the Summit probe station that is used to probe shared wafers of HCCStar and AMACStar chips [9]. Each wafer contains 487 AMACStars. Before probing of a wafer can begin, the wafer is carefully inspected and loaded into the probe station. To physically connect to and communicate with the chips, a custom probe card with thin needles is used,[2] which must be precisely aligned with the pads on the chip. The probe station microscope and software is then used to align the wafer with the needles. From there, contact is carefully established with the first AMACStar on the wafer. Once contact is made, the testing software is run only on the first AMACStar to ensure that the set-up was properly done. If there are no problems, probing can commence on all of the AMACStar die on the wafer with an automated procedure. Any AMACStar that does not pass every test on the first try is probed a second time after recontacting the pads with the needles, since failures can arise from poor contact with the chip. In total, about 27 hours is needed to complete the probing of all the AMACStars on a single wafer.

5 Results from Pre-Production and Priming

Once probing is completed for a given wafer, the testing data is run through post-processing software, also developed at UPenn. The software uses grading parameters to assess the digital and analog performance of the chips, with each AMACStar receiving one of three grades: Category A, B, or X. **Table 1** describes the criteria used to assign each grade. All 'Category A' AMACStars can be readily used in the detector. 'Category B' AMACStars may also be used, however they have some measured parameters, which, while acceptable, are outside the typical range seen in

[1] Eight of the first 12 wafers were used for "production priming." These are additional wafers which were ordered along with those for pre-production and are treated as the first phase of production. They allow for having production parts in hand earlier that would otherwise be possible. AMACStars from these wafers will be used in the detector.

[2] The probe card was designed at UPenn and manufactured by Rucker Kolls, Inc.

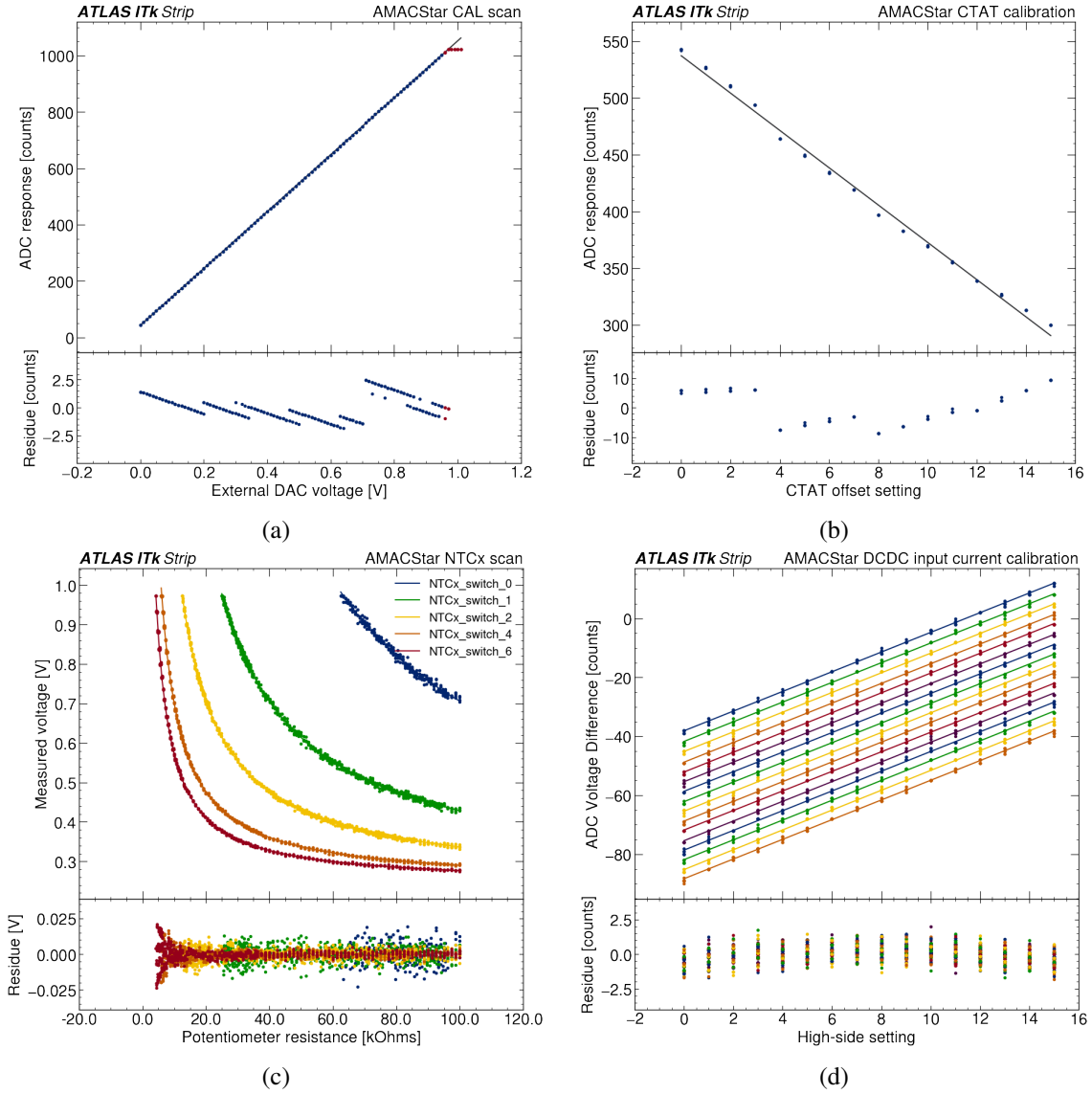

Figure 4: Functional characterizations of a single AMACStar ASIC. All distributions are fitted with the expected functional form (solid lines), with the bottom panel showing the residue of the fit. (a) The linear response of AMACStar's ADC to an independent calibration voltage, measured by the chip's analog monitor (AM). Points near the saturation level (red) are excluded from the fit. (b) The calibration test of the CTAT (complementary to absolute temperature) offset, used for AMACStar internal temperature measurements. (c) The response of the NTCx line to a potentiometer used to emulate a thermistor voltage. The switches correspond to different temperature ranges. AMACStar has three dedicated NTC sensor lines: NTCx and NTCy from the hybrids and NTCpb from the powerboard. (d) A test that is used to measure the high side (11 V) current into the DCDC converter. Two external resistors with precision-matched currents supplied by AMACStar are used to drop the voltage across the high side shunt to 800 mV, where the shunt voltage difference can be measured by the chip. A range of current adjustments are used to match the voltage drop in the two external resistors. [10].

other AMACStars. They are to be used only in the case where there is an insufficient quantity of 'Category A' chips. 'Category X' AMACStars are not used for any purpose after probing.

Table 1: Descriptions of the performance grades assigned to AMACStars.

Grade	Description
Category A (Cat. A)	All digital and analog parameters within expected range
Category B (Cat. B)	All digital and vital analog parameters within expected range
Category X (Cat. X)	At least one digital or vital analog parameter outside expected range

'Vital' parameters are used to determine which chips can be used. A measurement outside the vital parameter range indicates a part of the chip is not working as expected. Failure to fall within the range of one or more vital parameters gives the chip a 'Cat. X' grade. For example, all digital parameters are considered vital, as a single failed digital parameter likely indicates a flaw in the chip's digital logic. 'Non-vital' parameters are used to distinguish between 'Cat. A' and 'B' chips. A chip that fails any non-vital parameter is assigned a 'Cat. B' grade. An example of a non-vital parameter is the slope measurement of the scan seen in **Figure 4a**. For a 'Cat. A' AMACStar, the slope will fall within 5% of the expected value. Such a measurement indicates good, expected performance for this test. However, a 'Cat. B' AMACStar will have a slope outside the 'Cat. A' range, but within a wider 10% range (chips with a slope outside the 10% range are graded 'Cat. X'). This kind of measurement indicates that while the functionality is working, there exist some potential imperfections that can cause significant uncertainties if the chip is used in a module.

Table 2: Probing results of individual wafers for pre-production (PP) and production priming (Priming). Note: for PP wafer 1, only small fraction of the probing tests were developed, leading to a remarkably high yield.

	Category A	Category B	Category X
PP Wafer 1	486 (99.8%)	0 (0%)	1 (0.2%)
PP Wafer 2	447 (91.8%)	26 (5.3%)	14 (2.9%)
PP Wafer 3	473 (97.1%)	6 (1.2%)	8 (1.6%)
Priming Wafer 1	447 (91.8%)	24 (4.9%)	16 (3.3%)
Priming Wafer 2	463 (95.1%)	19 (3.9%)	5 (1.0%)
Priming Wafer 3	463 (95.1%)	18 (3.7%)	6 (1.2%)
Priming Wafer 4	439 (90.1%)	25 (5.1%)	23 (4.7%)
Priming Wafer 5	458 (94.0%)	21 (4.3%)	8 (1.6%)
Priming Wafer 6	439 (91.8%)	27 (5.5%)	13 (2.7%)
Priming Wafer 7	455 (93.4%)	23 (4.7%)	9 (1.8%)
Priming Wafer 8	437 (89.7%)	24 (4.9%)	26 (5.3%)
Priming Total	3609 (92.6%)	181 (4.7%)	106 (2.7%)

Each of the grading parameters were developed using data from prototype and pre-production wafers [11]. An extensive set of 262 analog and 68 digital grading parameters was used for the eight production priming wafers and that will also be used for production. Once all of the chips

on a wafer are graded, they are plotted in a wafer map describing the individual performance of each chip and its location on the wafer. An example wafer map from production priming is shown in **Figure 5**. The yield results from probing the pre-production and production priming wafers are shown in **Table 2**. Only a subset of the total grading parameters were used for pre-production, likely leading to slightly higher yields. Based on the detector requirements, an average yield of 90% 'Cat. A' chips is required across all wafers. This result was achieved in each of the pre-production wafers as well as the entire production priming phase.

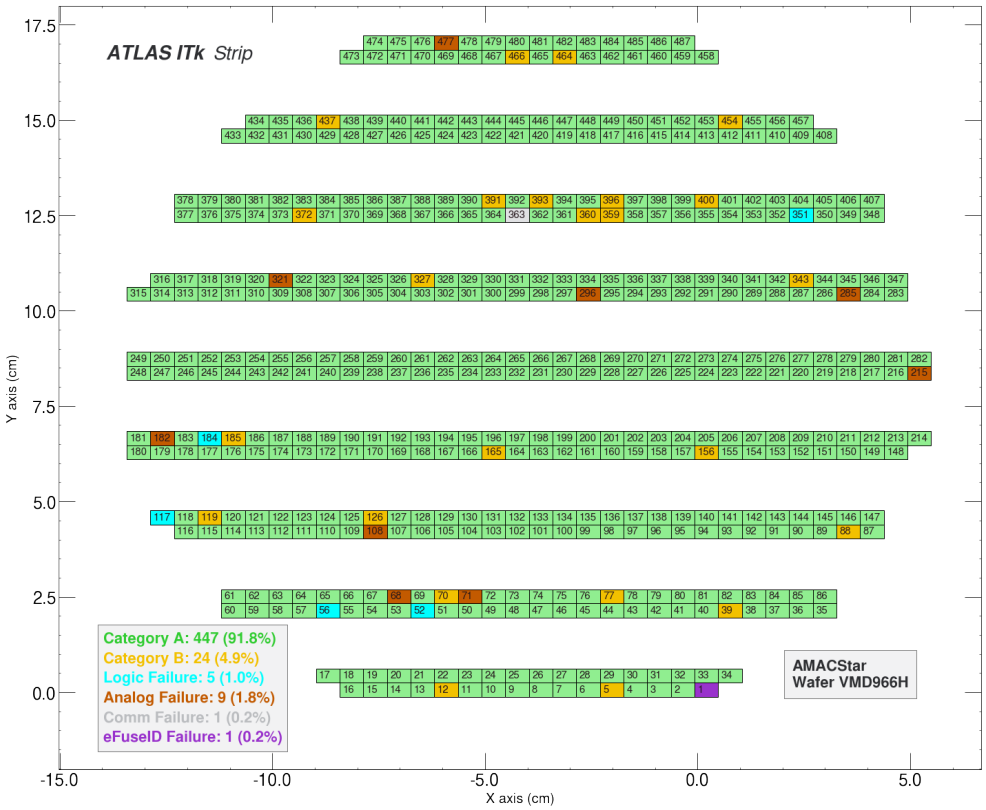

Figure 5: Wafer map of AMACStar ASICs for a single production priming wafer. The quality of each AMACStar is shown as a function of (x, y) position on the wafer. Cat. A (green) AMACStars will be used in the detector, while Cat. B (yellow) AMACStars may also be used. Cat. X AMACStars are categorized by their performance test failures: logic (cyan) analog functionality (brown), communication (grey), or programming the unique chip identifier, called the eFuse (violet). Copyright CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license, re-used with permission [10].

6 Conclusion

The HL-LHC upgrade to ATLAS will include a new inner detector, the ITk. The AMACStar chip is one of the ASICs needed for the construction of the ITk Strip subdetector. Eleven wafers of these chips have been probed, with the yield results meeting the necessary 90% threshold. Based on the

strong performance of the AMACStar (as well as the HCCStar [12]) throughout theses wafers, the next stage of production is scheduled to begin in early 2023.

Acknowledgments

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