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Hardware Design and Testing of the Generic Rear Transition Module for the Global Trigger Subsystem of ATLAS Phase-II Upgrade

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Abstract: In the framework of the ATLAS experiment's Phase-II Upgrade at the High-Luminosity Large Hadron Collider (HL-LHC), new and improved trigger hardware and algorithms will be implemented onto a single-level, 10 μs-latency architecture. The Global Trigger is a new subsystem which will bring event-filter capabilities by performing offline-like algorithms on full-granularity calorimeter data. The implementation of the functionality is firmware-focused and composed of several processing nodes, which are hosted on identical hardware, made up of an Advanced Telecommunications Computing Architecture (ATCA) front board, called Global Common Module (GCM), and a rear transition module (RTM), called Generic RTM (GRM). GRM, which was developed to mitigate the risks deriving from complex design and power management of GCM, features an advanced Xilinx Versal Prime system-on-chip and can handle communication with GCM and Front-End Link eXchange (FELIX) subsystem and trigger processors through 124 25.8 Gb/s transceiver links, for readout and control. Additionally, GRM mounts a Low-Power GigaBit Transceiver (lpGBT) chip which enables emulation of the detector front-ends for integration tests. This article proceeds from the TWEPP 2022 conference and presents the GRM hardware design and the testing of its key functionalities.

Keywords: Data acquisition circuits; Digital electronic circuits; Modular electronics; Trigger concepts and systems (hardware and software); Programmable Digital Logic Applications

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Contents

1 Introduction: the Global Trigger

As part of the ATLAS experiment's High-Luminosity Large Hadron Collider (HL-LHC)[1] trigger and data acquisition (TDAQ) "Phase-II" Upgrade [2], the single-level trigger architecture will feature new and improved hardware and algorithms, with an increased maximum rate of 1 MHz[2] and a latency of 10 μs, a new subsystem, called 'Global Trigger' (GT), will be introduced to bring event-filter capabilities to the trigger system by running offline-like (i.e. close to full reconstruction) trigger algorithms on full-granularity data [2].

The implementation of the functionalities is primarily firmware (FW)-based, and topologically factorized into three main layers, each composed of one or more nodes. The input layer aggregates bunch-crossing data from over 2700 serial channels and time-multiplexes it, so as to concentrate the complete data of every event onto a single Global Event Processor (GEP). At least 48 GEP nodes execute the actual trigger algorithms in parallel, each processing a different event. Finally, the Central Trigger Processor (CTP)-Interface layer de-multiplexes the results from the GEP nodes to the CTP, the subsystem responsible for the final trigger decision [2].

To simplify the system-level design and long-term maintenance, all the MUX, GEP and CTPI processing nodes are hosted on replicas of a single hardware platform, called the Global Common Module (GCM), whose design was presented at this conference last year (TWEPP 2021) [3]. GCM is an Advanced Telecommunications Computing Architecture (ATCA) front board designed to meet all the resource requirements of the three FW layers. It features two large Xilinx Virtex UltraScale+ XCVU13P field-programmable gate arrays (FPGA), the processing nodes, and a Xilinx Zynq UltraScale+ XCZU19EG multi-processor system-on-chip (MPSoC), for system monitor, control and readout, with many high-speed serial transceivers connections at up to 25.8 Gb/s. It is therefore a complex design which reaches close to the maximum power budget of 350 W set by cooling requirements in the ATLAS cavern. To mitigate the risks and allowing offloading some of the

[1] The HL-LHC is a major upgrade of the accelerator which will allow to deliver, starting from Run-4 (2029), more than 10 times the integrated luminosity of Runs 1-3 combined (up to 4000 fb^{-1}) [1].

[2] While the HL-LHC will increase the potential for new discoveries, it will also pose new challenges to the trigger and data acquisition (TDAQ) systems of the LHC experiments, which will have to cope with a higher throughput deriving from the increased rates of proton collisions.

functionality, a matching rear transition module (RTM), called Generic RTM (GRM) and shown in Figure 1, was also developed as a versatile rear board which can consume additional 50 W of power. GRM can handle system control and communication with the Front-End Link eXchange (FELIX) subsystem [4] and trigger processors thought optical links. Additionally, GRM can also be used as an emulator of detector front-ends, enabling early integration tests.

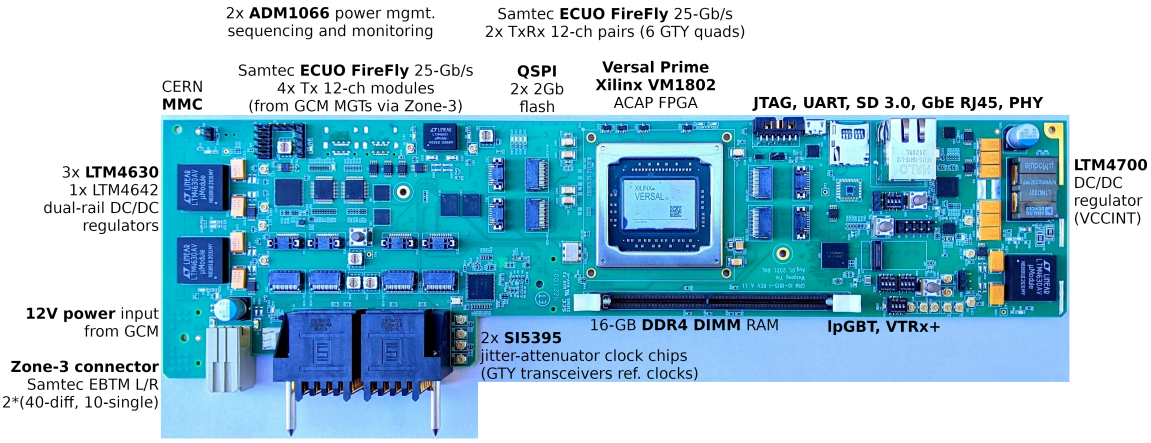

Figure 1. The Generic Rear transition Module (GRM), an ATCA RTM board composing, together with the Global Common Module (GCM), the unified hardware platform of the Global Trigger subsystem [5].

2 GRM Hardware Design

The GRM board design is centered around a Xilinx Versal Prime VM1802 adaptive computing acceleration platform (ACAP) [6]. Versal ACAPs are advanced extensible systems-on-chip (SoC) intended for heterogeneous computing, integrating, on a 7 nm-size die, processing system (PS) with Arm Cortex-A72 central processing unit (CPU), programmable logic (PL), artificial intelligence engines and DDR memory controllers (DDRMC), while a dedicated a packet-switching layer, the network-on-chip (NoC), interconnects these cores with an AXI-based interface.

As the GRM block diagram of figure 2 (right) shows, the VM1802 device was provided with many dedicated interfaces, such as Gigabit Ethernet (GbE), SD 3.0, JTAG, Universal Asynchronous Receiver-Transmitter (UART), Quad Serial Peripheral Interface (QSPI), Inter-Integrated Circuit (I2C), and 16-GB DDR4 dual in-line memory module (DIMM) RAM.

Out of 44 available GTY multi-gigabit transceivers (MGT) on the VM1802, 24 MGTs access two Tx-Rx pairs of 12-channel 25-Gb/s Samtec ECUO FireFly optical modules [7] (for communication with FELIX and other applications), and 9 Tx-Rx MGT links are connected to each processing FPGA on the GCM front board through the Zone-3 connector (Samtec ExaMAX EBTM L/R) (for monitoring, control, and data transmission). The GRM board also features 4 extra 12-channel, simplex-Tx FireFly optical modules connected to 40 Tx-only MGTs coming from GCM through the same connector, to expand the readout capacity of the front board. In total, there are 124 MGT links on GRM, all supporting 25.8 Gb/s line-rate. Their reference clocks are provided by two Skyworks SI5395 jitter-cleaning devices, whose input sources can be local oscillators, or clocks provided

by GCM, FELIX (e.g. recovered LHC clock), or the Low-Power GigaBit Transceiver (lpGBT) radiation-hard application-specific integrated circuit (ASIC).

The power is provided by a 12 V input from GCM, stepped down into the several power rails (ranging from 1.2 to 3.8 V) by 4 Analog Devices LTM DC/DC regulators, and can be monitored with 11 Texas Instruments INA226 devices via I2C. The power-on sequencing and rails health monitoring is handled by two ADM1066 chips. A CERN Module Management Controller (MMC) enables hot-swap power activation, monitoring and control, and interfaces the CERN Intelligent Platform Management Controller (IPMC) [8] card installed on GCM to monitor the health of the board and protect it from over-voltage and over-temperature.

GRM can also be used to emulate the ATLAS Phase-II subdetector front-ends, enabling early integration tests, thanks to the lpGBT ASIC. Its electrical links (eLinks) are connected to the VM1802, while the optical links (asymmetric 10.24 Gb/s Tx and 2.56 Gb/s Rx) are handled by a Versatile Link PLUS (VTRx+) radiation-hard transceiver [9], also featured on GRM.

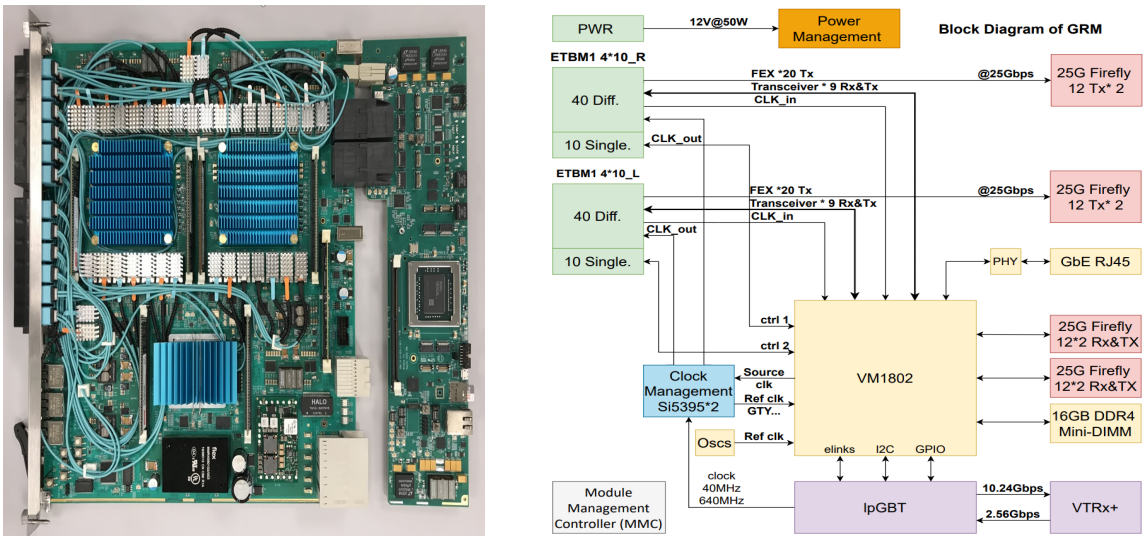

Figure 2. Left: The Global Trigger's ATCA hardware, GCM (front) and GRM (rear) boards, are connected and communicate via the Zone-3 connectors. Right: Block diagram of the GRM board, illustrating the main devices interfacing the Versal Prime ACAP [5].

3 GRM Hardware Testing

The design of GRM was validated by testing all functionality; the key items are presented here.

CPU-based configuration and monitoring After understanding the new Versal design flow, the Control, Interfaces and Processing System design was configured along with the NoC, DDRMC, and all the PS dedicated interfaces. At first, bare-metal C applications, were successfully developed and run on the ARM Cortex-A72 CPU to test the functionality of basic interfaces like UART, GbE and the DDR4 DIMM, and to configure and read out the I2C devices (such as clock chips, temperature and power sensors). Xilinx PetaLinux 2021.2 was then used to cross-compile a Linux operating system to boot on the Versal chip via SD card and modular Python3 scripts were then developed to

perform automatic power-on configuration (of SI5395 clock chips, lpGBT ASIC, FireFly modules, etc.), as well as controlling and monitoring of power consumption and thermal performances via the multiple I2C devices such as INA226 and TMP435.

FPGA PL and Transceiver tests Transceiver designs were successfully implemented for all the MGT quads of the VM1802, and programmed onto the FPGA via JTAG. Integrated bit-error-ratio tests (IBERT) with 31-bit pseudo-random bit sequence (PRBS) patterns were used to evaluate signal integrity; firstly, in internal physical-medium-attachment loopback tests on all the 44 GTY MGTs, at both 12.8 and 25.8 Gb/s line-rates; secondly, in external loopback through the 2 Tx-Rx pairs of 14-Gb/s and 25-Gb/s FireFly optical modules, at 12.8 Gb/s and 25.8 Gb/s line-rates respectively. In all cases, all links run error-free with observed BER < 1E-13. Table 3 provides examples of typical performances and Figure 3 shows a typical eye diagram for 25.8 Gb/s loopback.

GTY Link		**Open area**	
Quad	**MGT**	**12.8 Gb/s**	**25.8 Gb/s**
106	0	6848	4865
205	0	7360	5184
206	0	8000	6080
Average		7900	5380

Table 1. An example of typical performances for three quads and channels; the eye for 12.8 Gb/s operation is larger than it is for 25.8 Gb/s, and the open area is inversely correlated to the length the links' PCB tracks.

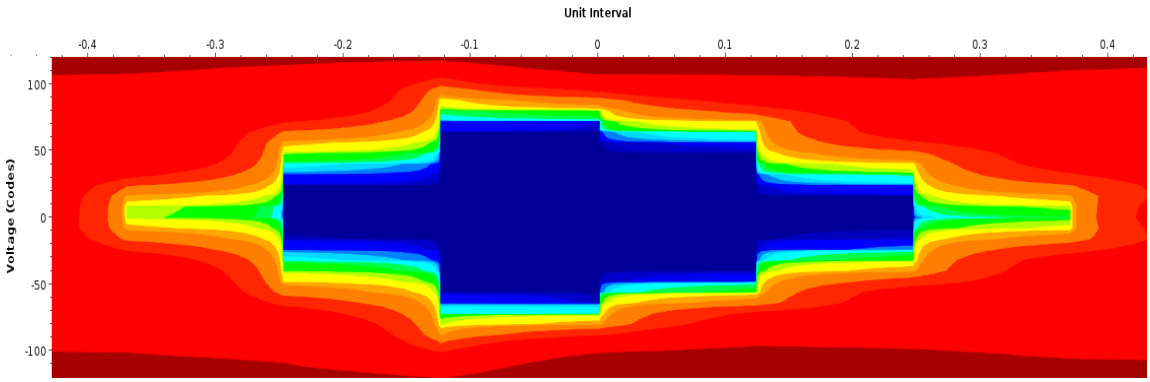

Figure 3. Typical eye diagram for the VM1802 GTY transceivers at 25.8 Gb/s optical loopback using a 20-meter fiber and a 25-Gb/s FireFly module connected to quad 205. The color-map represents the BER, from 1E-1 (dark red) down to 1E-9 (dark blue), for which the open area is 5184 [5].

lpGBT tests The lpGBT ASIC will be featured on several Phase-II detector front-ends. In order to exercise its operation and enable early integration tests, it was also added to the GRM design, and was then validated as follows: Following configuration of the lpGBT ASIC, to work in transceiver and simplex-Tx/Rx modes, via I2C (VM1802 as master) and then also optical interface ("IC" mode, using a FELIX BNL-712 board as master), up-link and down-link aligned successfully, confirming functionality of the asymmetrical optical links between the VTRx+ and FireFly modules; The

lpGBT general-purpose input/output (GPIO) links, connected to GPIOs of the VM1802, were configured at different settings and found functional; I/O eLinks between Low-Voltage Differential Signaling (LVDS) pins of the VM1802 and the CERN Low Power Signalling (CLPS) pins of the lpGBT where checked and proved the two differential physical-layer standards to be compatible; Then, complete up-link and down-link loopback, through both eLinks and optical links (via VTRx+ and FireFly), could finally be achieved, as described in figure 4.

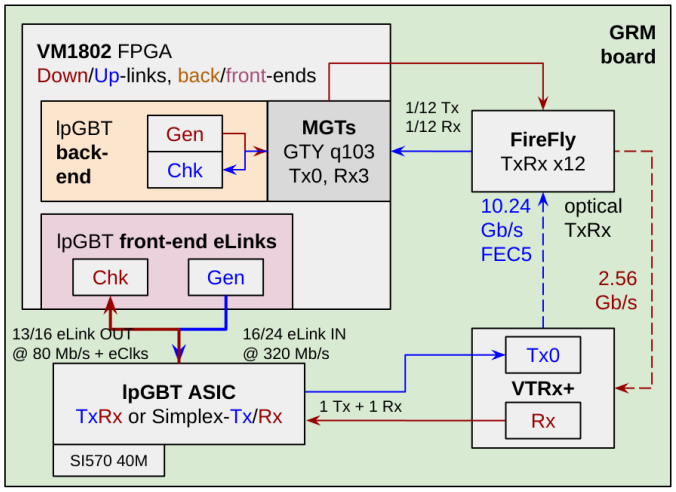

Figure 4. Testing of lpGBT with VM1802 on GRM. Down-link (red): PRBS data is generated at VM1802, encoded, scrambled and transmitted to the lpGBT at 2.56 Gb/s through GTY transceiver, FireFly optical module and VTRx+ connector; the lpGBT ASIC decodes and distributes the data to the output eLinks (CLPS) reaching the VM1802, where data is checked. Up-link (blue): raw data is generated by VM1802 logic on the input eLinks (LVDS); lpGBT collects and encodes the data, which is then optically looped back (via VTRx+ and FireFly) to the VM1802 at 10.24 Gb/s, where it is decoded, descrambled and checked [5].

4 Conclusions and Outlook

The GRM board design, fabrication and testing have been completed successfully. The hardware functionalities and critical technologies featured on GRM have been validated, and a first-time demonstration of Versal-lpGBT interfacing was achieved. As both devices will play crucial roles in ATLAS TDAQ for a long time, this experience on GRM will also be valuable to other projects (among which the next revisions of GCM and FELIX hardware at Brookhaven National Laboratory).

Acknowledgments

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