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# **Test of ITk 3D sensor pre-production modules with ITkPixV1.1 chip**

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- $_{21}$  Abstract: ITk detector, the new ATLAS tracking system at High Luminosity LHC, will be equipped
- with 3D pixel sensor modules in the innermost layer (L0). The pixel cell dimensions will be either
- 23 25×100  $\mu$ m<sup>2</sup> (barrel) or 50×50  $\mu$ m<sup>2</sup> (endcap), with one read-out electrode at the centre of a pixel
- 24 and four bias electrodes at the corners. Sensors from pre-production wafers  $(50 \times 50 \ \mu m^2)$  produced
- by FBK have been bump bonded to ITkPixV1.1 chip at IZM. Bare modules have been assembled
- in Genoa on Single Chip Cards and characterized in laboratory and at test beam.
- Keywords: Hybrid detectors; Radiation-hard detectors; Particle tracking detectors (Solid-state
- detectors); Detector design and construction technologies and materials

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## <sup>29</sup> **Contents**



# <span id="page-1-0"></span><sup>43</sup> **1 Introduction**

 In the next years, the Large Hadron Collider (LHC) will be upgraded (High Luminosity LHC [\[1\]](#page-8-1)) 45 to reach higher instantaneous luminosity, up to  $7.5 \cdot 10^{34}$  cm<sup>-2</sup> s<sup>-1</sup>. To cope with the higher particle rate, hit occupancy and radiation damage, the ATLAS detector [\[2\]](#page-8-2) will be updated as well: in particular, its tracking system will be completely replaced by a new all-silicon detector (Inner Tracker, ITk), to be installed during the Long Shutdown 3 (2026-2028). ITk will consist of a Pixel detector [\[3\]](#page-8-3) at small radius and a large area Strip detector [\[4\]](#page-9-0) surrounding it. In particular, the <sup>50</sup> innermost layer (L0) of the Pixel detector will face a non ionising fluence up to  $2 \cdot 10^{16}$  n<sub>eq</sub>/cm<sup>2</sup> and a ionising dose up to 1 Grad. After several years of R&D [\[5\]](#page-9-1), 3D sensors were chosen for the L0 pixel modules, with a square <sup>53</sup> pixel cell (50×50  $\mu$ m<sup>2</sup>) in the endcap rings modules and a rectangular pixel cell (25×100  $\mu$ m<sup>2</sup>) in

<sup>54</sup> the barrel ones. 3D sensors diced from previous batches of wafers produced by FBK (Fondazione <sup>55</sup> Bruno Kessler) [\[6](#page-9-2)[–8\]](#page-9-3) were bonded to the FE-I4 [\[9\]](#page-9-4) or RD53A [\[10\]](#page-9-5) readout chips: these prototype

<sup>56</sup> modules were characterized in laboratory and beam test [\[11,](#page-9-6) [12\]](#page-9-7) up to a fluence of 1·10<sup>16</sup> n<sub>eq</sub>/cm<sup>2</sup>.

<sup>57</sup> The results collected on prototypes have demonstrated the validity of the technology in the ITk <sup>58</sup> detector conditions: to move forward, pre-production has been launched.

<sup>59</sup> In this paper, we report on the characterization of the modules assembled with the first pre-<sup>60</sup> production 3D sensors produced by FBK bonded to ITkPixV1.1 chips, including laboratory char-

61 acterization and beam test results of unirradiated samples.

# <span id="page-2-0"></span><sup>62</sup> **2 ITk Pixel modules**

 $63$  The latest ITk Pixel detector layout [\[13\]](#page-9-8) includes 5 layers of pixel in the barrel and several disks  $64$  in the endcap. The two innermost layers (L0 and L1 barrel layers, together with R0, R0.5 and R1 <sup>65</sup> rings) will make up the Inner System (see Figure [1\)](#page-2-1), which is planned to be replaced after about <sup>66</sup> 2000 fb<sup>-1</sup>. Hybrid pixel modules will be glued to carbon support structures. Quad-modules (one  $67$  bare module, with four chips bonded to a planar sensor, glued to a flexible PCB) will be hosted in 68 the external layers (L1-4): 150  $\mu$ m planar sensors in L2-4 (Outer Barrel and Outer Endcap), while 69 100  $\mu$ m planar sensors in L1, R1 and R0 (Inner System, Figure [2,](#page-3-1) left).



<span id="page-2-1"></span>**Figure 1**. ITk Pixel detector layout, 3 sub-sections outlined: Outer Barrel, Outer Endcap and Inner System.

 Triplet modules (three separate bare modules, each with a 3D sensor bonded to a chip, glued to a flexible PCB) will be at 34 mm from collisions (L0) in the barrel or down to 33.2 mm (R0) in the endcap (Figure [2,](#page-3-1) left). A total of 288 (900) 3D sensors are needed to equip the triplet modules in the barrel (rings). In particular, there will be 12 L0 staves (barrel) with 8 triplets each, and two type of rings (endcap): 30 R0 rings, with 6 triplet modules and 20 planar modules each, and 12 R0.5 rings with 10 triplet modules each. The number of carbon supports, triplet modules and 3D

<sup>76</sup> sensors needed is summarized in Table [1.](#page-2-2)

	<b>Supports</b>	Triplets per support Total triplets		Total 3D sensors   Pixel cell $\lceil \mu m^2 \rceil$	
	12 staves		96	288	$25\times100$
R <sub>0</sub>	30 rings		180	540	$50\times50$
R0.5	12 rings		l 20	360	$50\times50$

<span id="page-2-2"></span>**Table 1**. Number of carbon supports, triplet modules and 3D sensors in the ITk detector.

 The ITk detector project just completed the prototyping phase: prototype carbon supports equipped with services and RD53A modules have been built and tested. A R0 ring prototype equipped with RD53A modules can be seen in Figure [2,](#page-3-1) right. The community is now moving towards the detector production: an intermediate step, the pre-production, is currently ongoing.

81 Details about pre-production of FBK 3D sensors and ITkPixV1.1 chips are given below.



<span id="page-3-1"></span>**Figure 2.** Left: L0, R0 and R0.5 supports for triplet modules. Right: Prototype of R0 ring carbon support with RD53A modules, one side loaded with 10 quad-modules and 3 triplets.

#### <span id="page-3-0"></span><sup>82</sup> **2.1 3D sensor**

83 Pre-production 3D sensors are being produced by FBK, SINTEF and CNM foundries. The sensors <sup>84</sup> of interest for this report (50×50  $\mu$ m<sup>2</sup>) have been produced on 6 inches wafer (24 sensor each, <sup>85</sup> Figure [3,](#page-3-2) left) designed at the University of Trento and fabricated at FBK (Trento, Italy). The 86 3D pixel is built in single-sided technology with columns etched in a 150  $\mu$ m active layer (high-resistivity p<sup>-</sup>), bonded to a 500-μm thick low-resistivity (p<sup>++</sup>) handle wafer (Figure [3,](#page-3-2) right). The 88 handle wafer is thinned to ∼100  $\mu$ m after dicing and before flip-chip bonding to the readout chip. 89 The ohmic (p<sup>+</sup>) columns pass through the active layer and penetrate the handle wafer to facilitate <sup>90</sup> the bias from the backside. The readout (n<sup>+</sup>) columns stop about ∼20  $\mu$ m before the end of the 91 active layer. A p-spray layer (not shown in the Figure) isolates the n<sup>+</sup> columns at the surface. The 92 n<sup>+</sup> column is connected to the bump pad through a contact, these surface details can be seen in <sup>93</sup> Figure [4:](#page-4-2) left, the layout of the cell and right, photo of the surface of a pre-production wafer pixel <sup>94</sup> cell.



<span id="page-3-2"></span>**Figure 3.** Left: six inches FBK pre-production wafer with 24 sensors (and test structures at the periphery). Right: schematic cross section of 3D pixel sensor built in single-side technology.



<span id="page-4-2"></span>**Figure 4**. Left: 3D pixel cell layout. Right: surface of a pixel cell from FBK pre-production wafer. The bump pad observed in wafer is smaller due to an error in the in the pre-production layout, that was fixed later.

## <span id="page-4-0"></span>**2.2 ITkPixV1.1 chip**

 After the positive experience gained by testing planar and 3D sensor modules with RD53A chip, a new common library has been prepared, so-called RD53B [\[14\]](#page-9-9), to develop the final layout of the 98 ATLAS (ITkPixV1) and CMS (CROC v1) readout chips. The first version of the ATLAS chip, ITkPixV1.0, was submitted in March 2020. This very first version presented a problem with Time over Threshold (ToT), which caused a significant increase in current and made it impossible to use for data taking. An updated version, ITkPixV1.1, was submitted in 2021: the issue with the ToT has been overcome by disabling it with simple changes in the more external wafer layer.

103 Several ITkPixV1.1 wafers were produced, probed, thinned (to 150  $\mu$ m) and diced: a 80% green yield is achieved. ITkPixV1.1 is still a prototype, the final version of the chip, ITkPixV2, will be submitted at the end of 2022.

106 ITkPixV1 chip has a matrix of  $50 \times 50 \ \mu m^2$  pixels, with 384 rows and 400 columns. A total 107 area of about  $2 \times 2$  cm<sup>2</sup>, with a power dissipation of about 0.5 W/cm<sup>2</sup>. The discrimination threshold can be set to 1000 *e* (target value), but it is possible to tune to lower values: 600 *e* without noisy pixels, 400 *e* with 1% noisy pixels. The properties of ITkPixV1 chip have been studied in depth, 110 also with irradiation up to 1 Grad  $[15]$ .

#### <span id="page-4-1"></span>**3 Samples**

 Five pre-production wafers have been delivered by FBK to CERN in 2021. Among them, 20 sensors were diced out and flip-chipped at IZM to ITkPixV1.1 chips: these early modules have been tested for sensor pre-production quality assessment. Six of these modules have been assembled in Genoa on dedicated PCBs that host a single module/chip: Single Chip Cards (SCCs). Tests executed in INFN Genoa laboratory on the six samples are documented in section [3.1,](#page-5-0) while results 117 of measurements performed at CERN beam facilities on SCC 2 and 4 are described in section [3.2.](#page-6-0)

## <span id="page-5-0"></span>**3.1 Laboratory test**

 The tests executed in INFN Genoa laboratory includes: sensor IV, chip threshold tuning and data acquisition with X-rays.

## <span id="page-5-1"></span>**3.1.1 Sensor IV**

 Sensor IV was previously measured at sensor level (on wafer) in Trento, then on bare module (assembled on SCC) in Genoa. Measurements at room temperature are performed up to 80 V bias, then scaled to 20 $\degree$ C for comparison. For all the six samples, the leakage current at 25 V (20 V higher than the depletion voltage, assumed to be around 5 V) is always below 0.05  $\mu$ A/cm<sup>2</sup>, much lower than the technical requirement:  $2.5 \mu A/cm^2$ . The results obtained on wafer (red) and on SCC 127 (blue) for one of the samples assembled in Genoa can be seen in Figure [5.](#page-5-4) The minor increase of the leakage current at bare module level is not considered worrisome, it may be due to the hybridization steps (wafer dicing, flip-chip).



<span id="page-5-4"></span>**Figure 5**. IV measured on the same sensor directly on wafer (red) and on bare module mounted on SCC 8 (blue). Room temperature measurements: the leakage current values have been scaled to  $20^{\circ}$ C.

## <span id="page-5-2"></span>**3.1.2 Threshold tuning**

<sup>131</sup> The threshold tuning has been executed with a YARR DAO system [\[16\]](#page-9-11) with sensor bias of 10 V. The target threshold was set to 1000 *e*: an homogeneous distribution was achieved on all samples, with a threshold dispersion of about 30 *e*. The corresponding noise was observed to be ∼70 *e* on modules with sensor (10 V bias), to be compared to ∼40 *e* observed on bare chip. As expected, the noise decreases by increasing the bias voltage (Figure [6\)](#page-6-1): it reaches a plateau at about 6 V: this suggests that the sensor is completely depleted at this bias voltage.

# <span id="page-5-3"></span>**3.1.3 X-ray data taking**

 A 60 second long self-trigger scan with X-rays from Amptek Mini-X2 is performed to qualify the data acquisition capability. In these conditions (tube powered at 50 kV and 80 uA, with the tip at 15 cm from the module), about 6700 hits/pixel in 60 seconds (110/pixel/s) are collected by the inner



<span id="page-6-1"></span>**Figure 6**. Threshold noise decreasing versus bias voltage: a plateau is reached at about 6 V. The standard deviation of the threshold noise distribution is reported as the uncertainty.

<sup>141</sup> pixels of the matrix (Figure [7,](#page-6-2) left), while the edges pixels, both horizontal and vertical, recorded

<sup>142</sup> about 30% more hits (Figure [7,](#page-6-2) left). This is explained by the fact that the electric field that collects <sup>143</sup> the charge in the edges pixels extends partly also in the slim edge region of the sensor (Figure [7,](#page-6-2) <sup>144</sup> left).



<span id="page-6-2"></span>**Figure 7.** Left: Hit occupancy with 60 s long X-ray scan. Right: edges pixel cells, with 150  $\mu$ m of additional ohmic columns before the dicing line.

## <span id="page-6-0"></span><sup>145</sup> **3.2 Beam test**

146 During Spring 2022, two test beam campaigns have been performed to study the performance of the 147 unirradiated modules on the beam. The first campaign took place at the PS (12 GeV protons), then <sup>148</sup> the setup was moved to the SPS (about 120 GeV pions). The setup included a telescope with six <sup>149</sup> MIMOSA26 [\[17\]](#page-9-12) planes and a FE-I4 chip module as a timing reference plane. The data acquisition  system was YARR and EUDAQ based. The coincidences of two scintillators, placed at the two ends of the telescope, were used to generate the trigger signal for the readout, distributed to telescope planes and Devices Under Test (DUTs) by a Trigger Logic Unit (TLU).

 At the PS facility, data were collected supplying the DUT sensor with a bias of 1, 2, 4, 6 and 10 V, while at SPS data were taken only with a bias of 0 and 10 V. SCC 2 was tested only at the PS, while SCC 4 in both facilities. The SCCs, tuned to a 1000 e threshold, were perpendicular to the beam inside an aluminum coldbox. Data have been analyzed using the Corryvreckan [\[18\]](#page-9-13) framework. Data in EUDAQ-native raw format were loaded on Corryvreckan, the noisy pixels were masked on each device, then the telescope planes were aligned, followed by the DUTs. Finally, the resolution and efficiency of DUTs were measured.

#### <span id="page-7-0"></span>**3.2.1 Resolution**

 Since the ToT reading was disabled for the ITkPixV1.1 chip, only binary read-out is possible. Therefore the expected resolution ( $\sigma$  = pitch/ $\sqrt{12}$ ) for the 50×50  $\mu$ m<sup>2</sup> pixel cell is about 14  $\mu$ m in 163 both the X and Y directions. The residuals RMS observed at the SPS is about 13  $\mu$ m, as expected, 164 while at the PS it is higher (20-25  $\mu$ m): this could be explained by the lower particle beam energy at PS, which increases the multiple scattering due to the aluminum walls of the cooling box.

#### <span id="page-7-1"></span>**3.2.2 Efficiency**

 Several runs were collected for each bias voltage point: for each point, the mean value and the standard deviation of the efficiency are extracted by a Gaussian fit to the distribution of the results obtained in each run. At PS, the efficiency was always higher than 97%. At SPS, the efficiency is 170 already (98.6 $\pm$ 0.1)% with a bias voltage of 0 V, reaching (98.9 $\pm$ 0.1)% with a bias of 10 V (Figure [8,](#page-7-2) 171 left). The efficiency is almost 100% in the central part of the pixel cell,  $(99.91\pm0.02)\%$  at 10 V, while in the corner it is lower, down to 75% (Figure [8,](#page-7-2) right). The inefficiency zone, due to the <sup>173</sup> p<sup>+</sup> columns (max 4  $\mu$ m radius), extends for about 10  $\mu$ m in both 0 and 10 V bias (Figure [9\)](#page-8-4). The efficiency in the dead area due to the p<sup>+</sup> columns is expected to be of 0%: the effect is smeared by the telescope resolution (∼5 μm), that likely also makes the size of the region with lower efficiency to appear larger than its true value.



<span id="page-7-2"></span>**Figure 8**. Left: Efficiency versus bias voltage at PS and SPS. Right: Pixel cell efficiency at 10 V (SPS data).



<span id="page-8-4"></span>**Figure 9.** Projection of the first 1  $\mu$ m along the X direction of the pixel local efficiency map at 0 and 10 V bias (SPS data): the inefficiency zone due to the  $p^+$  columns (max 4  $\mu$ m radius) extends for about 10  $\mu$ m.

# <span id="page-8-0"></span>**4 Conclusion**

 ITk detector, the new ATLAS tracking system at High Luminosity LHC, will be equipped with 3D pixel sensor modules in the innermost layer. Sensors from pre-production wafers produced by

FBK have been bump bonded to ITkPixv1.1 chip. Bare modules have been assembled in Genoa on

Single Chip Cards and characterized in laboratory and with beam at CERN facilities.

The leakage current is well below 0.2  $\mu$ A/cm<sup>2</sup> in the considered bias voltage range (0-80 V). At 10 V bias, an average noise of 70±10 *e* has been observed after tuning the threshold to 1000 *e*. The edges pixels record about 30% more hits than pixels in the center of the matrix, due to the extension of the electric field in the slim edge. Hit detection efficiency higher than 97% has been measured on modules before irradiation already at 0 V bias.

<sup>187</sup> Two devices has been irradiated with protons up to  $1 \cdot 10^{16}$  n<sub>eq</sub>/cm<sup>2</sup> fluence and 1 Grad dose, characterization with the beam is ongoing at SPS.

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The test beam measurements were performed at the CERN Test Beam Facility (PS and SPS).

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