Integration and Commissioning of the ATLAS Tile Demonstrator Module for Run 3

F. Carrió on behalf of the ATLAS Tile Calorimeter System

***Abstract*—The Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS experiment at Large Hadron Collider (LHC). The LHC will undergo a series of upgrades leading into the High Luminosity LHC (HL-LHC). The TileCal Phase-II Upgrade will accommodate the detector readout electronics to the HL-LHC conditions using a new clock and readout strategy.**

The TileCal Phase-II upgrade project has undertaken an extensive R&D program. A Demonstrator module containing the upgraded on-detector readout electronics was built in 2014, evaluated during seven test beam campaigns, and inserted into the ATLAS experiment in 2019. This module will be operated in the ATLAS experiment during Run 3 (2022–2026) through a Tile PreProcessor (TilePPr) Demonstrator board implementing the clock and readout architecture envisioned for the HL-LHC. The TilePPr also provides backward compatibility of the Demonstrator module with the present ATLAS Trigger and Data AcQuisition and the Timing, Trigger and Control systems.

This paper describes the hardware and firmware for the implementation of the data acquisition system of the Demonstrator module and discusses the results of the integration tests performed during the commissioning of the Demonstrator module for Run 3.

***Index Terms*—ATLAS Tile Calorimeter(TileCal), Data Acquisition (DAQ) systems, Field-Programmable Gate Array (FPGA), High Energy Physics, High-Speed Electronics.**

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I. Introduction

THE Tile Calorimeter (TileCal) [1] is the central hadronic calorimeter of the ATLAS experiment [2], covering a pseudorapidity of $\eta < |1.7|$. TileCal is a sampling calorimeter made of steel plates and scintillator material, and it contributes to the measurement of jets, tau leptons, and missing transverse energy ($E_{\mathrm{T}}^{\mathrm{miss}}$).

TileCal is composed of three cylindrical barrels along the beam axis, which are divided into four readout sections: the central Long Barrel (LBA, LBC) and two Extended Barrels (EBA, EBC). Each barrel comprises 64 wedge-shaped modules distributed azimuthally as shown in Fig. 1.

The light produced by a charged particle crossing the calorimeter are carried by Wave-Length Shifting (WLS) fibers to photomultiplier tubes (PMTs). The complete readout of the detector is done using approximately 10,000 PMTs.

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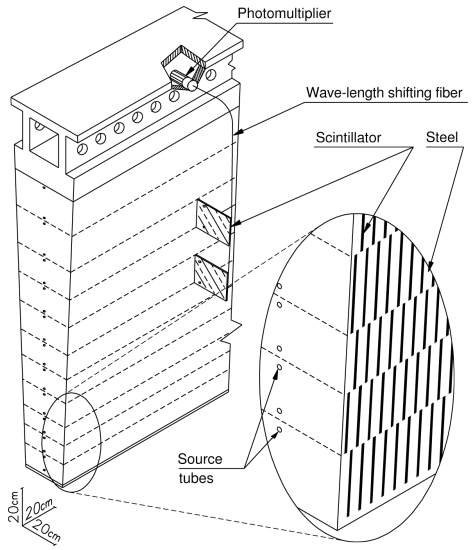

Fig. 1: Detail of a Tile module showing the 11 radial layers of scintillator tiles interleaved with the steel absorber, and the position of the PMTs and readout electronics.

In the on-detector electronics, the analog PMT signals are shaped with a 7-pole LC shaper, amplified with two gains (1:64 ratio), and digitized with 10-bit Analog-to-Digital Converters (ADCs), before being stored in pipeline memories. The low-gain PMT signals are also analog summed into pseudo-projective trigger towers and transmitted to the ATLAS trigger system via electrical cables.

Once the TileCal modules receive a trigger acceptance signal from the ATLAS trigger system, the selected events are transmitted off-detector to the Read-Out Drivers (ROD) [3] via optical fibers. The RODs reconstruct the energy and time per channel, and transmit all the processed data to the next elements in the ATLAS DAQ chain after the first-level trigger.

II. TileCal Phase-II Upgrade

During the Long Shutdown 3 (2026–2029) the Large Hadron Collider (LHC) will be upgraded towards the High-Luminosity LHC (HL-LHC). The HL-LHC will deliver an instantaneous peak luminosity up to $7.5 \times 10^{-34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$, and a total integrated luminosity of 4000 fb^{-1} by the end of its data-taking (2029–2040). The ATLAS Phase-II Upgrade [4] will prepare all the subdetectors in order to operate under the new conditions imposed by the HL-LHC.

TileCal will undergo a series of upgrades during the ATLAS Phase-II Upgrade where both the on-detector and off-detector

readout electronics will be replaced introducing a new readout strategy. This new readout architecture will enable the transmission of full-digital data with fine granularity information to the ATLAS trigger system.

The TileCal on-detector readout electronics will transmit detector data to the off-detector electronics per every bunch crossing (25 ns). In the off-detector electronics, the Tile PreProcessor (TilePPr) [5] modules will reconstruct cell energies per bunch crossing transferring the results to the Trigger and Data Acquisition Interface (TDAQi) boards. The TDAQi boards will use the reconstructed cell energies to build trigger objects for the ATLAS calorimeter trigger system.

The TilePPr modules will store the samples and reconstruct energy per channel in pipeline memories, until the reception of a trigger acceptance signal when the event is transmitted to the ATLAS Front End LInk eXchange (FELIX) [6] system.

III. THE TILE DEMONSTRATOR MODULE

A full-size Demonstrator module was built as part of TileCal Upgrade R&D program. This module was constructed in 2014 with the latest version of the readout electronics designed for the HL-LHC.

This module implements the clock and readout strategy for the HL-LHC but keeping at the same time backward compatibility with the current system by transmitting triggered data to the RODs, and analog trigger towers to the ATLAS trigger system.

A. Mechanics

The Demonstrator module is composed of four independent mechanical structures, called mini-drawers (Fig. 2). Each mini-drawer is an aluminum substructure with one MainBoard [7], one DaughterBoard v4 [8], one high voltage distribution board, and up to 12 PMT blocks.

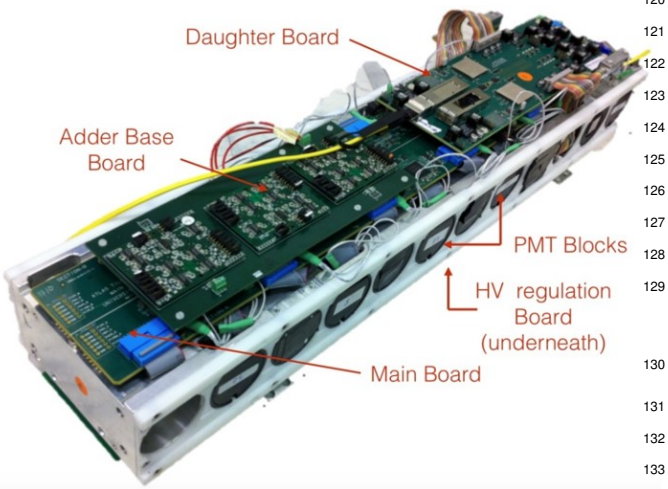

Fig. 2: Picture of one of the mini-drawers of the Tile Demonstrator [4].

B. On-detector electronics

Each PMT block is equipped with one upgraded 3-in-1 card (Fig. 3) which shapes and amplifies the PMT signals with two gains (1:32 ratio). The upgraded 3-in-1 cards provide additional capabilities as a calibration circuit to calibrate the electronics over the full dynamic range, and an integrator circuit for luminosity measurements and Cesium calibration.

As in the current system, the lower gain signals are summed in the adder cards into trigger towers, and transmitted to the ATLAS trigger system. This feature ensures backward compatibility with the current ATLAS trigger system.

Fig. 3: Picture of a upgraded 3-in-1 card.

The MainBoards (Fig. 3) are responsible for the digitization of the PMT signals, and the configuration of the upgraded 3-in-1 cards. Each MainBoard is equipped with twelve dual 12-bits ADCs to digitize the two gain signals coming from 12 PMTs, twelve 16-bit ADCs to read out the integrator signal, and four Intel Cyclone IV FPGAs for configuration and control of the upgraded 3-in-1 cards. The analog PMT signals are digitized for every bunch crossing, and the digitized data is transferred to the DaughterBoards.

Fig. 4 shows a picture of the DaughterBoard v4 installed in the Demonstrator module. The DaughterBoards are responsible for transmission of the readout data to the off-detector electronics, as well as for the reception and distribution of the timing control and configuration commands for the operation of the on-detector electronics. Each DaughterBoard is equipped with two Xilinx Kintex-7 XC7K160T FPGAs for the data acquisition and processing tasks, two GBTx [9] ASICs for the recovery of the accelerator clock, and two QSFP optical modules for the communication with the off-detector electronics.

C. Off-detector electronics

The Tile PreProcessor Demonstrator [5] is the core element of the off-detector electronics, acting as a bridge between the Demonstrator module and the current ATLAS TDAQ system. The TilePPr Demonstrator receives and decodes detector data from the Demonstrator module for every bunch crossing, sending the triggered data to the legacy ROD and to the FELIX system. It is also responsible for the propagation of

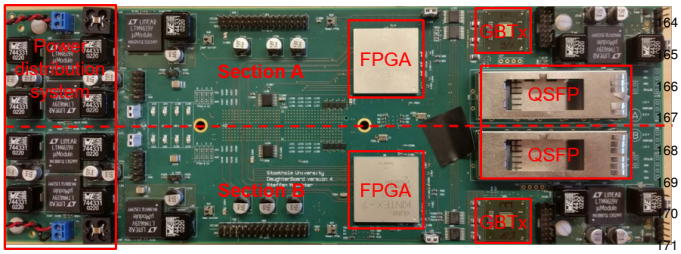

Fig. 4: Picture of the DaughterBoard v4 installed in the Demonstrator module.

the accelerator clock and configuration commands towards the on-detector electronics received from the Trigger, Timing, and Control (TTC) system.

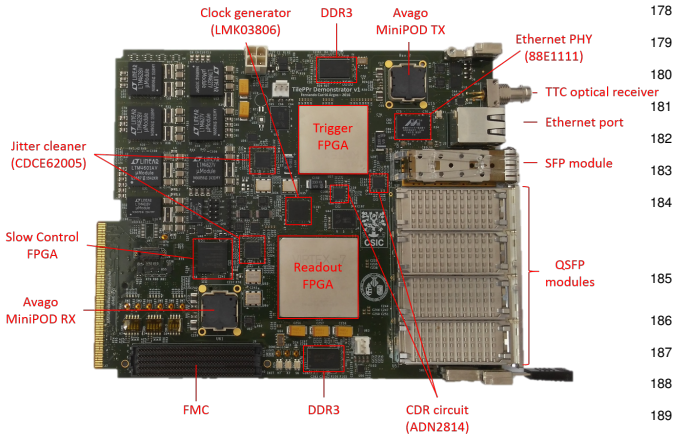

Fig. 5: Picture of the Tile Preprocessor Demonstrator.

The TilePPr Demonstrator [5] is a double mid-size Advanced Mezzanine Card form factor compliant with the AdvancedTCA standard. The TilePPr Demonstrator (Fig. 5) hosts one Xilinx Virtex-7 XC7VX415T and one Kintex-7 XC7K420T FPGAs, four QSFP modules, DDR3 memories, and two Texas Instruments CDCE62005 jitter cleaners. The Virtex-7 FPGA is connected to the four QSFP modules for the communication with the on-detector electronics, implements all the firmware modules for the readout and operation of one TileCal module, and communicates with the legacy ROD and FELIX systems and with the TTC system. The Kintex-7 FPGA is devoted for the study and evaluation of pre-processing trigger algorithms for the HL-LHC.

IV. Clock and Data Readout Architecture Implementation

The Demonstrator module implements the clock and readout architecture for the HL-LHC, keeping backward compatibility with the current TDAQ system. Fig. 6 presents a block diagram with the firmware blocks implemented in the Demonstrator module and the TilePPr Demonstrator module.

A. High-speed communication path

A total of 16 high-speed links are implemented using the GigaBit Transceiver (GBT) protocol [10] to communicate the DaughterBoards and the TilePPr Demonstrator with a fixed and deterministic latency operation.

The GBT links operate at 4.8 Gbps in the downlink direction (from off-detector to on-detector), and are used to distribute the configuration commands and the accelerator clock to the Demonstrator module. In the uplink direction (from on-detector to off-detector) the GBT links operate at 9.6 Gbps and are used to acquire detector samples at the bunch crossing frequency.

B. Configuration blocks

The TilePPr Demonstrator receives the configuration commands for the Demonstrator from two different paths: from the TTC system and from the ATLAS TDAQ software via a GbE port using the IPbus protocol [11].

The configuration commands received from the TTC system are decoded in the TilePPr Demonstrator and transmitted to the DaughterBoards via four downlinks. Then, the DaughterBoards distribute the configuration commands to MainBoard FPGAs, which finally configures the upgraded 3-in-1 cards.

C. Clock and data readout path

Each DaughterBoard deserializes the data coming from 6 dual-channel ADCs for every bunch crossing, and builds a data packet which is transmitted to the TilePPr Demonstrator together with the integrator and monitoring data. This data is transferred to off-detector via 4 uplinks per DaughterBoard (16 uplinks in total).

The TilePPr Demonstrator decodes the data packets storing the integrator, monitoring and detector samples in pipeline memories with a maximum depth of 10 μs. The data samples are stored in circular pipeline buffers until the reception of a trigger acceptance signal from the ATLAS trigger system. Then, the selected events are transmitted to the ROD system ensuring backward compatibility with the current TDAQ system.

For the clock distribution towards the Demonstrator module, the TilePPr Demonstrator transmits the accelerator clock via downlinks embedded with the configuration commands. The TilePPr Demonstrator recovers the accelerator clock from the current TTC system, and obtains a low-jitter version of the accelerator clock using and on-board jitter cleaner (Texas Instruments CDCE62005). The cleaned copy of the accelerator clock is used to drive the FPGA high-speed transceivers. Finally in the on-detector electronics, the accelerator clock is recovered via a GBTx ASIC located in the DaughterBoards and distributed to the MainBoard as a sampling clock for the ADCs.

V. Test Beam Results

The performance of the Demonstrator module was studied during seven test beam campaigns between 2015 and 2018 in the H8 beam line of the Super Proton Synchrotron (SPS) accelerator at CERN, where it was exposed to electron, hadron

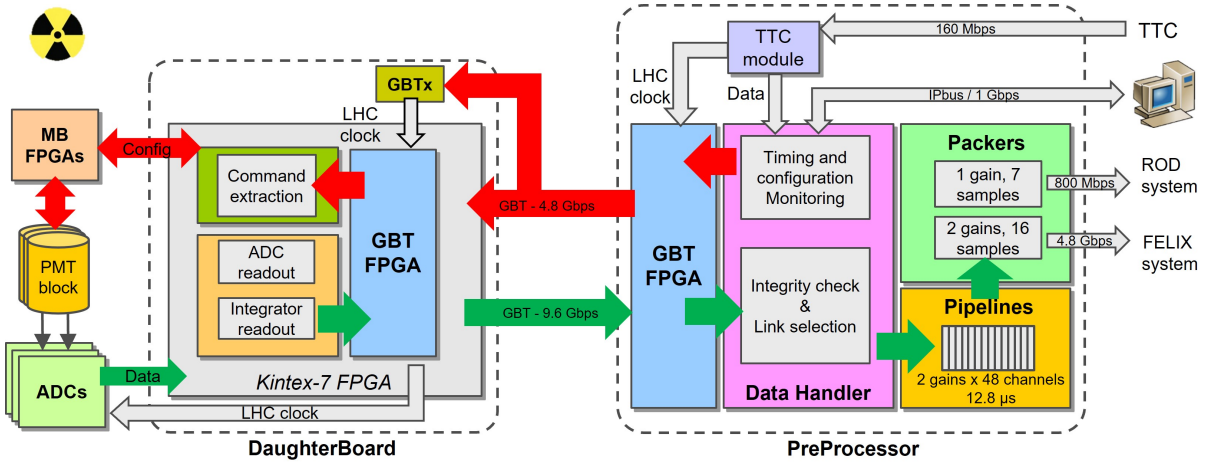

Fig. 6: Block diagram of the main blocks used for the implementation of the Demonstrator data acquisition system.

and muon beams with different energies and incident angles. The purpose of these test beam campaigns was the validation of the new readout electronics for the HL-LHC. Fig. 7 shows the distribution of the total energy deposited in the Demonstrator module for different electron beam energies (20 GeV, 50 GeV, and 100 GeV) using experimental and simulated data.

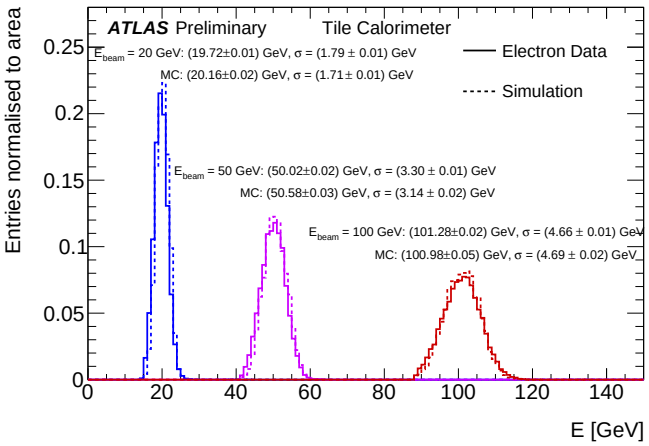

Fig. 7: Distribution of the total energy deposited in the Demonstrator for different electron beam energies (20 GeV, 50 GeV, and 100 GeV). The solid lines refers to the experimental data and the dashed lines to the simulated data with Monte Carlo simulations [12].

The energy response and resolution of the Demonstrator module to positive pions, kaons, and protons was studied using energies from 16 to 30 GeV. Fig. 8 shows the energy response ratios for protons ($R^{\langle E^{raw}\rangle} = \frac{\langle E^{raw}\rangle}{E^{raw}_{beam}}$) of the measured and predicted energies by Monte Carlo (MC) as a function of the proton beam energy.

Finally, the response of the Demonstrator module to high-energy muons has been studied using 165 GeV muons at an incident angle of -90º. The ratio between the energy deposited (dE) in a cell and the track path-length along the same cell (dl) was calculated in order to study the residual dependence of the muon energy on the path length. Fig. 9 presents the

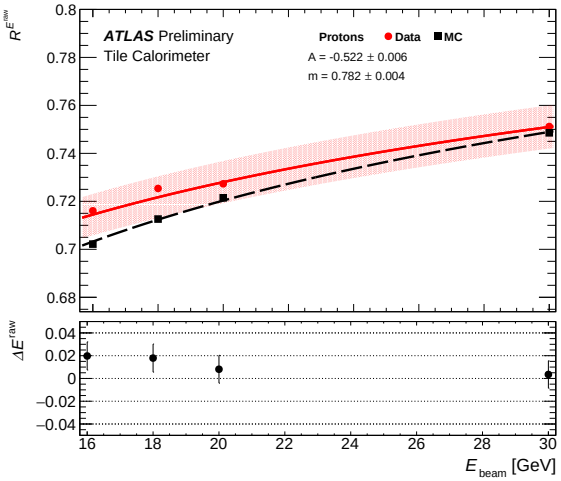

Fig. 8: Energy response ratios, $R^{\langle E^{raw}\rangle} = \frac{\langle E^{raw}\rangle}{E^{raw}_{beam}}$, as a function of the proton beam energy. Variations between the measured and MC data are within 2.5%. [12].

dE/dl ratio for the A8 cell of the Demonstrator module using measured and MC simulated data.

VI. Integration and Commissioning

After the validation of the electronics during the test beam campaigns, the Demonstrator module was installed into the ATLAS experiment in July 2019. It was commissioned during the Long Shutdown 2 (2019–2021), where the Demonstrator module was completely integrated into the ATLAS TDAQ system via the TilePPr Demonstrator module installed in the counting rooms.

During the installation and commissioning of the Demonstrator module several tests were done to validate its correct performance.

The signal quality of the high-speed links communicating the on-detector and off-detector electronics over fiber was studied after the insertion of the Demonstrator module. Link monitoring blocks were integrated in the TilePPr Demonstrator

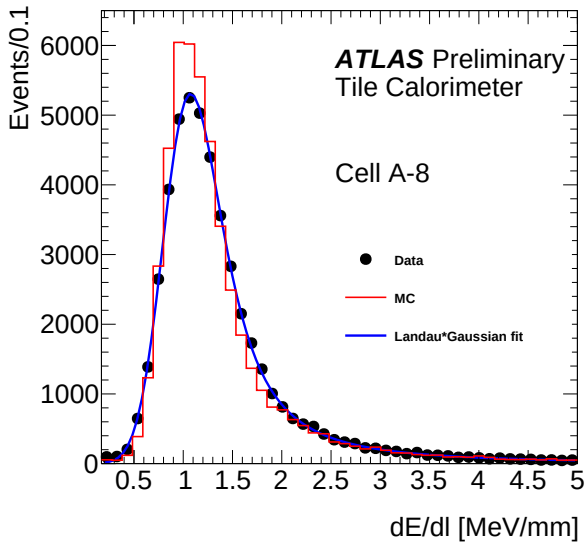

Fig. 9: Distribution of the quantity dE/dl for the cell A8 obtained using experimental (full points) and simulated muons (solid lines) at -90° hitting in the middle of Tile-row 2. [12].

using the eye scan circuitry of the Xilinx transceivers [13]. Fig. 10 presents the BER test results obtained for all the uplinks (4 channels per QSFP module). The BER test results indicates a good performance of the uplinks in terms of signal integrity with time margins between 0.34 and 0.52 Unit Interval (UI) at a BER level of 10^{-11}.

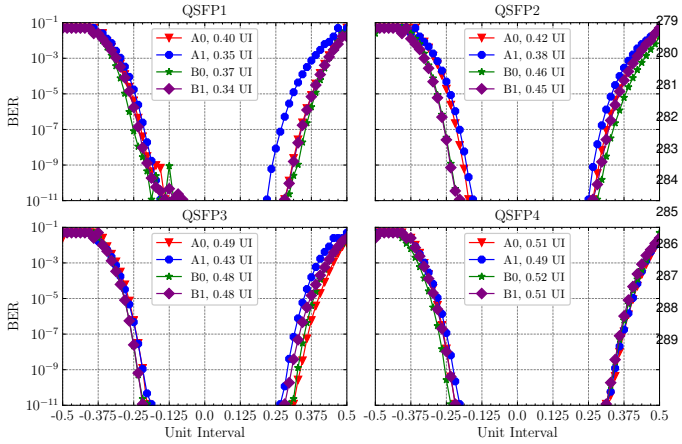

Fig. 10: BER test scan results corresponding to the sixteen uplinks at the TilePPr Demonstrator.

The frequency components of the readout channel were studied in order to detect faulty cables between the upgraded 3-in-1 card and the trigger adder cards during the installation and commissioning of the Demonstrator module. These faulty connections were introducing large noise levels at the output of the trigger amplifiers contributing to the distortion of the analog PMT signals and trigger sum signals. For this study, the TilePPr Demonstrator was prepared to store in FIFO memories up to 130k consecutive PMT samples from a single channel. Once the FIFO memory was full, the data samples are readout via IPbus for the computation of the Fast Fourier Transform (FFT) in a external computer. This procedure was followed to identify all faulty connections and replaced them by new analog cables when required. Fig. 11 presents the FFT results from one low-gain channel pedestal noise with a faulty trigger output connection. The FFT results includes two frequency components at 6.63 MHz and 13.37 MHz when the trigger output amplifier is enabled (red), adding noise to the analog trigger sum signals due to a misconnection between the 3-in-1 card and the adder card; and the FFT results when the trigger output amplifier is disabled (blue).

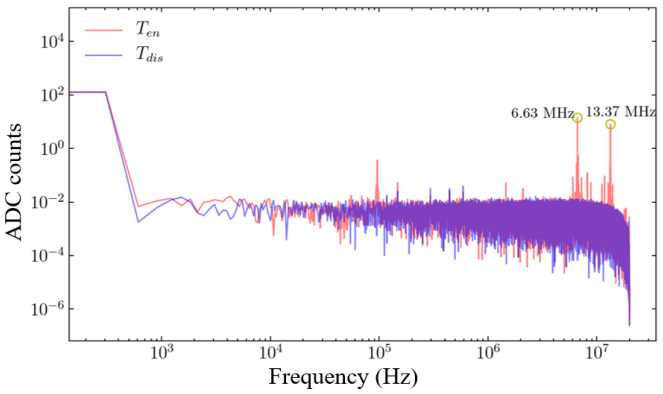

Fig. 11: Fast Fourier Transform analysis of the pedestal noise data of an non-terminated trigger output of one upgraded 3-in-1 card before (blue) and after (red) deactivating its trigger output.

As introduced in Section IV, the high-speed links interfacing the on-detector and off-detector electronics operate with fixed and deterministic latency in order to implement the architecture envisioned for the HL-LHC. Fig. 12 shows the phase variation measurements at the TilePPr Demonstrator between the clocks recovered from the uplinks and one distributed to the on-detector electronics. In order to perform such measurements, a phase monitoring circuit based on the Digital Dual Mixer Time Difference (DDMTD) circuit [14] was implemented in the TilePPr Demonstrator with a time resolution 12.189 ps.

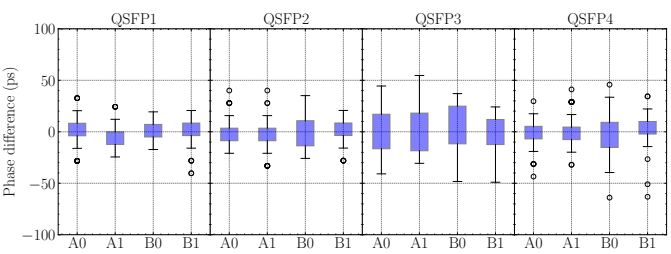

Fig. 12: Boxplot representations of 150 phase variation measurements resetting the on-detector electronics after each measurement.

Fig. 12 represents a boxplot with 150 measurements after resetting the on-detector electronics. As observed, the phase variations between the recovered and distributed clock do not exceed 100 ps_{pk-pk}. As studied in [15], these variations do not

introduce a significant degradation of the energy reconstruction algorithms.

The Demonstrator was included in the start of the Run 3 data-taking period (2022–2026) recording runs with cosmic rays, LHC splash events, laser and Charge Injection System (CIS) runs, showing a good performance in terms of noise levels, performance, and stability. Currently, the Demonstrator module provides physics data from proton-proton collisions with the rest of the TileCal modules. Fig. 13 shows an event display of one of the first collision events recorded in ATLAS at 13.6 TeV during the Run-3 data taking period. The red layer of the ATLAS view represents the hadronic calorimeter, where the energy depositions are shown as yellow boxes.

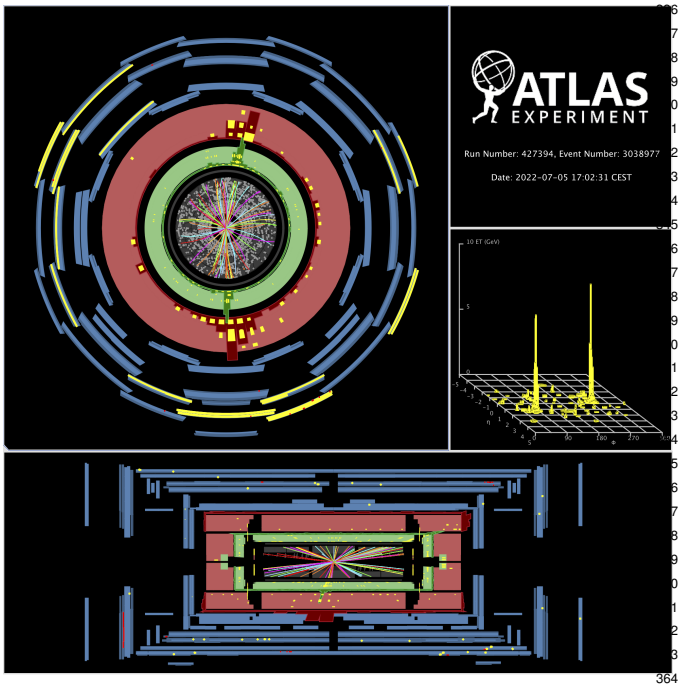

Fig. 13: Event display of a collision event recorded in ATLAS on 5 July 2022, when stable beams of protons at the energy of 6.8 TeV per beam were delivered to ATLAS for the first time by the LHC [16].

VII. CONCLUSIONS

In order to cope with the requirements for the HL-LHC, all the readout electronics of the Tile Calorimeter will be redesigned with a new clock and readout strategy able to provide high-granularity and full-digital input for the ATLAS trigger system.

As part of a wide R&D program for the upgrade of TileCal, a Demonstrator module containing the latest versions of the upgraded readout electronics was constructed in 2014. This module implements the clock and readout strategy for the HL-LHC, while it keeps backward compatibility with the current system by sending analog trigger signals to the ATLAS trigger system. In the off-detector electronics, the TilePPr Demonstrator board receives digitized data from the Demonstrator module at the LHC frequency, and transmits triggered data to the legacy RODs.

The Demonstrator module was evaluated during seven test beam campaigns (2015–2018) with different particle beams and range of energies. Finally, the Demonstrator module was inserted into the ATLAS experiment and commissioned during the Long Shutdown 2 (2019–2021), where it was successfully integrated into the legacy ATLAS DAQ system. During the current Run 3, the Demonstrator module is providing physics data with proton-proton collisions to the ATLAS TDAQ system in parallel with the rest of the TileCal modules.

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