A CMS Level-1 Track Finder for the HL-LHC

B. R. Yates for the CMS collaboration[1]

[1]*The Ohio State University,*
281 W Lane Ave, Columbus, OH 43210 USA

E-mail: brent.yates@cern.ch

ABSTRACT: The High-Luminosity LHC will put significant demands on trigger systems. To control trigger thresholds, the CMS Collaboration is designing a novel Level-1 track trigger. The Outer Tracker will use modules with pairs of sensor layers to read out hits compatible with charged particles above 2-3 GeV. The system will combine these front-end trigger primitives to reconstruct tracks, providing a measurement of p_T, η, ϕ, and z_0. This proceeding will introduce the CMS L1 track finding system: the algorithm and its estimated performance, hardware prototypes, and the unique challenges associated with this system.

KEYWORDS: CMS, track trigger, level one, L1, HL-LHC

Contents

1 Introduction

The increased luminosity in the proposed High Luminosity Large Hadron Collider (HL-LHC) upgrade [1, 2] offers some unique challenges to the continued operation of the Compact Muon Solenoid (CMS) detector [3]. With the current conditions of the LHC [4, 5] a proton-proton bunch crossing (bx) occurs every 25 ns with a peak instantaneous luminosity of $2 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$, resulting in a pile-up (PU) of approximately 20. The bx interval results in an initial data rate of 40 MHz, which is far too much information to read out from the detector and store on current hardware. The CMS detector employs a technique known as a trigger [6]. The CMS trigger consists of two main parts: the Level-1 (L1) trigger, and the High Level Trigger (HLT). The L1 trigger uses information from the calorimeters and muon system. This reduces the data rate to 100 kHz, which is then passed to the HLT server farm. The final output of the HLT is 1 kHz, which can be comfortably saved to disk for offline processing by analyzers.

The HL-LHC upgrade will increase the instantaneous luminosity to $7.5 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$, increasing the PU to roughly 200. In order to handle this increased luminosity, by reducing the data rate to a reasonable value, the CMS collaboration has decided to introduce a L1 Track Trigger [7]. The L1 Track Trigger will allow the CMS trigger system to include information from the precision silicon tracker, while keeping the trigger decision time at a resonable rate. The full trigger path is shown in Fig 1.

This proceeding will detail the creation of the CMS L1 Track Trigger, including: the algorithm, firmware development, target hardware, and the current status as of this publication.

2 The L1 Track Trigger algorithm

The Level-1 Track Trigger upgrade will make use of the proposed upgrades to the CMS silicon tracker. These changes include six barrel layers and five endcap disks, and a tilted geometry for
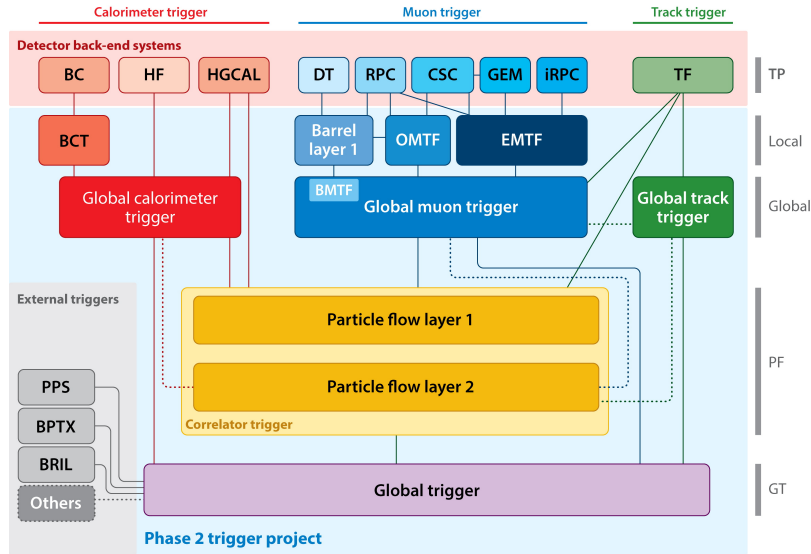
Figure 1. The full CMS L1 trigger path, including the Track Trigger, for the HL-LHC upgrade.

the first three barrel layers. The first three layers of the barrel, and the bottom half of the endcap disks, are made of pixel-strip (PS) detectors, while the rest of the layers are made of strip-strip (2S) detectors. The PS detectors are specially designed for the high occupancy, and harder radiation, closer to the beam pipe.

The L1 Track Trigger algorithm starts by reading information from the pair of modules in a single layer, known as a stub, giving a measurement of the transverse momentum (p_T) of a charged particle. Charged particles producing tracks with a large bend (corresponding to a p_T below 2 GeV) are rejected. Next, a tracklet is formed using pairs of neighboring stubs (Fig. 2 a). These tracklets are used as seeds for extrapolating to other layers, known as projections (Fig. 2 b). If a projection overlaps with a physical hit in the subsequent layers, a potential track is found. A Kalman filter takes all potential tracks from all seeding combinations, and produces a best track fit (Fig. 2 c).
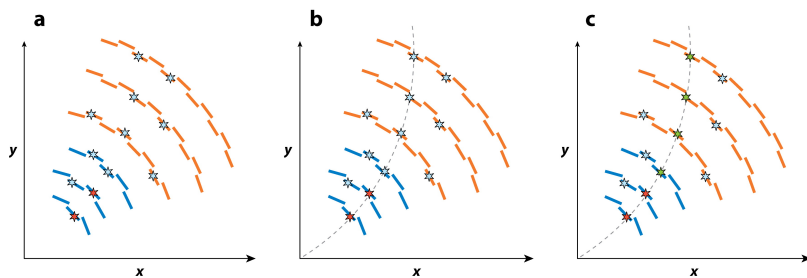
Figure 2. A diagram of the L1 Track Trigger algorithm, including the seeding (a), projecting (b), and fitting (c) stages.

3   Implementation

The designed implementation of the L1 Track Trigger will run at 240 MHz with a time multiplexing (TMUX) of 18. This TMUX gives each module 18 bx, or 108 clock cycles, to processes data. The entire φ-region of the detector is divided into nine non-overlapping regions, known as nonants, resulting in at most one sector-to-sector crossing for the 2 GeV minimum track p_{T} requirement. For the physical hardware, we have chosen to use a field-programmable gate array (FPGA), specifically the Xilinx Virtex UltraScale+$^{\text{TM}}$. The benefits of using FPGAs over application-specific integrated circuits (ASICs) includes: flexible designing, ease of changes and/or updates, off-the-shelf components, and the designs can improve as the industry improves. The track finding algorithm is broken into several modules: Input Router, VM Router, Tracklet Engine, Tracklet Calculator, Projection Router, Match Engine, Match Calculator, Purge Duplicates, and Kalman Filter. The functionality of each is detailed below.

Input Router

The Input Router (IR) is responsible for collecting all inputs from the DTC, and organizing them into the appropriate φ nonants.

VM Router

The VM Router (VMR) futher divides the outputs of the IR into the various virtual modules (VMs). The VMs allow for fast, parallel processing of stubs in different regions of the detector.

Tracklet Engine

The Tracklet Engine (TE) is responsible for organizing pairs of adjacent stubs into the seeds required for the track finding algorithm.

Tracklet Calculator

The Tracklet Calculator (TC) subsequently produces the projections based on the seeds created in the TE.

Projection Router

The Projection Router (PR) organizes the resulting projections from the TC.

Match Engine

The Match Engine (ME) is responsible for grouping all possible stub and projection matches created by the TE and TC.

Match Calculator

The Match Calculator (MC) sorts through the stub/projection pairs from the ME, and finds the best match among the redundant collection. This collection is known as a full match.

Purge Duplicates

The Purge Duplicates (PD) stage looks for any duplicate full matches the MC may have found, resulting from seeding in multiple layers simultaneously.

Kalman Filter

The Kalman Filter (KF) takes the final, cleaned, collection from the PD and produces a best-fit track across all layers containing a full match.

We are also in the processes of creating super-modules to help with resource management. These modules are known as the Tracklet Processor (TP) and Match Processor (MP). The TP combines the TE and TC stages into a single super-module, while the MP combines the PR, ME, and MC stages into a single super-module.

The L1 Track Trigger algorithm was also implemented in a software emulation to measure performance. Using simulated events with top quark pair production, and a PU of 200, an efficiency above 95% is observed for the desired pseudorapidity coverage ($|\eta| < 2.5$), as well as a very good resolution on the reconstructed lateral impact parameter, z_0.

4   Hardware

As mentioned, the target hardware is the Xilinx Virtex UltraScale+$^{\text{TM}}$ FPGA chipset. The current demonstrator is using the Apollo module [8]—named after the Apollo missions—which consists of a Service Module (SM) and a Command Module (CM) as shown in Fig. 3. The SM contains a Zynq system on a chip (SoC) which allows the module to communicate with the outside world. The CM plugs directly into the SM, and contains both a Virtex and Kintex FPGA chip. Demonstrator boards are located at CERN in the CMS Tracker Integration Facility (TIF), Boston University, and Cornell University.
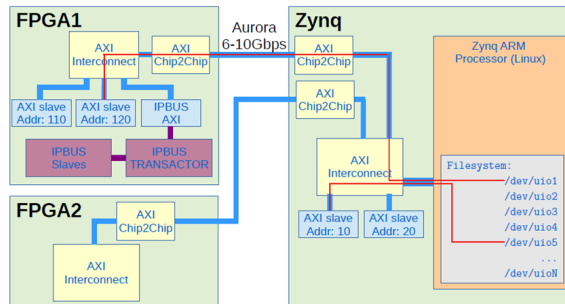

Figure 3. A block diagram of the Apollo module, including the CM (left) and the SM (right).

The Apollo boards are currently on revision 1 (Fig. 4 left), which has been fully evaluated at a link speed of 25 Gbps via a FireFly optical connector, with a bit error rate below 10^{-16}. Cornell University is in the processes of testing revision 2 of the CM. Revision 2 (Fig. 4 right) of the SM

is expected around the end of November 2021. The target delivery date to CERN is mid to late 2024, while installation and commissioning will take place in 2025, and the L1 Track Trigger will be ready for HL-LHC data starting in 2027.
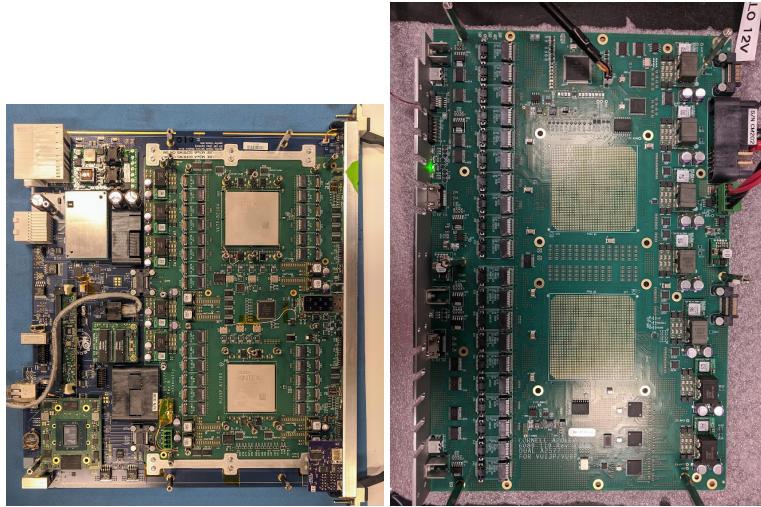

Figure 4. Revision 1 of the SM+CM (left) and revision 2 of the CM (right)

5   Conclusion

A robust algorithm for the CMS L1 Track Trigger has been developed to handle the run conditions of the HL-LHS upgrade; it is currently being tested on physical hardware. The algorithm was designed to run at 240 MHz with a time multiplexing of 18. The target hardware is the Xilinx Virtex UltraScale+$^{\text{TM}}$, and the current demonstrator is the Apollo module revision 1. The development of the L1 Track Trigger is on target for delivery, installation, and commissioning between 2024 and 2025. The system will be fully ready for the start of the HL-LHC in 2027.

References

[1] F. Zimmermann, *CERN upgrade plans for the LHC and its injectors*, *PoS* **EPS-HEP2009** (2009) 140.

[2] G. Apollinari, I. Béjar Alonso, O. Brüning, P. Fessia, M. Lamont, L. Rossi et al., *High-Luminosity Large Hadron Collider (HL-LHC): Technical Design Report V. 0.1*, .

[3] CMS collaboration, *The CMS Experiment at the CERN LHC*, *JINST* **3** (2008) S08004.

[4] O. S. Bruning, P. Collier, P. Lebrun, S. Myers, R. Ostojic, J. Poole et al., *LHC Design Report Vol.1: The LHC Main Ring*, .

[5] L. Evans and P. Bryant, *LHC Machine*, *JINST* **3** (2008) S08001.

[6] CMS collaboration, *The CMS trigger system*, *JINST* **12** (2017) P01020 [1609.02366].

[7] D. Contardo, M. Klute, J. Mans, L. Silvestris and J. Butler, *Technical Proposal for the Phase-II Upgrade of the CMS Detector*, tech. rep., Geneva, Jun, 2015.

[8] E. S. Hazen, A. Albert, J. Butler, Z. Demiragli, K. Finelli, D. Gastler et al., *The APOLLO ATCA Platform*, *PoS* **TWEPP2019** (2020) 120.