

Testing of the Micromegas detector trigger electronics for the New Small Wheel Phase I upgrade of ATLAS detector

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In conjunction with the High Luminosity upgrade of the LHC, the ATLAS detector is also undergoing an upgrade to handle the significantly higher data rates. The muon end-cap system upgrade in ATLAS, lies with the replacement of the Small Wheel. The New Small Wheel is expected to combine high tracking precision with upgraded information for the Level-1 trigger. To accomplish this, small Thin Gap Chamber and Micro-Mesh Gaseous Structure detector technologies are being deployed. The Micro-Mesh Gaseous Structure detector technology is equipped with three types of electronic boards to produce signals from muons to send them to trigger and tracking processors. These boards are the Micromegas Front End with 8 VMM chips, the Level 1 Data Driver Card and the ART Data Driver Card. The Address in Real Time signals produced by VMMs in the front ends are propagated through the trigger electronics and sent to the detector's Trigger Processor which provides segment of the Level 1 Accept trigger signal to ATLAS. In order to test the functionality and efficiency of the trigger electronics, various tests are being conducted at building 899. During the "Address in Real Time connectivity test", Address in Real Time pulses generated synchronously are sent through the trigger electronics and to the Trigger Processor. This test is performed to validate every New Small Wheel sector and is essential to identify front end electronics or fibers that must be tested, repaired or replaced. Finally, the trigger processor's data acquisition, firmware and trigger logic are being tested with cosmics data. In this paper, the various tests and results from cosmics data are presented.

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1. Introduction: ATLAS Phase I upgrade

The Large Hadron Collider (LHC) complex will be upgraded in several phases which will allow the reach for particle physics research to be significantly extended. The improvements will result in the luminosity increasing to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and with luminosity leveling, the integrated luminosity is expected to be 3000 fb^{-1} after about 10 years of operation [2].

Two major issues represent a serious limitation on the ATLAS detector [1] performance beyond its designed luminosity. The performance of the muon tracking chambers (in particular in the end-cap region) degrades with the expected increase of cavern background rate and the approximately 90% of fake high p_T Level-1 muon triggers that appear to come from the interaction point due to low energy particles produced by the material around the end-cap region [3].

In order to solve the two problems together, ATLAS is replacing the present muon Small Wheels with the 'New Small Wheels' (NSW). The NSW is a set of precision tracking and trigger detectors (Micromegas and sTGC) able to work at high rates with excellent real-time spatial and time resolution [4].

2. The Micromegas detector

The Micromegas is a gaseous detector operating under high voltage. Muons pass through the detector ionizing the gas and producing electrons that are drifting to its readout strips by the high voltage. Eight layers of this technology make up a Micromegas double wedge [5] and the readout signals on each layer formed by a passing muon [6] are used for track reconstruction.

The detector operates using three custom made electronic boards: The Level-1 Data Driver Card (L1DDC) [7], the ART [8] (Address in Real Time) Data Driver Card (ADDC) and the MicroMegas Front End with 8 VMM [9] chips (MMFE8). A connection diagram of these components is shown in Figure 1. In total, each Micromegas sector houses 128 MMFE8s, 16 ADDCs and 16 L1DDCs.

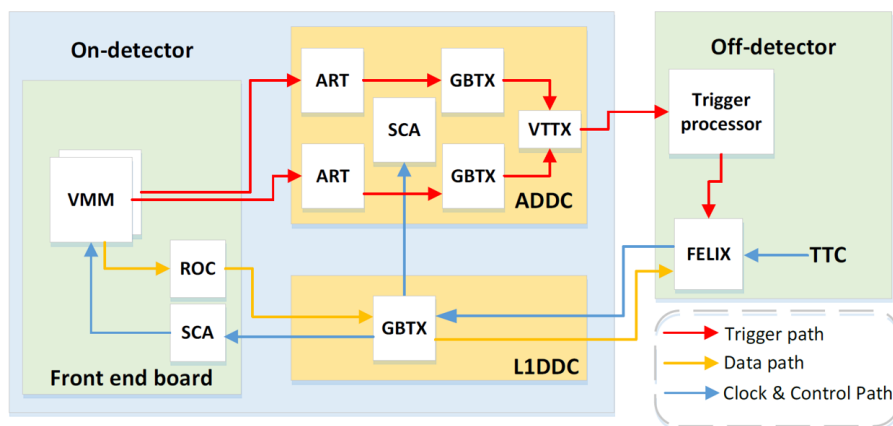


Figure 1: On the trigger path, the ADDC deserializes the ART data received by the VMMs and phase aligns them to the TTC clock produced by ALTI [10]. Then it identifies which strip is hit and sends the ART data to the MicroMegas Trigger Processor (MMTP) [11]. Off-detector, the MMTP makes a trigger decision based on the strips that had a hit and sends it to the Front-End Link eXchange (FELIX) system [12].

3. Testing of the Trigger electronics

In order to test the Micromegas trigger electronics, a setup is configured at Building 899 at CERN to test every Micromegas double wedge together with the trigger electronics. Two FELIX servers are used, one to configure all the cards through the L1DDC and one to receive data from the MMTP. An ALTI module [13] provides the TTC signals and clock to all the electronics. Data acquisition is orchestrated by applications in the Software Readout Driver (SW ROD) [14] machine. This machine is also used to operate run control.

A typical test run on each detector is to measure the Trigger Processor Input Phase. Since the ADDCs from different positions on the detector have different fiber lengths, all the ART data streams from the fibers connected to MMTP must be synchronized. Thus, selecting the best possible offset and phase is critical for data acquisition. An example is shown in Figure 2.

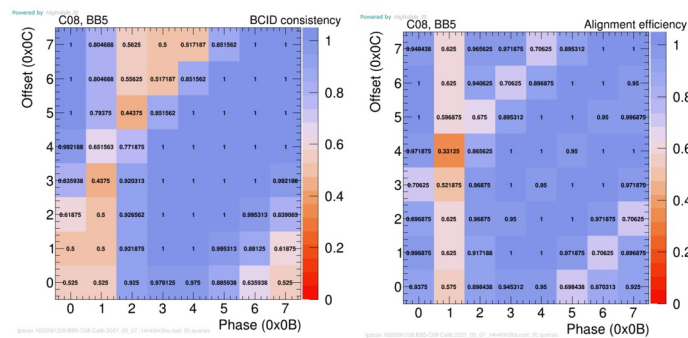


Figure 2: Trigger Processor Input Phase plot for different phases and offsets for a Micromegas sector. The BCID consistency is the fraction of the fibers that have the most commonly reported BCID whereas alignment efficiency is measured by counting sufficiently consecutive BCIDs for a fiber.

The VMM ART phase also needs to be aligned with the ART clock. ART signals from each VMM are delayed in the input of the ART ASIC of the ADDC by different amounts. After finding efficient phases, we then choose the phase in the middle of the first plateau of efficient phases. A plot of this test is shown in Figure 3 (left).

The final validation test of the detector electronics is their connectivity altogether. Using the VMM internal pulsar, 100 ART hits are produced from every one of its 64 channels. In total, 51 200 ART hits are produced per MMFE8 and are propagated through the trigger electronics. Then, a Level-1 Accept signal (L1A) (which decides that a trigger has been made) is created also artificially to match the ART timing. Data from all MMFE8s of all layers are passed to FELIX and eventually read out in a 2D histogram as shown in Figure 3.

It is rather impossible for all hits to be read out as there can be small inconsistencies in any step of the trigger scheme. Throughout all of this procedure, multiple errors can be identified regarding the ADDCs, the VMMs or even the cabling. Every Micromegas double wedge was tested for NSW at building 899 before being installed on the Wheel on the commissioning site.

In the previous tests described, the internal pulsar was generating ART hits towards the trigger electronics. A final test of the scheme is to produce actual triggers from cosmic muons with the trigger processor firmware. This was put to test at building 899 with several sectors. Using the

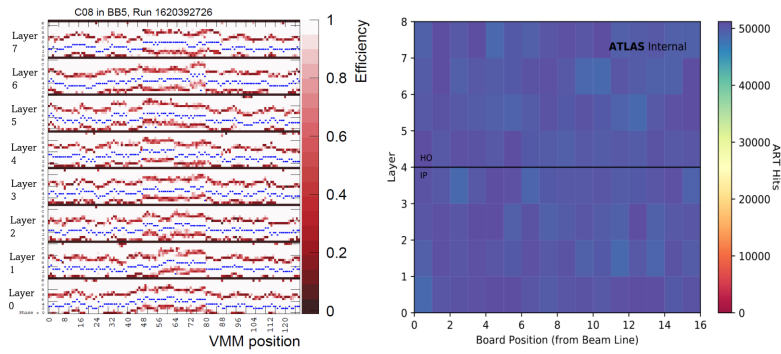


Figure 3: ART phases of all VMMs on detector (left) and ART hits from all MMFE8s (also known as 'Connectivity' plot) on the right.

trigger processor algorithm, a decision is made on which ART hits construct a trigger and sends an L1A signal to FELIX, noting which ART hits would form a track. An occupancy plot (Figure 4) can therefore be created of all the ART hits that caused a trigger decision.

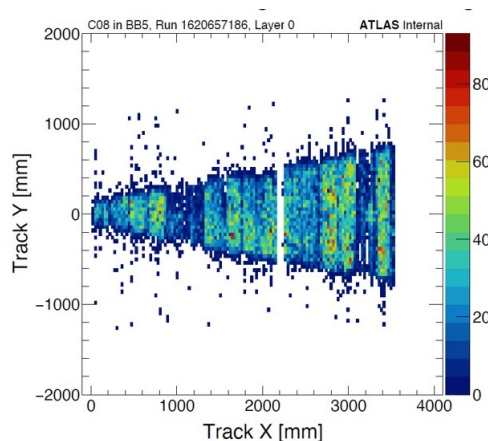


Figure 4: Example of an occupancy plot on Layer 0 of a Micromegas sector.

Masking noisy VMM channels significantly improves data acquisition as seen in Figure 4 since it prevents the MMTP readout lines from overflowing. Further tests and improvements of the trigger algorithm are under development in order to fully optimize the detector trigger electronics.

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References

- [1] The ATLAS Collaboration et al (2008) *The ATLAS Experiment at the CERN Large Hadron Collider*, 2008 JINST 3 S08003
- [2] G. Apollinari, I. Bejar Alonso, O. Bruning, P. Fessia, M. Lamont, L. Rossi, L. Tavian (2017) *High-Luminosity Large Hadron Collider (HL-LHC) Technical Design Report* [doi: <https://doi.org/10.23731/CYRM-2020-0010>]
- [3] ATLAS Collaboration (2013) *Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System* [Report number: CERN-LHCC-2013-018, ATLAS-TDR-023]
- [4] ATLAS Collaboration (2013) *ATLAS New Small Wheel Technical Design Report* [Report number: CERN-LHCC-2013-006, ATLAS-TDR-020]
- [5] T. Alexopoulos et al. (2020) *Construction techniques and performances of a full-size prototype Micromegas chamber for the ATLAS muon spectrometer upgrade* Nuclear Instruments and Methods in Physics Research [doi: <https://doi.org/10.1016/j.nima.2019.04.040>]
- [6] T. Alexopoulos, M. Dris (2017), *Signal Formation in Various Detectors* [arXiv:1406.3217v3 [hep-ex]]
- [7] P. Gkoutoumis (2016), *Level-1 data driver card of the ATLAS new small wheel upgrade compatible with the phase II 1 MHz readout scheme*, [doi: [10.1109/MOCAS.2016.7495115](https://doi.org/10.1109/MOCAS.2016.7495115)]
- [8] Component: ART ASIC, “Address in Real-Time” Concentrator ASIC, private communication, 2016
- [9] G. Iakovidis (2020), *VMM3a, an ASIC for tracking detectors* [doi:10.1088/1742-6596/1498/1/012051]
- [10] B.G. Taylor (1998), *TTC Distribution for LHC Detector*, [doi: [10.1109/23.682644](https://doi.org/10.1109/23.682644)]
- [11] NSW Trigger Processor Group (2020), *New Small Wheel Trigger Processor: Firmware Requirements & Implementation* [ATLAS note]
- [12] N. Ilic, J. Vermeulen, S. Kolos (2019) *FELIX: the new detector interface for the ATLAS experiment* [doi: <https://doi.org/10.1051/epjconf/201921401023>]
- [13] Predrag Kuzmanovic (2018), *Development and testing of the ALTI module for timing and synchronization in the ATLAS Experiment at CERN*, [CERN-THESIS-2018-335]
- [14] S. Kolos (2021), *New software based readout driver for the ATLAS experiment*, [doi: [10.1109/TNS.2021.3083987](https://doi.org/10.1109/TNS.2021.3083987)]